AI Is Scaling Faster Than Test

Rethinking Wafer, Chip and Module Test for the Photonics Era

September 1, 2026

André Lalonde
President – ficonTEST Business Unit

TRANSFORM TOMORROW

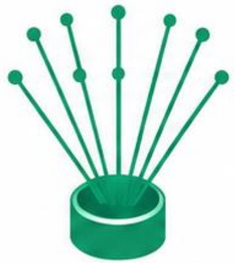
With the AI Explosion we need More…

MORE BANDWIDTH



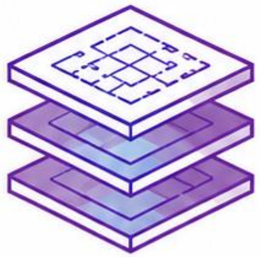
- Higher data rates
- More lanes
- More channels

MORE PHOTONICS



- More optical I/O
- More integration
- More performance

MORE PROCESS INTEGRATION

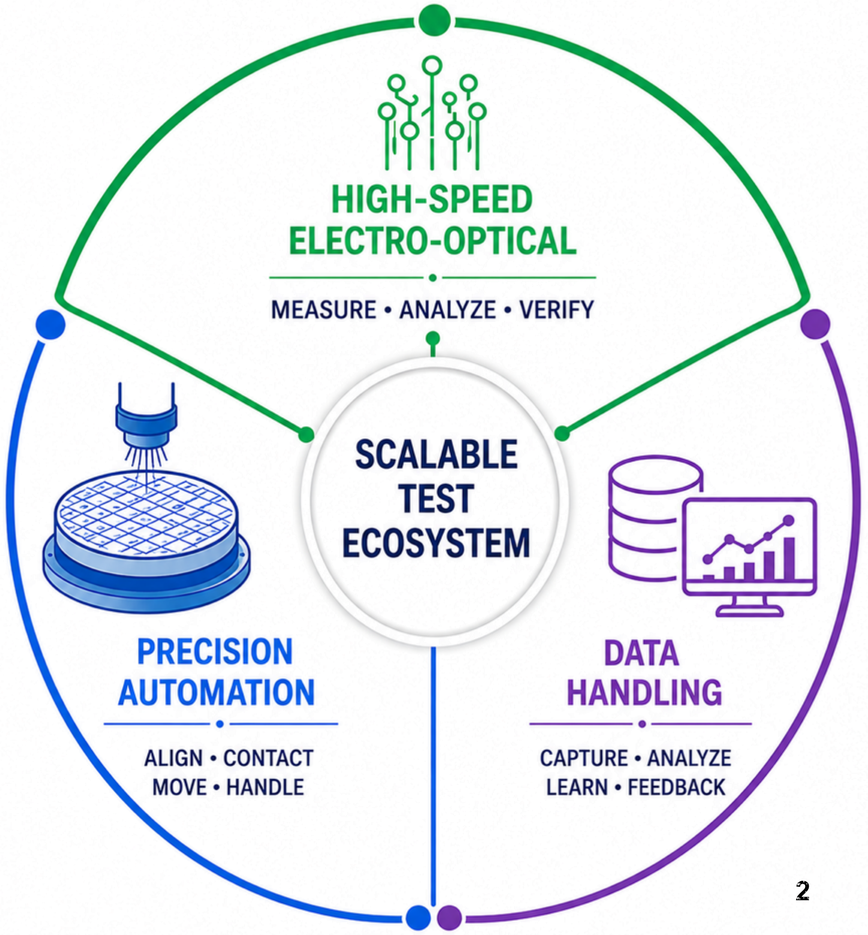


- Heterogeneous integration
- Advanced packaging
- System in a package

MORE TEST COMPLEXITY



- Multi-domain test
- Tighter tolerances
- More parameters



AI Is Scaling Faster Than Test

The AI revolution isn't only a compute problem. It's a manufacturing scale problem — and test is rapidly becoming one of its biggest bottlenecks.

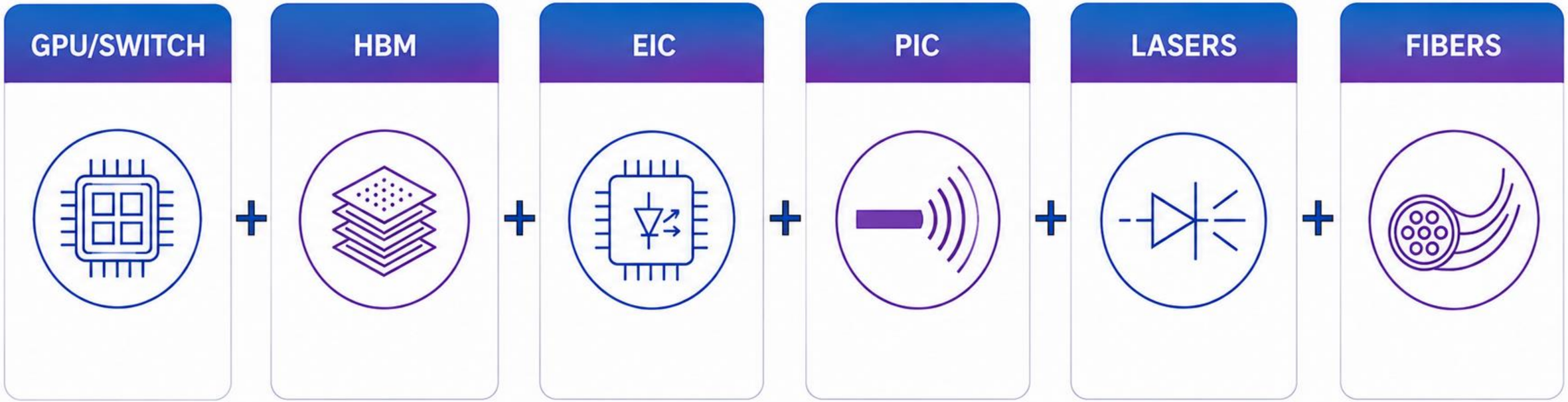


- **Greater lanes + higher baud rates**
- **Greater number of optical channels + electrical I/O**
- **Tighter tolerances + higher packaging complexity**
- **Higher device value → higher cost of test escapes**

The manufacturing challenge is no longer simply whether a device can be measured; it is whether millions+ can be measured economically

Moore's Law Is Becoming a Packaging Problem

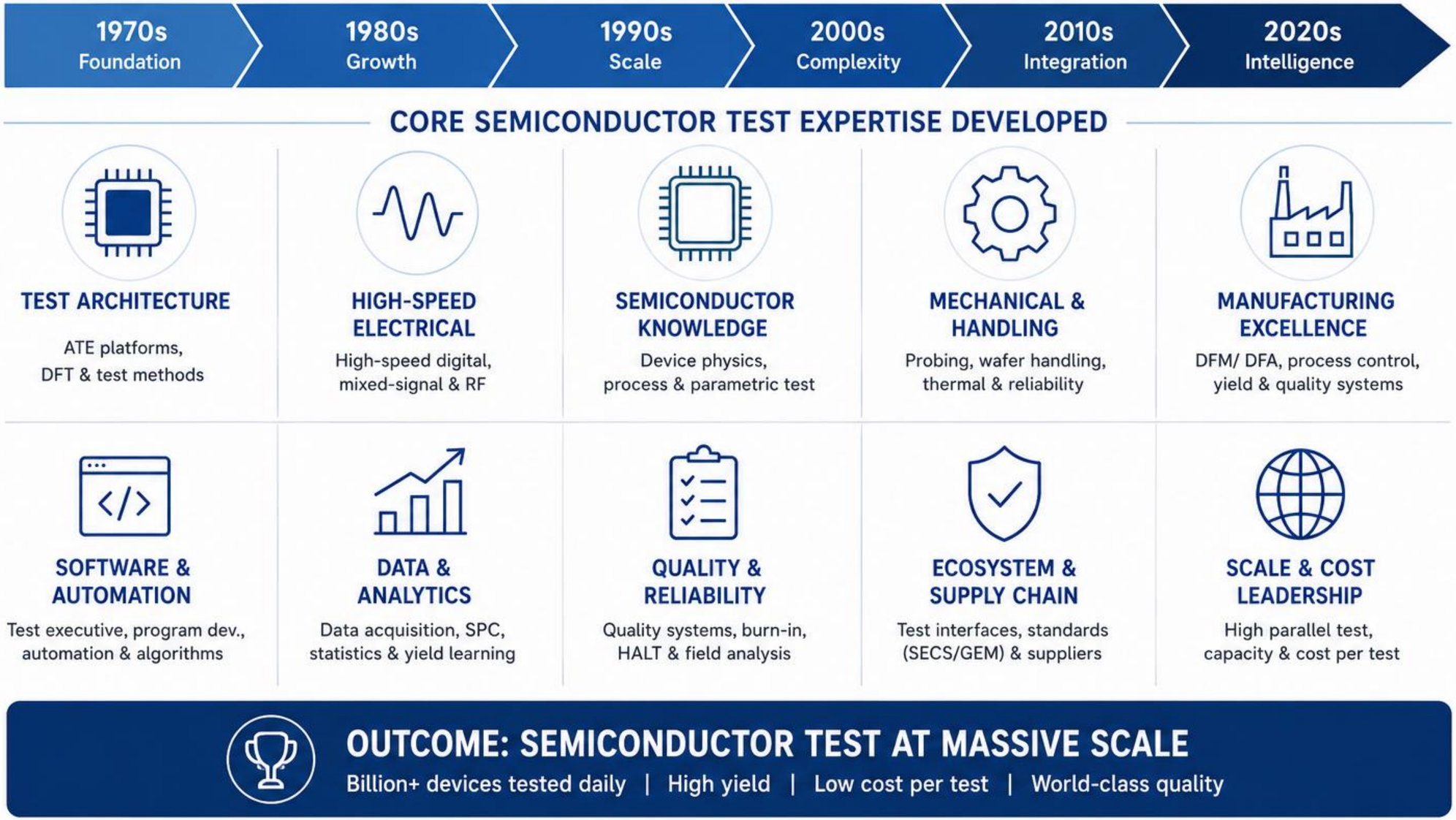
The device is no longer a chip. It is a system. Test architecture must evolve accordingly.



Photonics must now meet semiconductor standards for volume, yield, quality, and reliability—while adding the optical, precision alignment, automation, and data expertise required beyond traditional electrical test.

The next five years may require the photonics industry to build more high-volume manufacturing and test capacity than it developed during the previous twenty-five.

Photonics Breaks Traditional Semiconductor Test



Photonics Breaks Traditional Semiconductor Test

NEW PHOTONIC TEST CAPABILITIES REQUIRED



PHOTONIC DEVICE ENGINEERING

Modulators, detectors, lasers, couplers, PIC building blocks



OPTICAL ARCHITECTURE & SYSTEM DESIGN

PIC architecture, optical system design, wavelength planning



OPTICAL ENGINEERING & MEASUREMENT

Propagation, insertion loss, ER/OSNR, dispersion, crosstalk, polarization



PRECISION ALIGNMENT & POSITIONING

Sub-micron alignment, vibration control, 6-DOF control



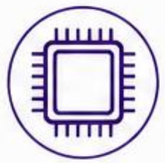
MATERIALS & FABRICATION

SiPh / III-V / LN, heterogeneous integration, wafer-level features



FIBER & COUPLING TECHNOLOGY

Fiber attach, array align, mode control, low-loss coupling



PACKAGING & INTEGRATION

Optical packaging, hermetic sealing, CPO / LPO integration



NEW TEST METHODOLOGIES

Electro-optical test, wavelength sweep, coherent & bidirectional



PHOTONIC DATA & AI ANALYTICS

Optical data models, ML/AI for yield, anomaly detection



STANDARDS & QUALITY SYSTEMS

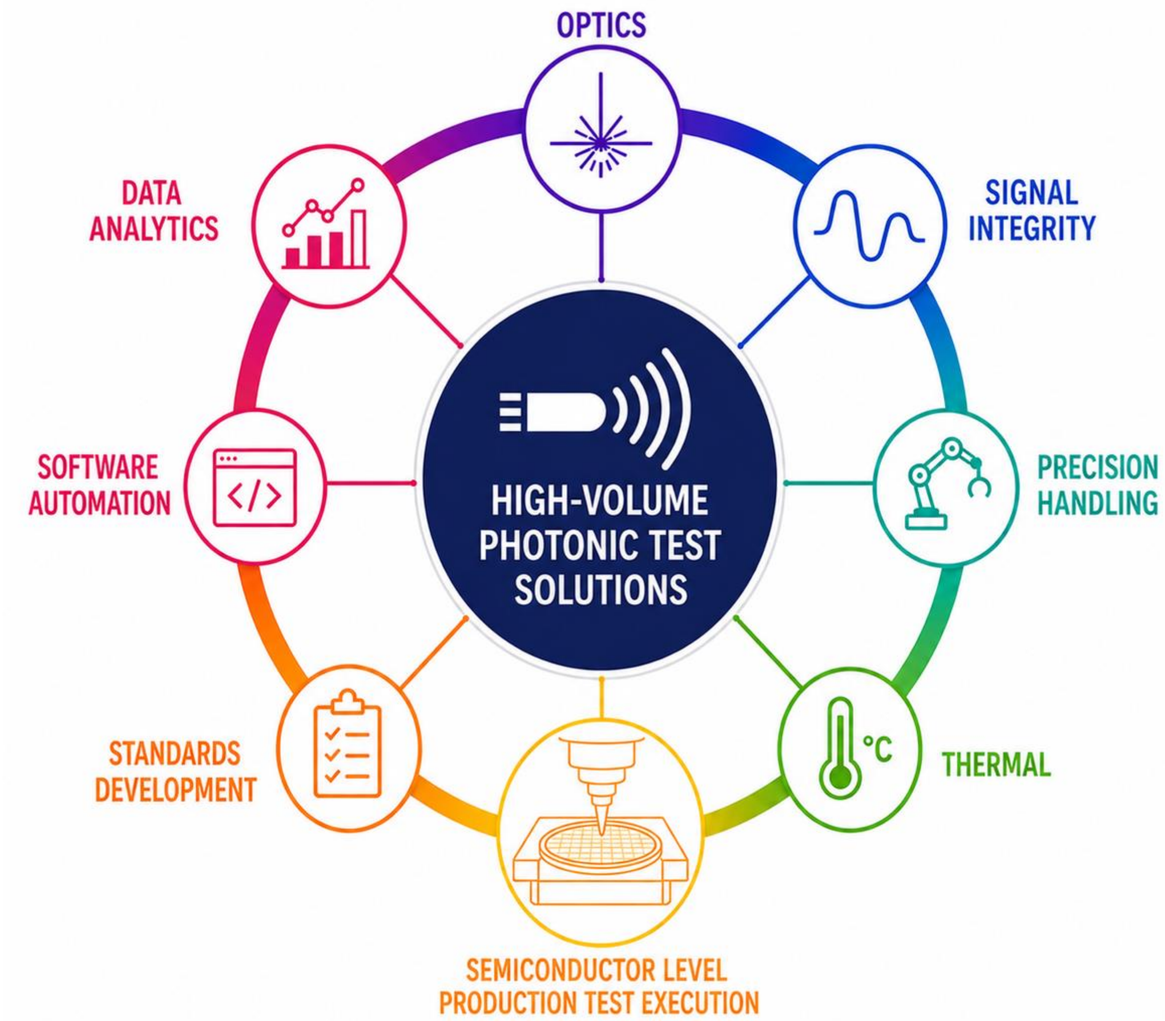
Photonic PDKs, test standards, reliability models



OUTCOME: PHOTONIC TEST AT SEMICONDUCTOR SCALE

High-volume | High-yield | Low cost per device | Reliable | Scalable for the AI era

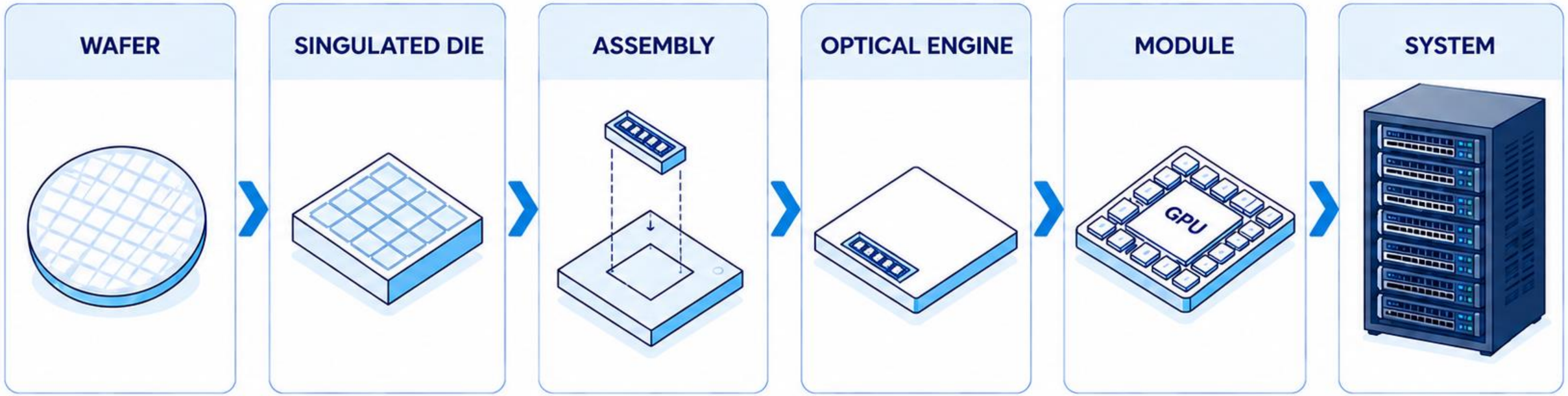
Integrated Disciplines to Enable Photonic Test at Semiconductor Scale



No single traditional test discipline solves the photonic production problem.

Scalability demands top-level expertise in each one of these categories for success.

Test Must Follow the Device Through Manufacturing



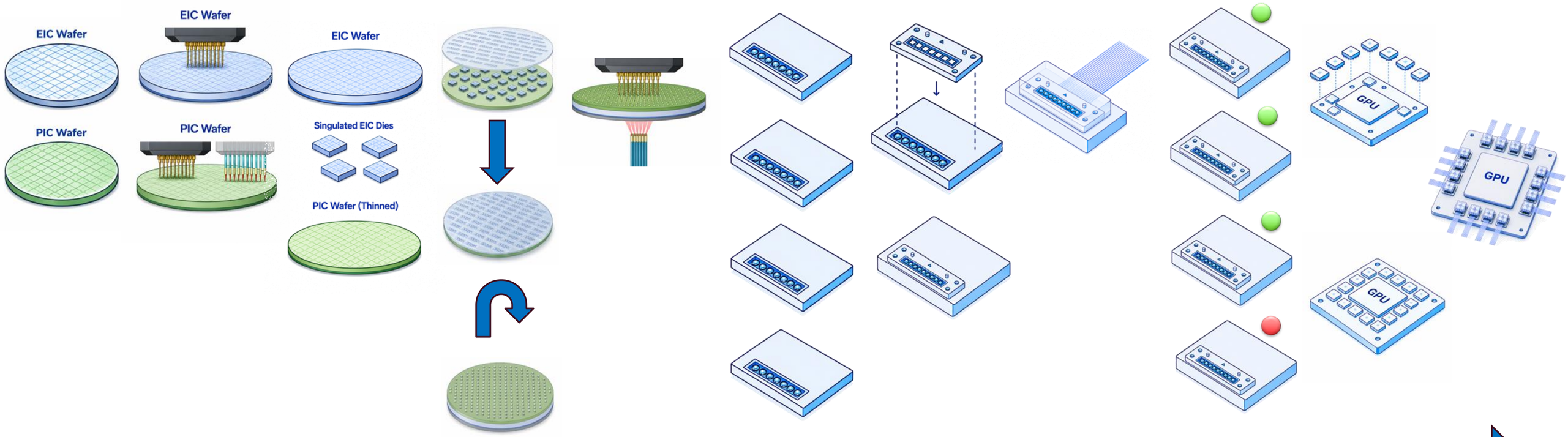
CPO PRODUCT FLOW: FROM WAFER TO SYSTEM

Insertion 1	Insertion 2	Insertion 3	Insertion 4
EIC Probe PIC Top Side Optical Probe	Dual-Side Wafer Electro-Optical Probing	Die / Engine Test	Module Test & Final Qualification (pre System)

INCREASING DEVICE VALUE – INCREASING COST OF FAILURE

Find Failures Early (COUPE example)

1. Start: Two Wafers
2. Insertion 1 Wafer Test
3. Singulate EIC Thin PIC Wafer & Place EICs
4. Lens Layer Added (Top Side)
5. Insertion 2 Dual-Side Wafer Test
6. Singulate COUPE ICs
7. Lens Array Attach (Optical Engine Assembly)
8. Insertion 3 Die / Engine Test
9. Known Good Die Passed to Assembly
10. Assemble into Module
11. Insertion 4 Module Test & Final Qualification

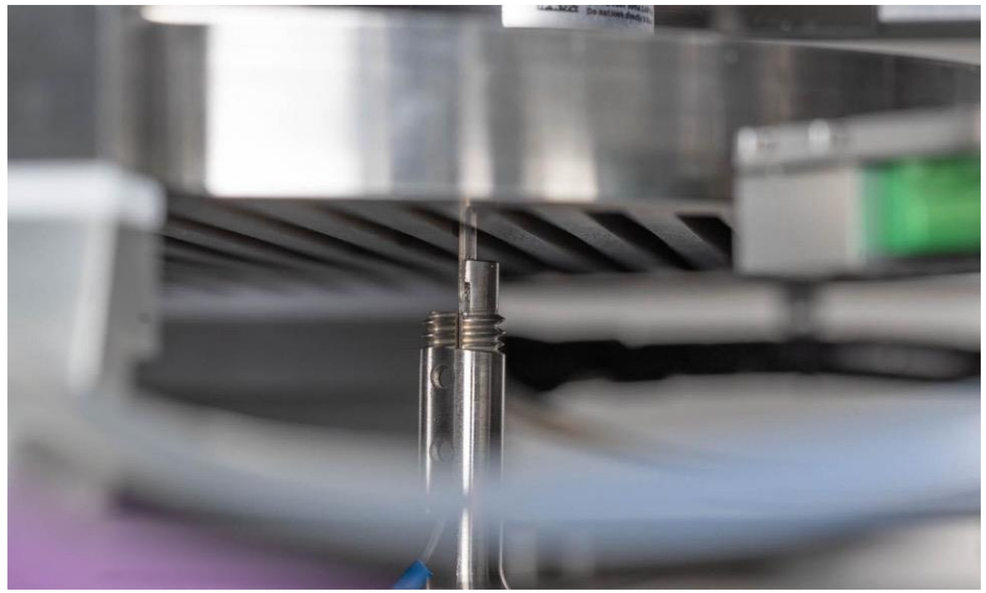


1× → 10× → 100× → 1,000× COST OF FAILURE

Every test insertion is an economic firewall — preventing a low-value defect from becoming a high-value failure.

Double-Sided Wafer Test Changes the Architecture





TOP
Electrical Probes / Probe Card

WAFER

Thermal Chuck

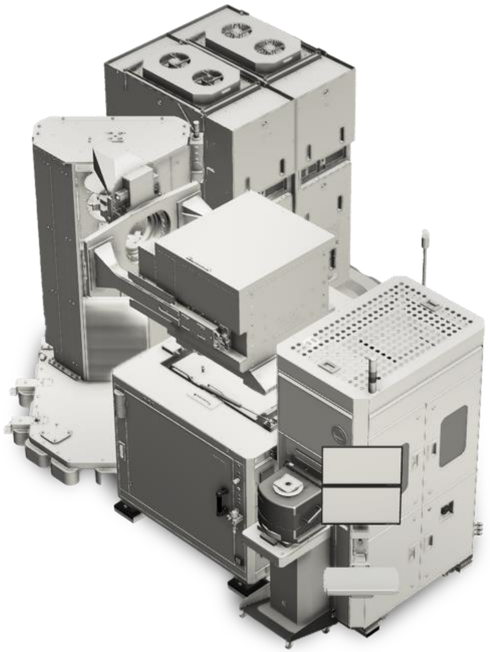
BOTTOM
Fiber Array Unit (FAU) Interface

INSERTION 2

Double-Sided Wafer Tester WLT-D2



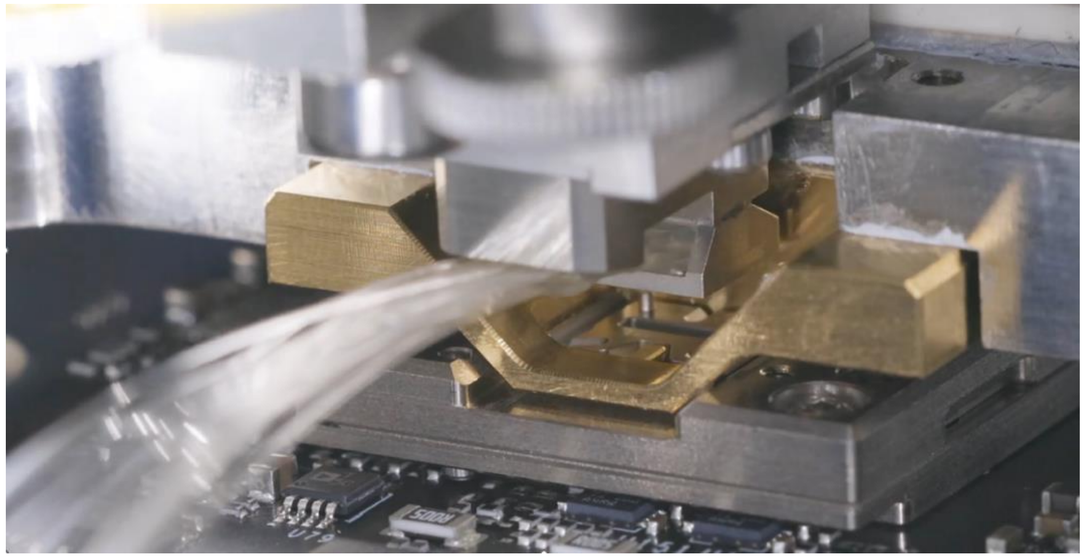




INSERTION 2

Singulation Creates a New Test Problems





TOP
Optical Head Assembly (OHA) / Fiber Array Unit (FAU)

Thermal Chuck

Chip

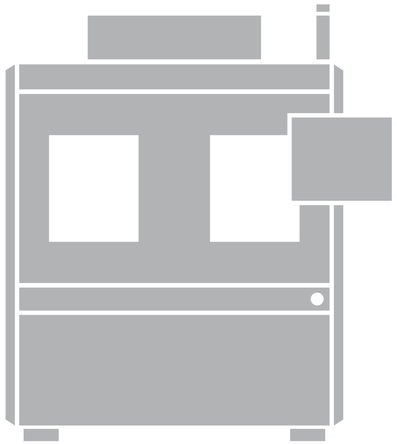
BOTTOM
High Speed Socket Interface

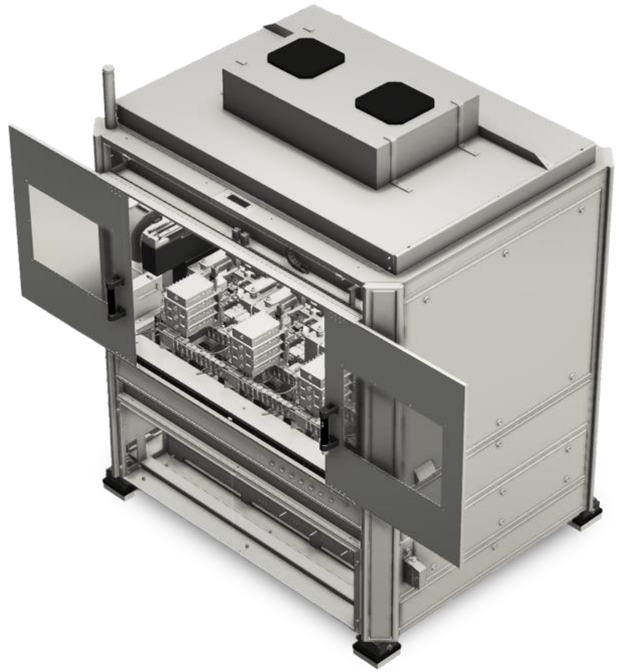
High Speed Probe Card

INSERTION 3

Double-Side Chip Test DLT-D2



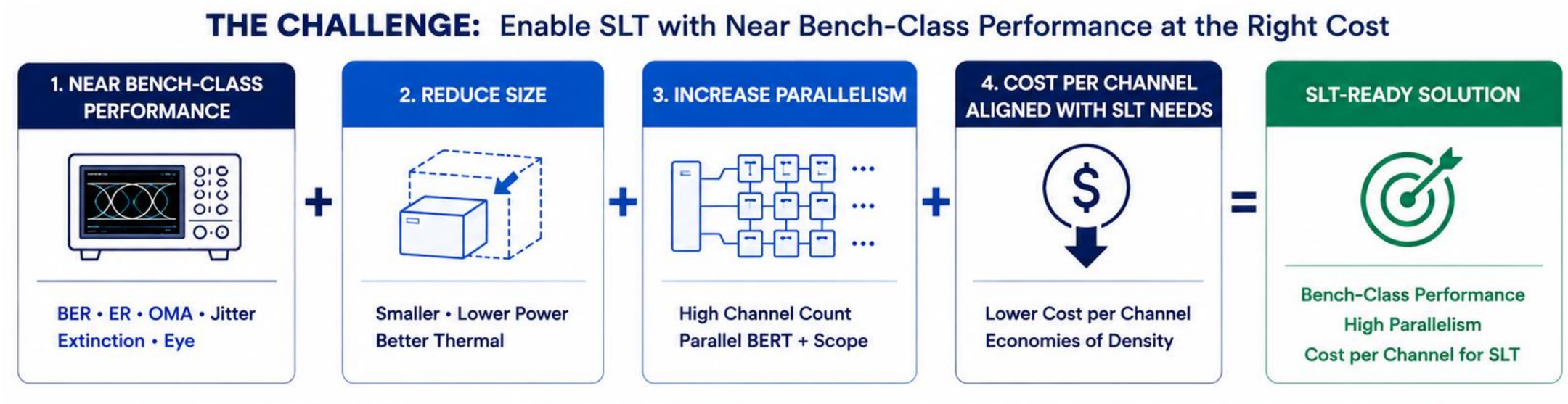




INSERTION 3

SLT vs ATE vs Characterization for Insertion 3

	SLT / Loopback	224G HSIO/ATE Production Test	Full Characterization
Role	**100% functional production screen**	Targeted 224G production measurements	Deep engineering measurement
Architecture	DUT optical loopback / mission-mode	**External 224G BERT/O'scope + automation**	Bench-class PPG/BERT + O'scopes
Coverage	Link, BER, lock, functional faults, power	Selected Tx/Rx parametrics	Full Tx/Rx performance & margins
Throughput	**Highest**	Medium	Lowest
Cost/device	**Lowest ($)**	Medium–High ($$)	Highest ($$$)
Best use	HVM screening	Targeted production coverage	Qual / margin / debug / correlation



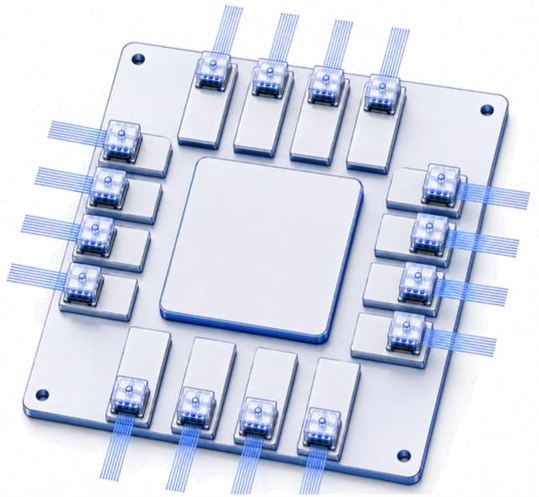
INSERTION 3

THE GOAL: Deliver bench-class insight and quality of test in a production-scale, cost-effective platform.

Module Test Moves From Characterization to Production



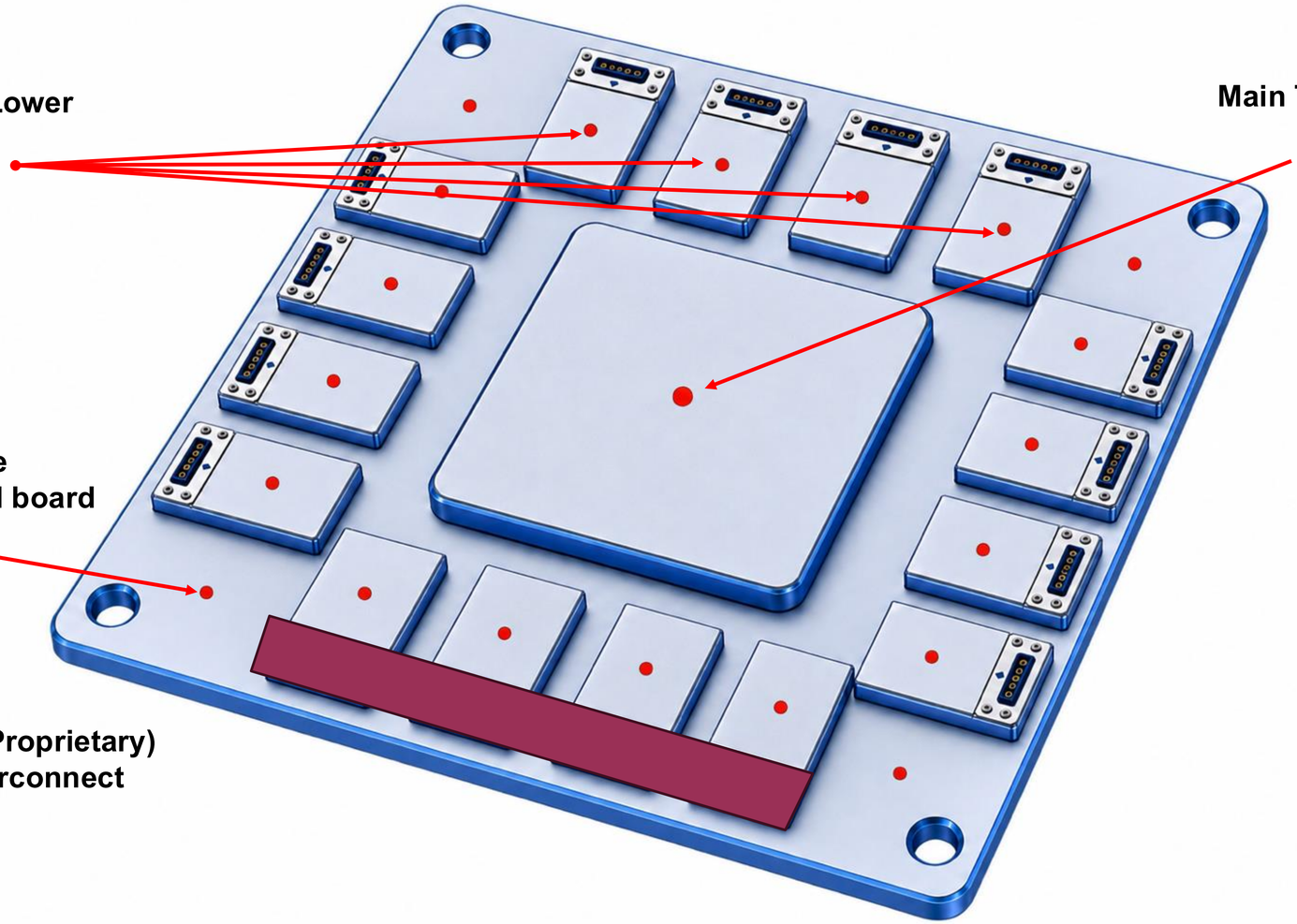
- **Standalone instruments:** Individual optical and electrical test equipment
- **Engineering Supervised:** Manual setup, execution and troubleshooting
- **Connections:** Lasers, loopback hardware all connected by hand



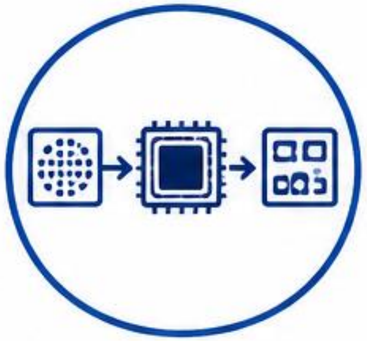
INSERTION 4

RESULT: Time-consuming, labor-intensive, and difficult to scale for high-volume production.

Module test solutions – High Density



Summary



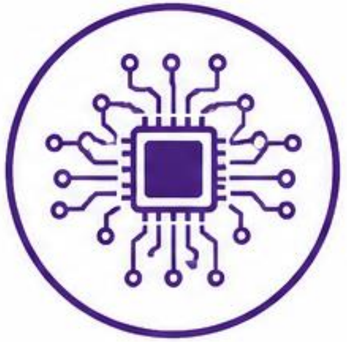
END-TO-END SCALABLE PLATFORM

- Wafer → Chip/Die → Module seamless continuity
- One architecture across the entire flow
- Future-ready and adaptable for next-gen speeds



MAXIMUM THROUGHPUT AND YIELD

- High UPH at every stage
- Advanced alignment, handling, and sorting
- Active control and thermal management for stability and uniformity



HIGH CHANNEL DENSITY AND INTEGRATION

- Hundreds of optical and electrical channels
- Parallel test with 224G+ electrical and optical
- Integrated instrumentation, optics, motion, and automation



BUILT FOR PRODUCTION

- Production automation end-to-end
- Consistent, repeatable, and reliable results
- Lower cost of test and higher first-pass yield


semi
SEMICON TAIWAN
Thank you
TRANSFORM
TOMORROW