How COUPE Redefines AI Interconnects

Aug 31, 2026

TRANSFORM
TOMORROW

Outline

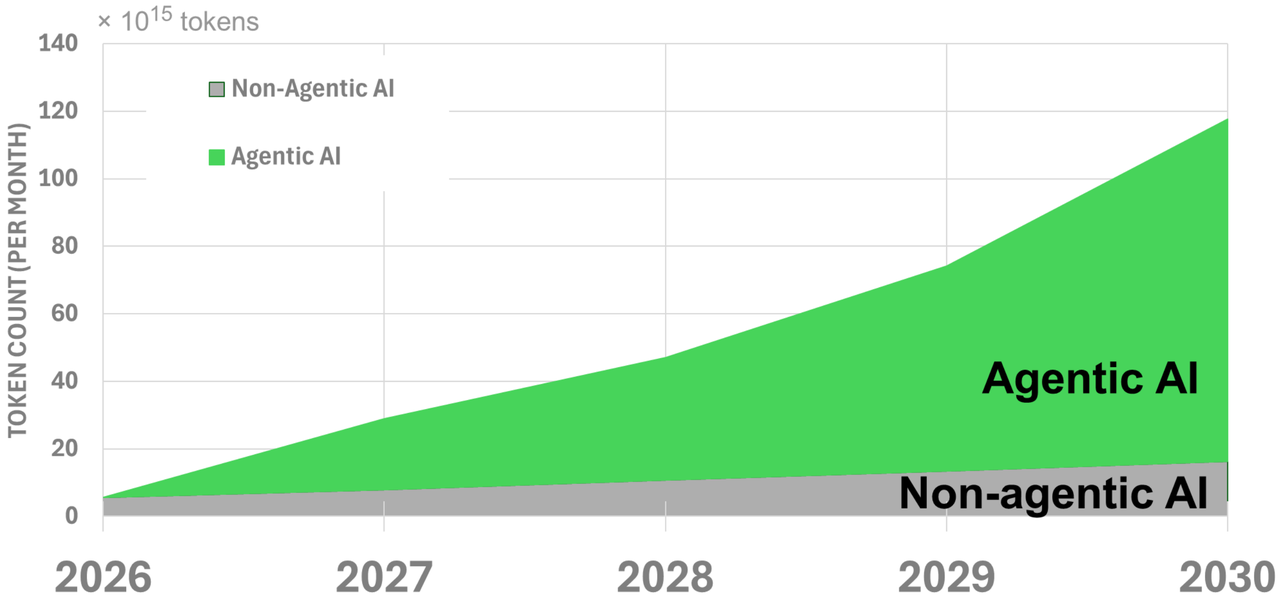
1. Scaling for AI Growth
2. What is COUPE?
3. COUPE’s Performance and next steps
4. Conclusions

Scaling for AI Growth



AI Token growth accelerating computing demand

- According to Goldman Sachs, driven by the rise of agentic AI, global AI token usage is projected to surge 24x by 2030, reaching 120 quadrillion tokens.
- To support this soaring demand, optical transmission performance is critical.



Data: Goldman Sachs

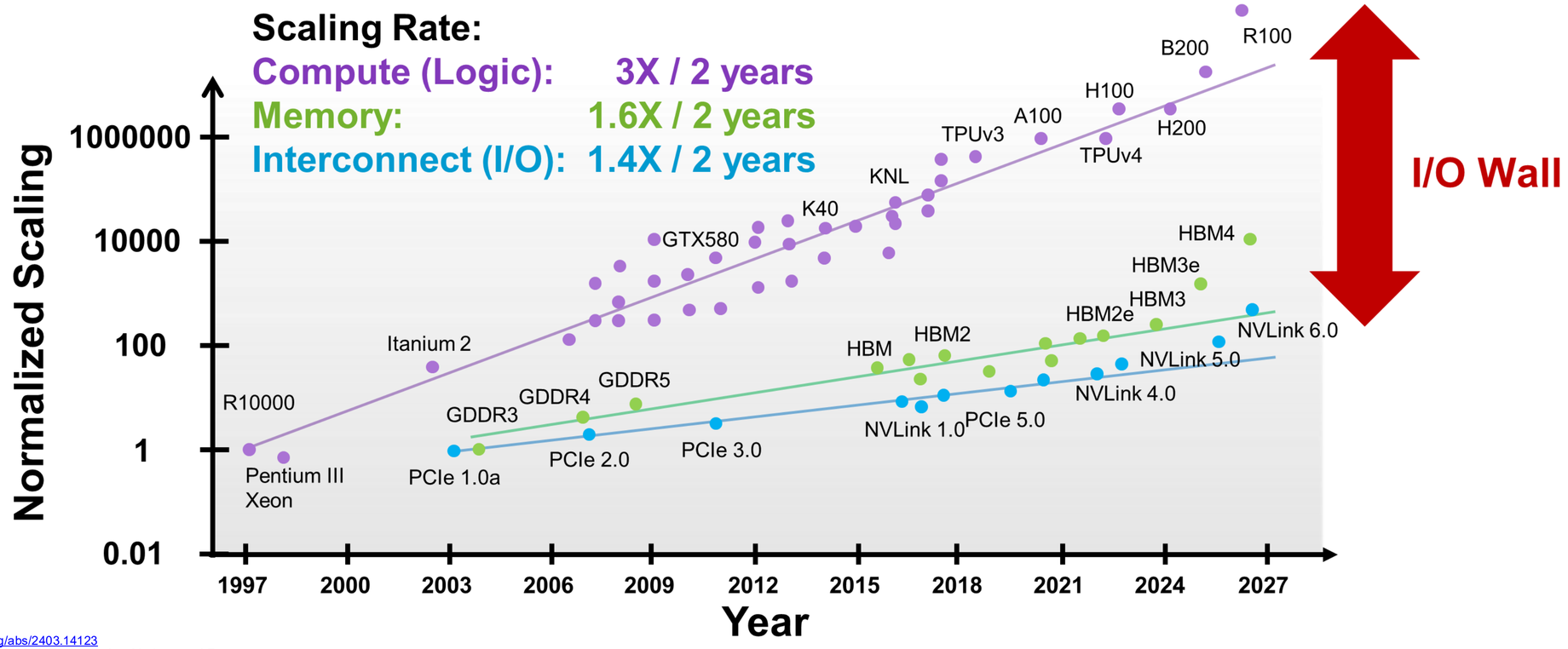
A 24x increase mainly driven by agentic AI
2026 - 2030

Source: AI Agents Forecast to Boost Tech Cash Flow as Usage Soars (Goldman Sachs Research): https://www.goldmansachs.com/insights/articles/ai-agents-forecast-to-boost-tech-cash-flow-as-usage-soars

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AI Bottleneck: I/O Wall

- I/O Wall:
  - AI compute power (Logic) surges at 3X every 2 years, But I/O bandwidth scales at only 1.4X.
  - How to increase I/O transmission performance is the key.



- Source: AI and Memory Wall, Amir Gholami et. al, https://arxiv.org/abs/2403.14123
- IDTechEx, Silicon Photonics and Photonic Integrated Circuits 2026-2036: Technologies, Markets, and Forecasts: https://www.idtechex.com/en/research-report/silicon-photonics-and-photonic-integrated-circuits/1151
- Nvidia Datasheet: (H200, B200): https://www.nvidia.com/en-us/data-center/h200/; https://www.nvidia.com/en-us/data-center/hgx/
- NVIDIA GTC 2026 Keynote, https://www.nvidia.com/gtc/keynote/

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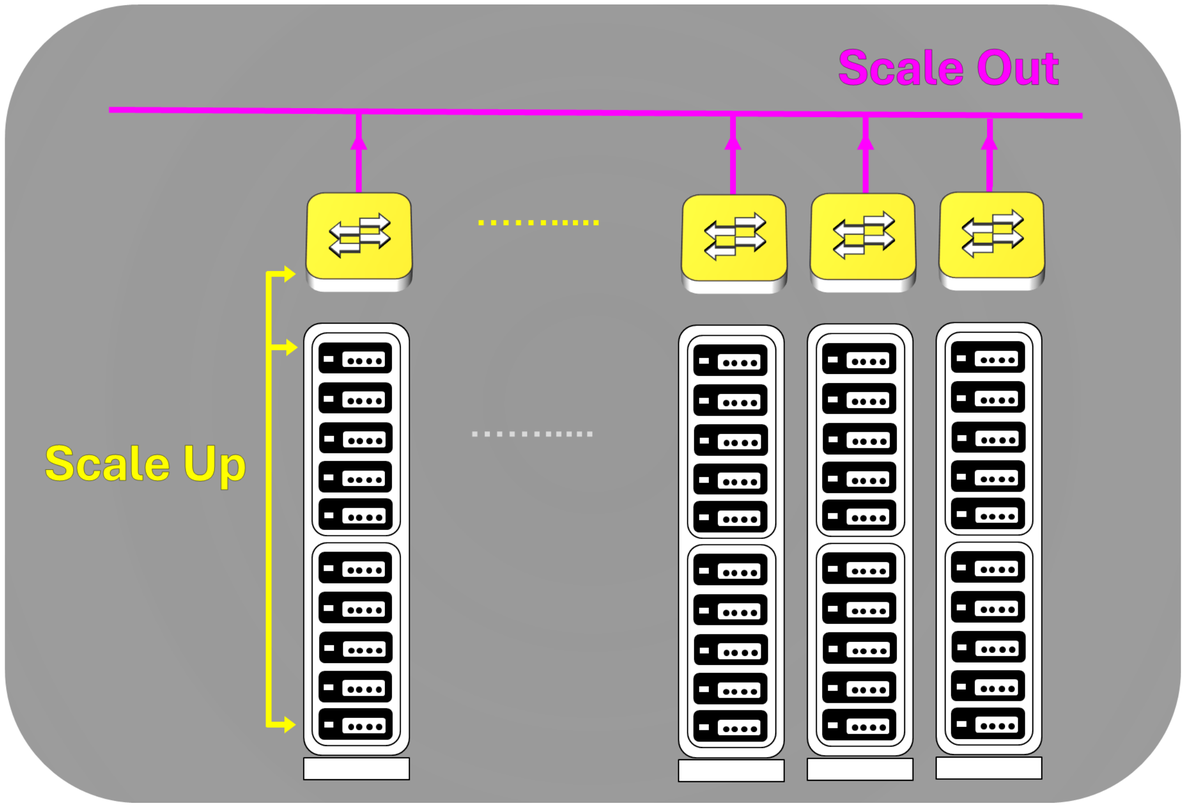
Optical Interconnect for Scale out and Scale up

- Traditional copper is constrained to short distances under high-frequency operation.
- By using optical transmission, the signal reach can be extended, which enables the scale-up and scale-out application.

Scale Up

Optical

Cu



Scale Out

CPO

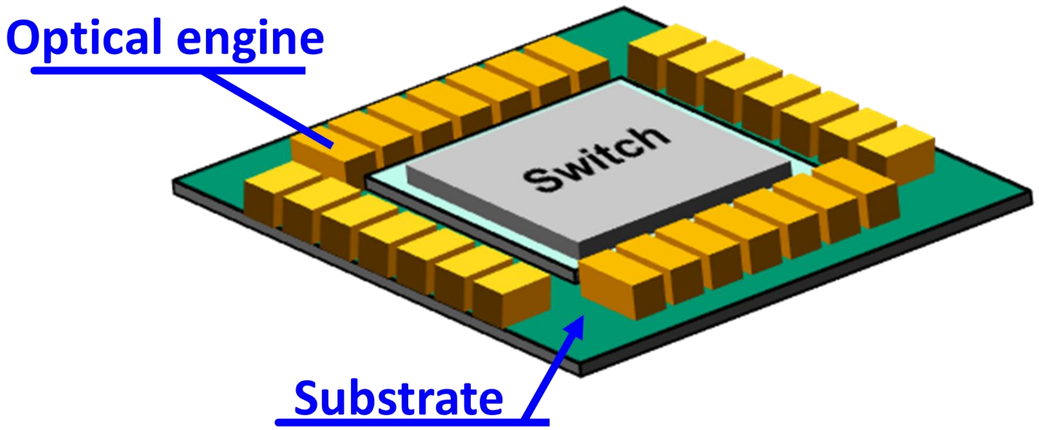
Pluggable

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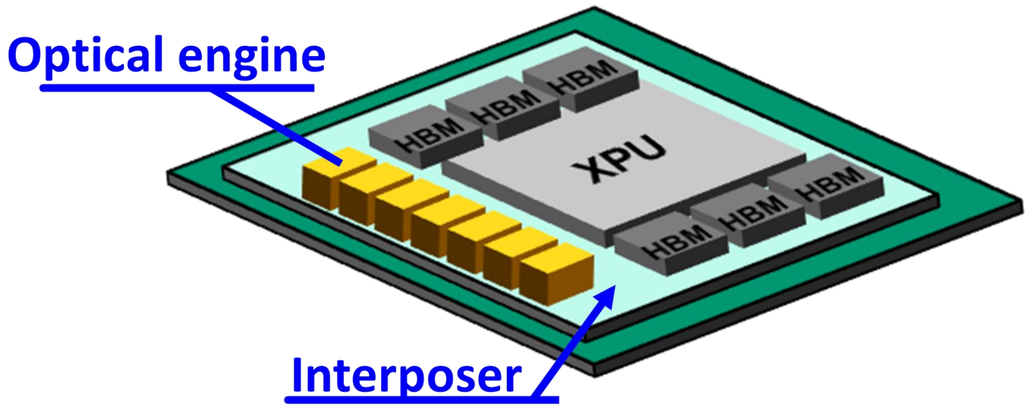
CPO-MCM and CPO-OOI

- **CPO-MCM**: Adopts a Multi-Chip Module (MCM) approach, integrating optical engines on the substrate.
- **CPO-OOI**: Directly integrates the optical engine onto the XPU's interposer

CPO-MCM
for Switch



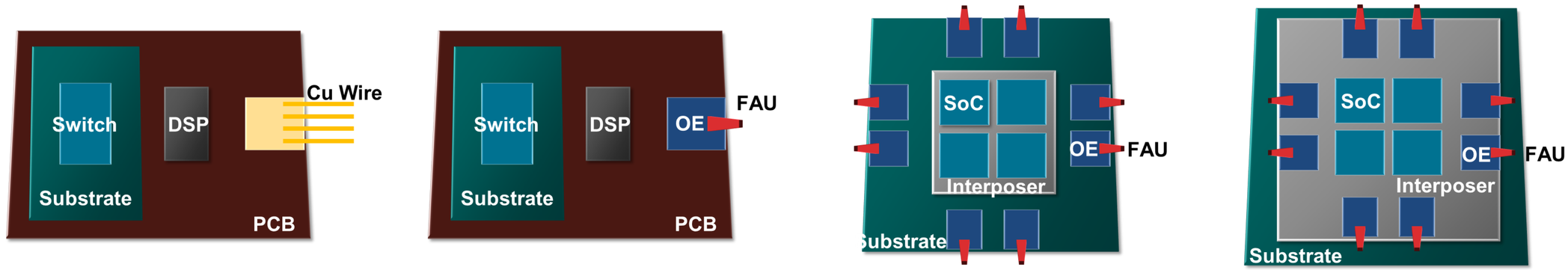
CPO-OOI
for XPU optical I/O



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From Copper to CPO

- CPO and OOI(Optical on Interposer) delivers a 4x~10x boost in power efficiency and a 10x~20x reduction in latency compared to Cu.
- A highly integrated, low-loss Optical Engine is the key.

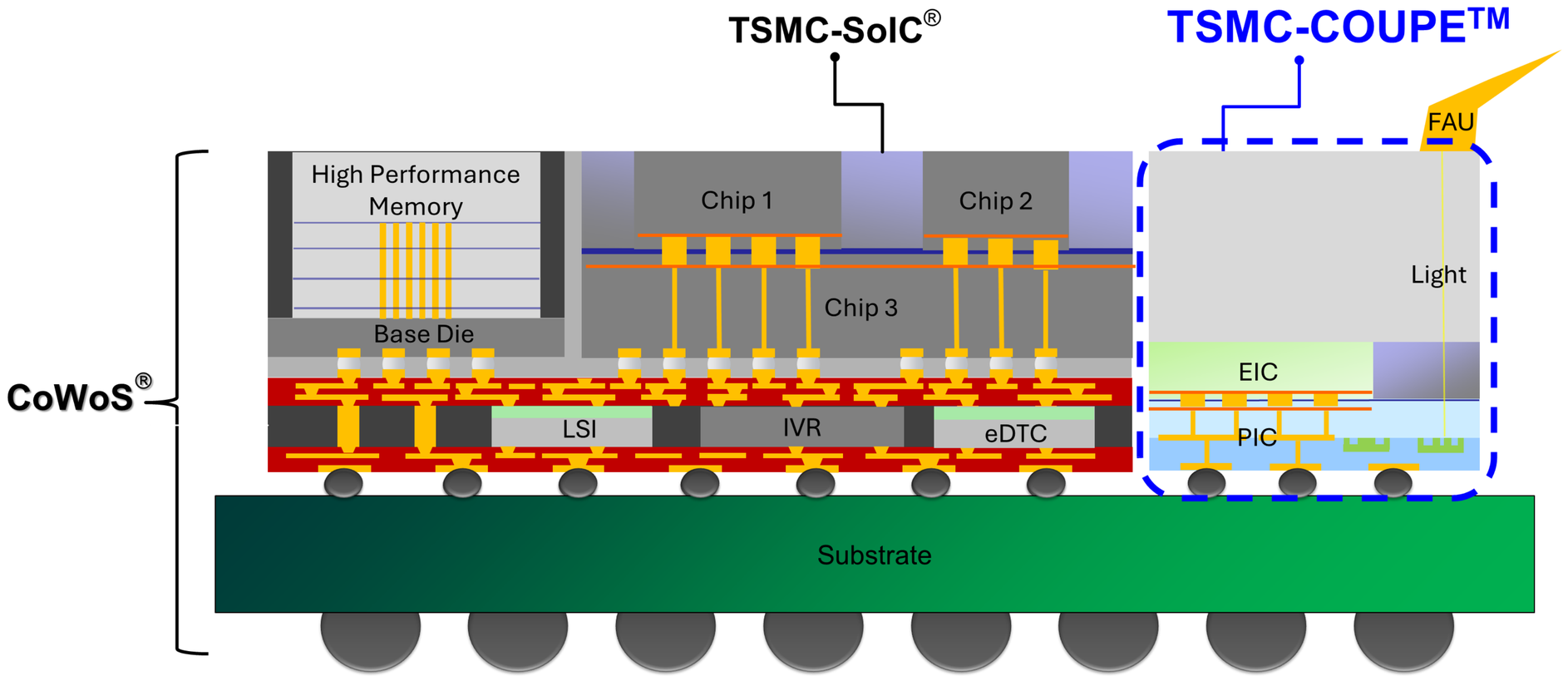


	Cu Wire	Pluggable Optics	Co-Packaged Optics (CPO)	Optics on Interposer (OOI)
Energy Efficiency	1X	2X	4X	10X
Latency	1X	1X	<0.1X	<0.05X

Source: TSMC 3DFabric® Advanced Packaging and 3D Silicon Stacking, Mii YJ, 2026 North America Technology Symposium

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TSMC Integrated Platform for AI



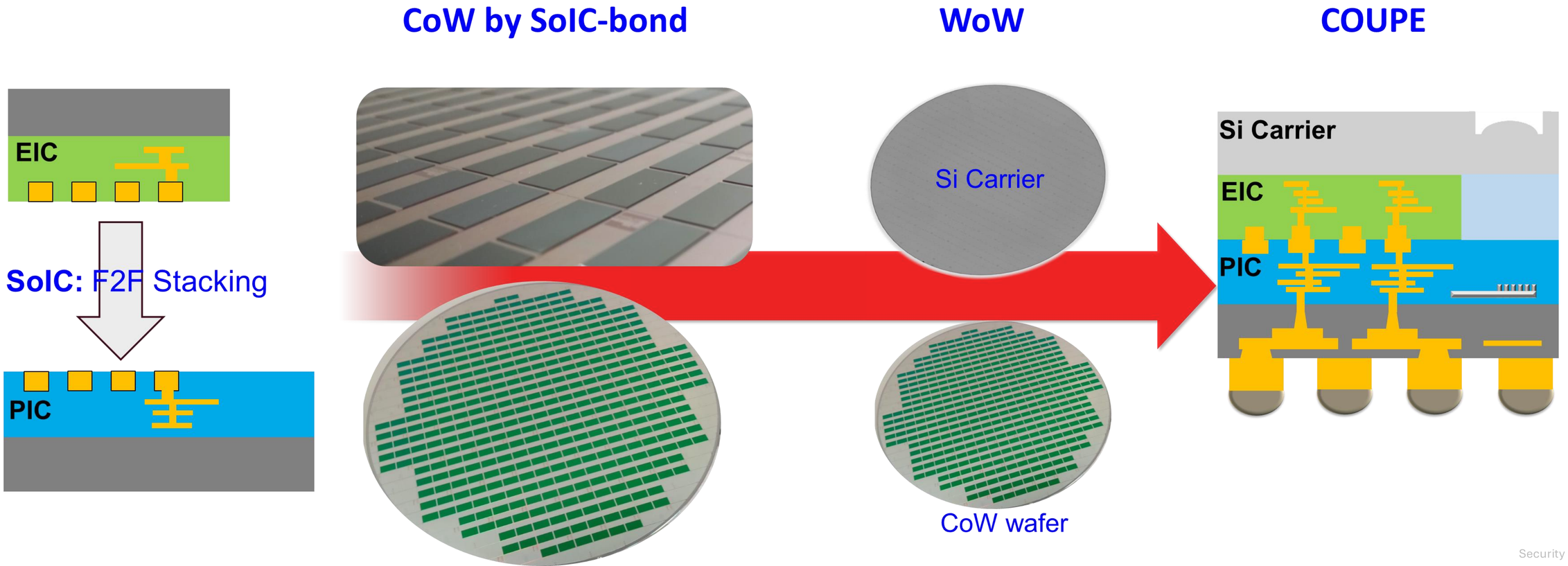
Source: TSMC 3DFabric® Advanced Packaging and 3D Silicon Stacking, Mii YJ, 2026 North America Technology Symposium

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What is COUPE?

COmpact Universal Photonic Engine (COUPE)

- COUPE leverages SoIC-bond stacking to integrate advanced logic (EIC) and PIC.
- Featuring a proprietary optical path design and components, such as Si uLens and Cu BMR (Backside Metal Reflectors).

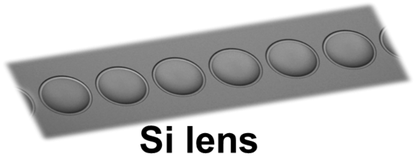


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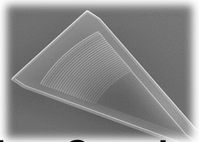
COUPE Key Features

- COUPE-GC (Grating Coupling): Si ulens, Cu BMR, and Si/SiN GC.
- COUPE-EC (Edge Coupling): EC facet and SiN tip.

GC Key Features



Si lens

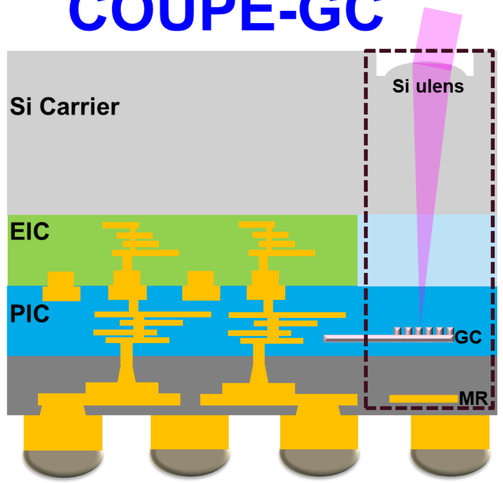


Grating Coupler (GC)

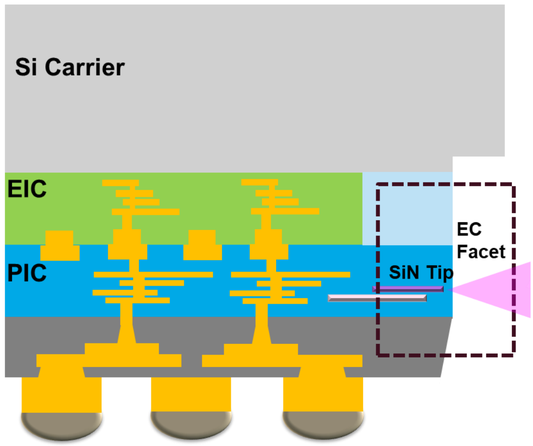


Metal Reflector (MR)

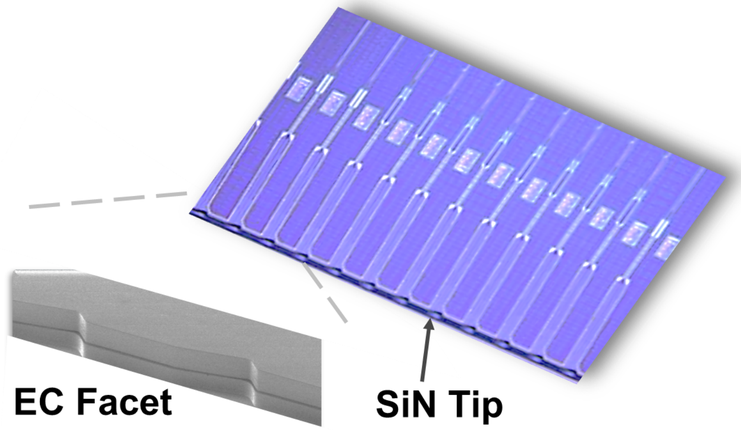
COUPE-GC



COUPE-EC

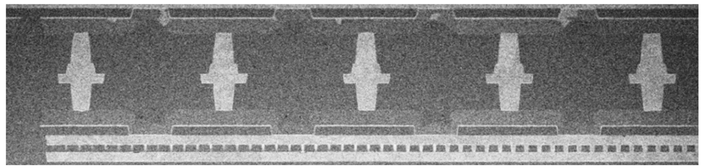


EC Key Features

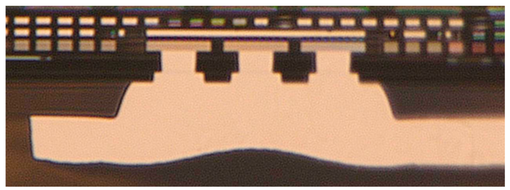


Common Features

SoIC-bond



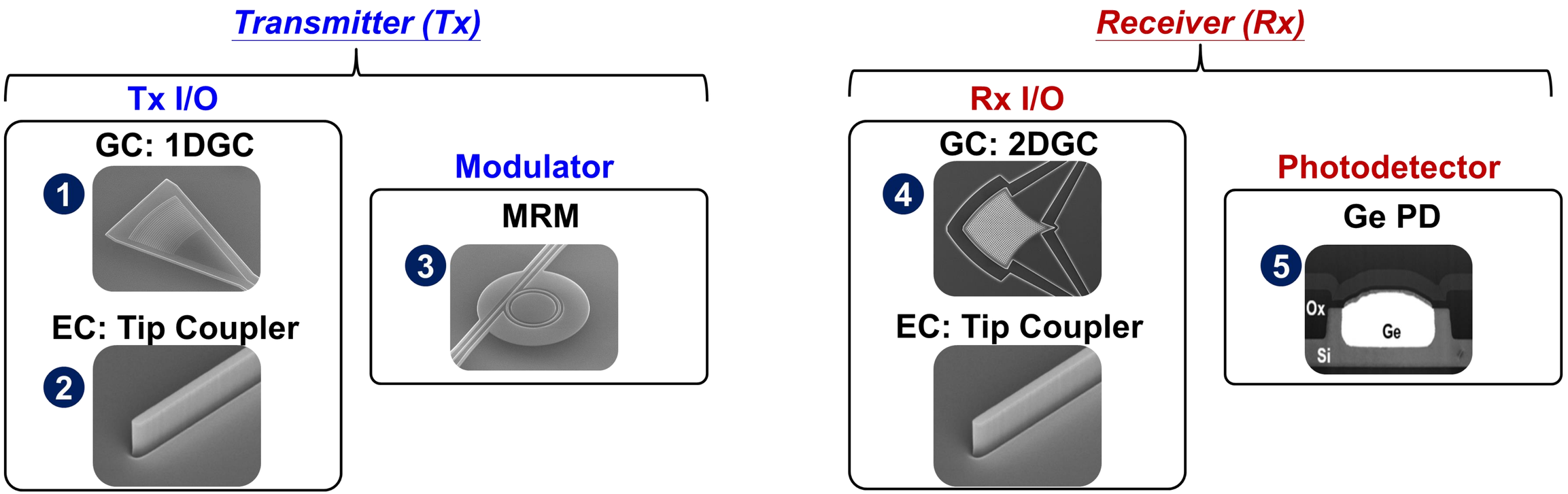
TDV



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COUPE Critical Devices in Tx/Rx

- Transmitter (Tx): 1DGC, Tip Coupler, and Micro-Ring Modulator (MRM).
- Receiver (Rx): 2DGC, Tip Coupler, and Ge Photodetector (PD).

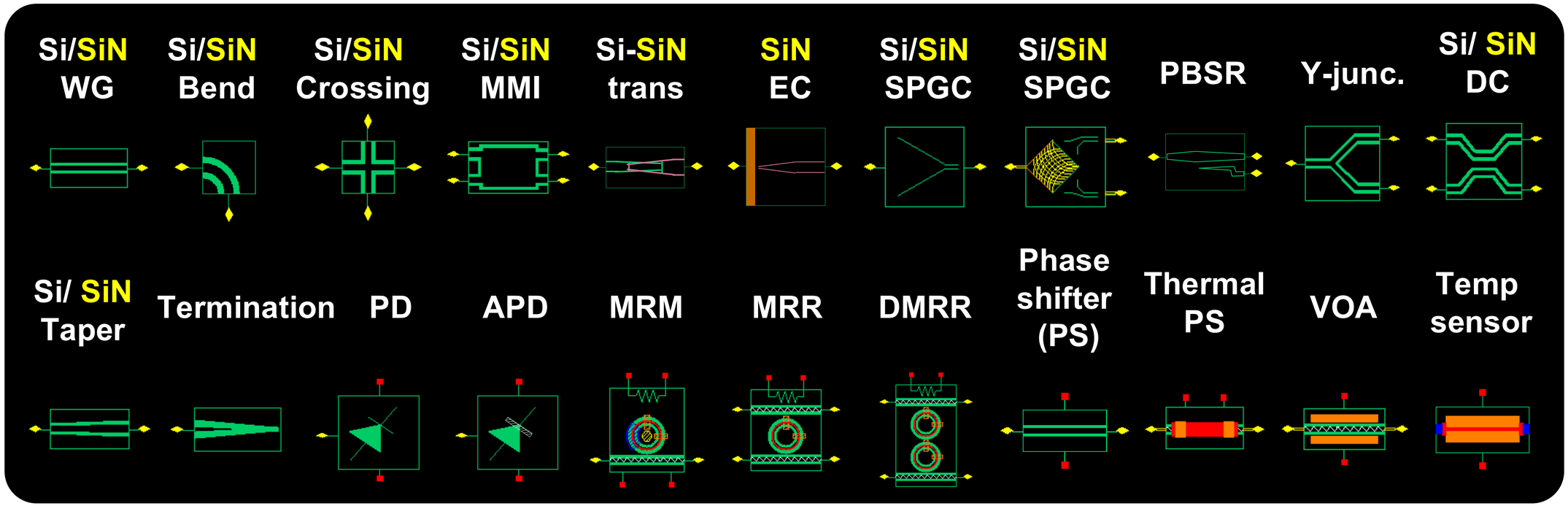


Source: Advancement in Silicon Photonics: From Research to Real-World Application, K.C. Hsu, 2024 SEMICON

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TSMC Process Design Kit (PDK) for Photonics Devices

- TSMC provides a complete device PDK to help customers design SiPh and shorten their time-to-market.

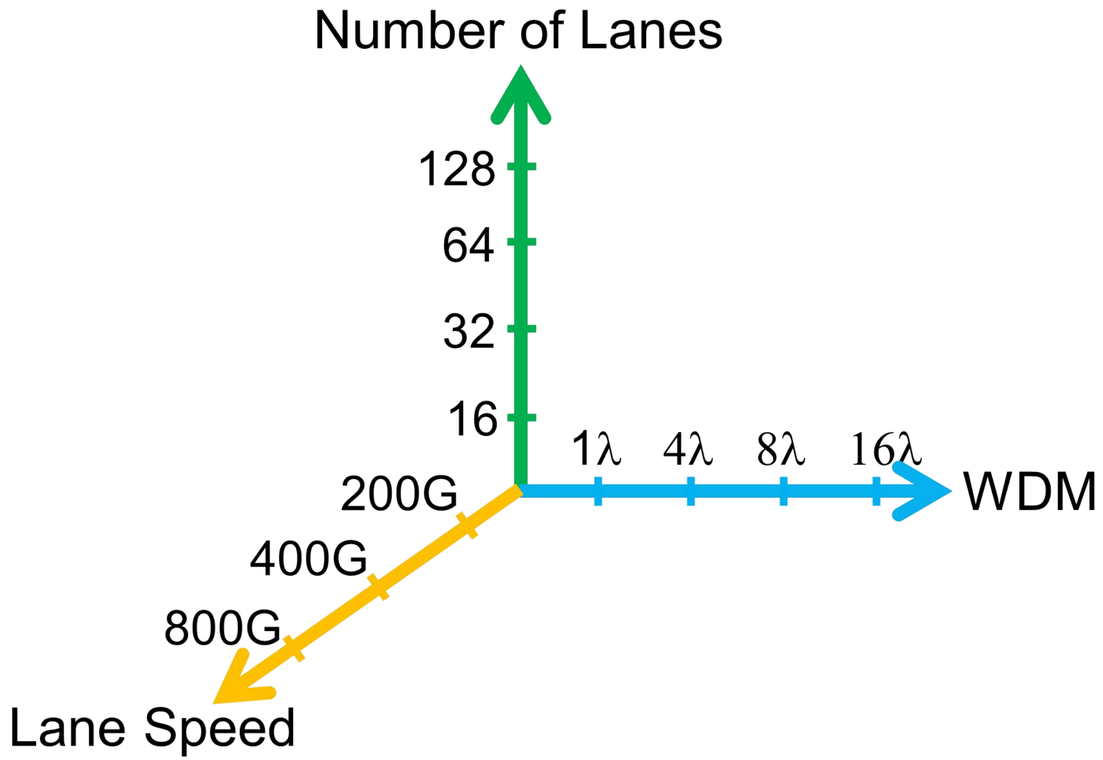


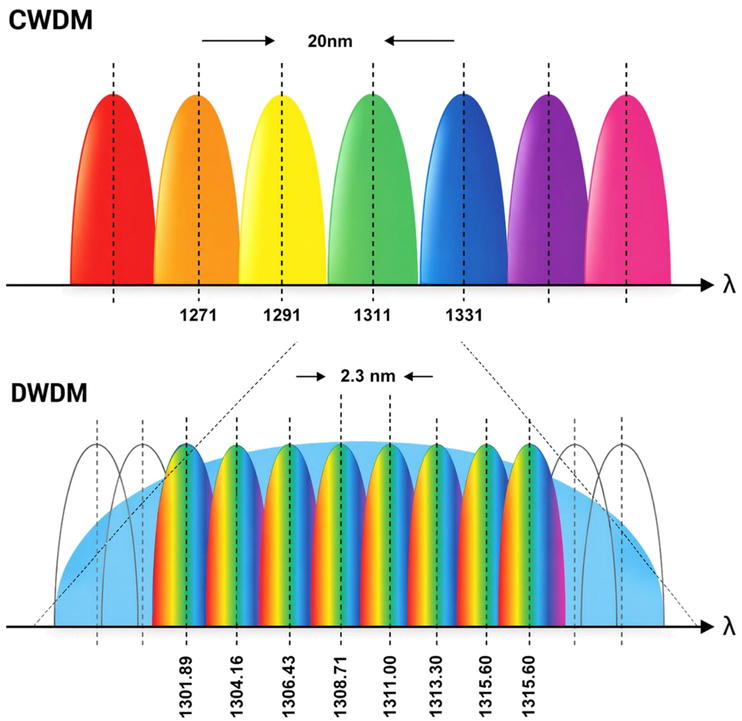
Source: High Volume Manufacturing of Scalable Silicon Photonics, S.F. Huang, 2025 SEMICON

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How COUPE Scales Bandwidth?

- Bandwidth per COUPE = (Lane Speed) x (Number of Lanes) x (WDM)

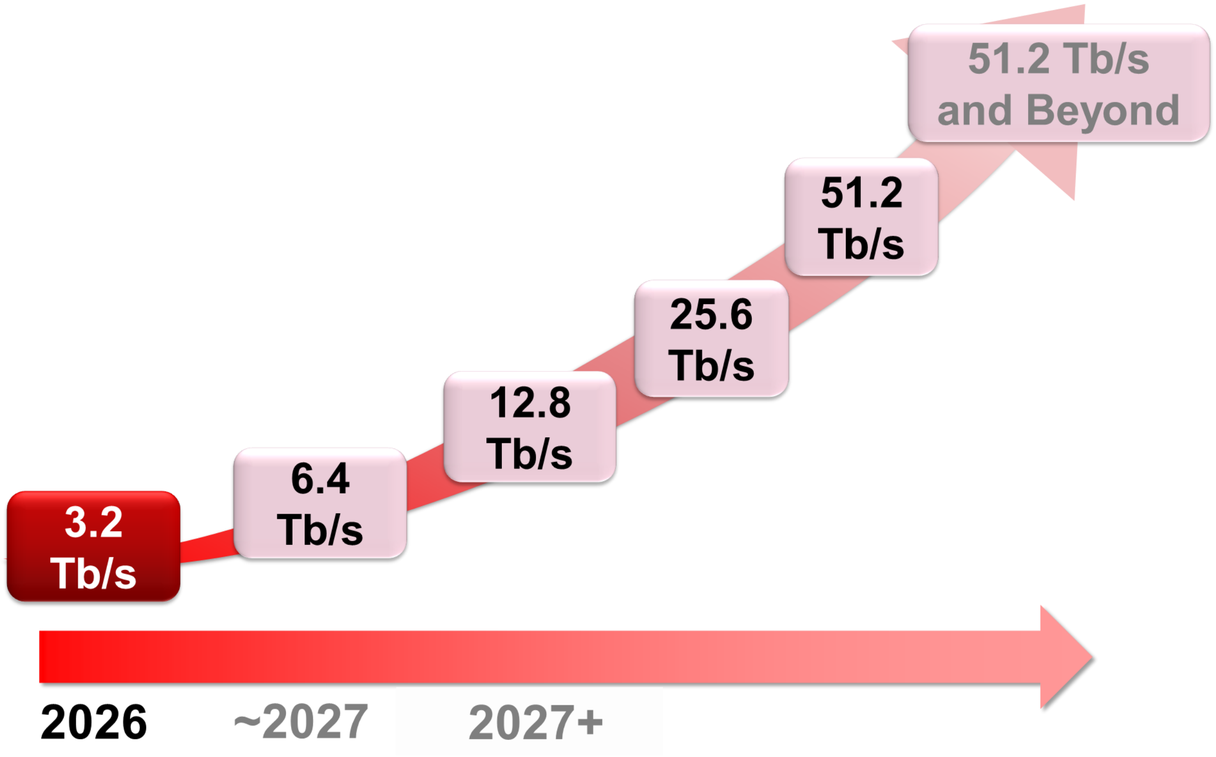




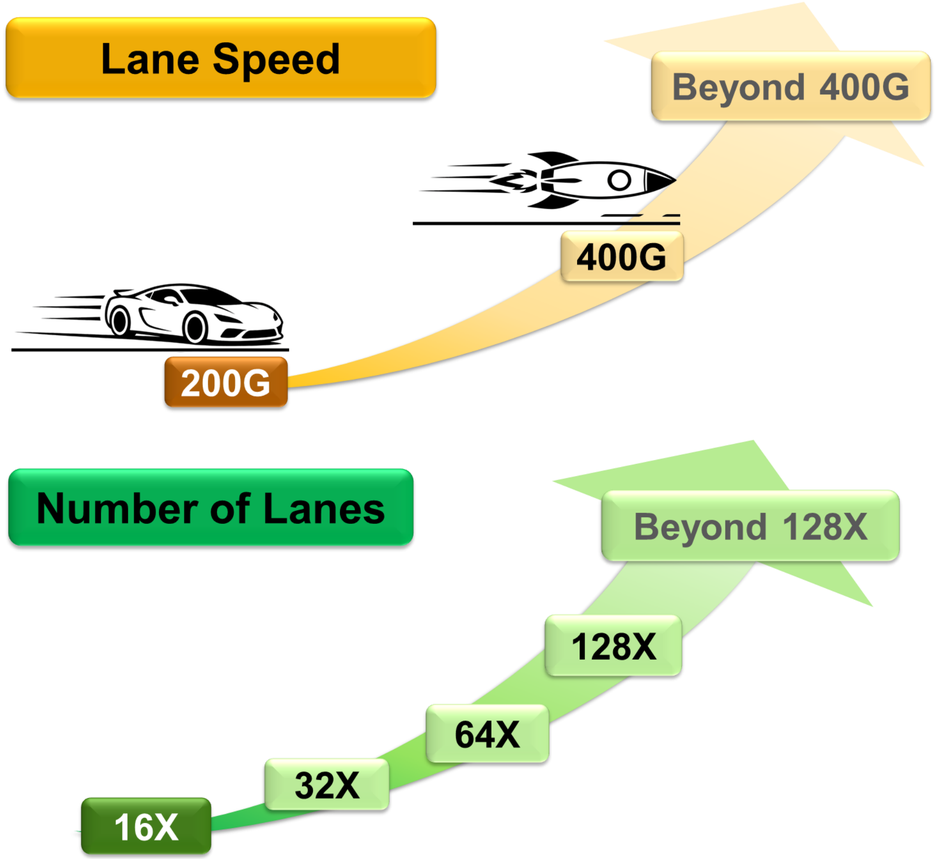
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COUPE Bandwidth Scaling: Fast and Narrow

- **Bandwidth per COUPE:**



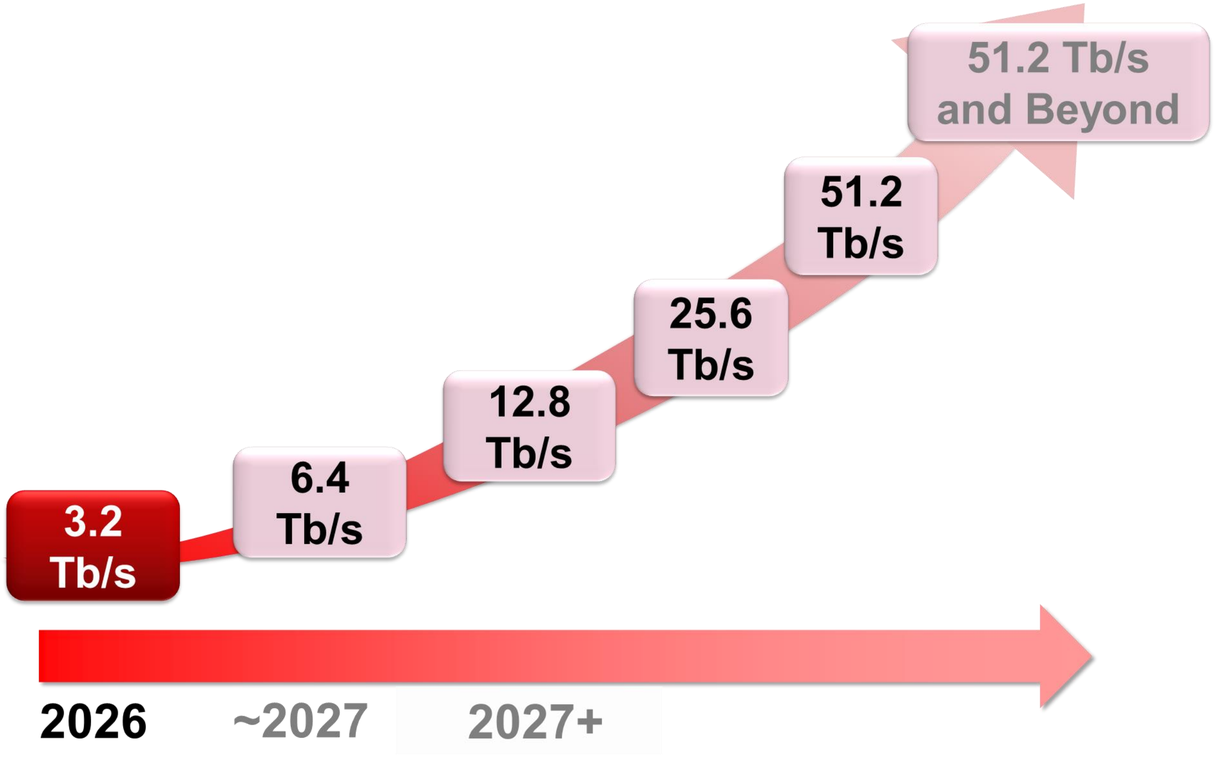
- **Scaling Strategies:**



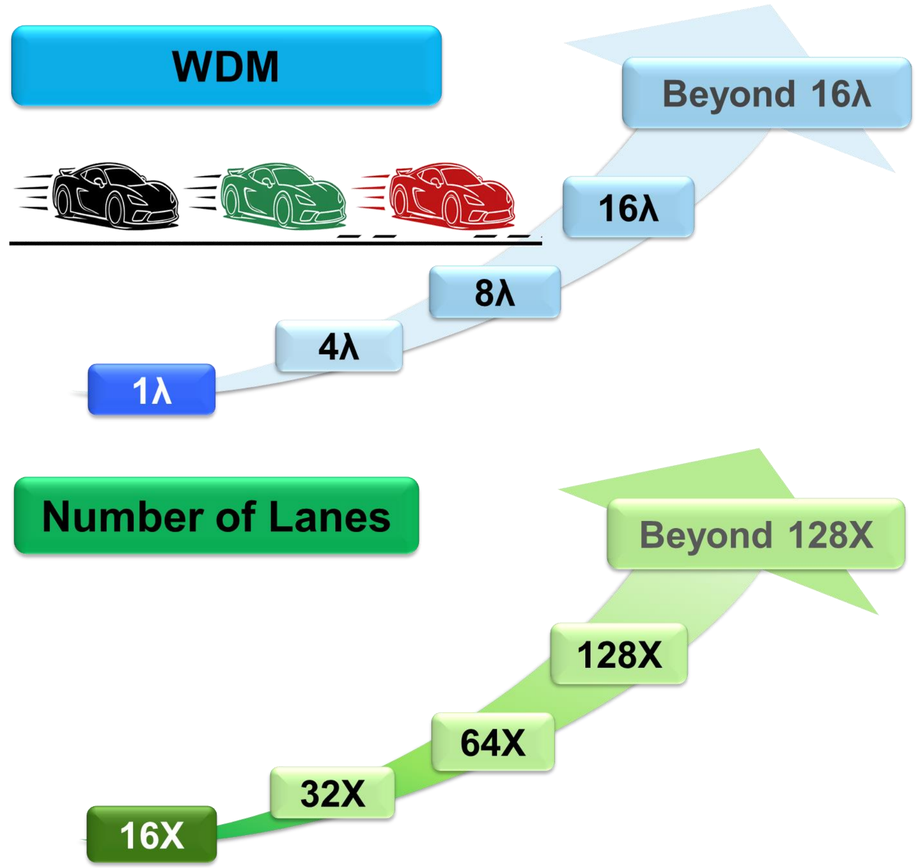
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COUPE Bandwidth Scaling: Slow and Wide

- **Bandwidth per COUPE:**

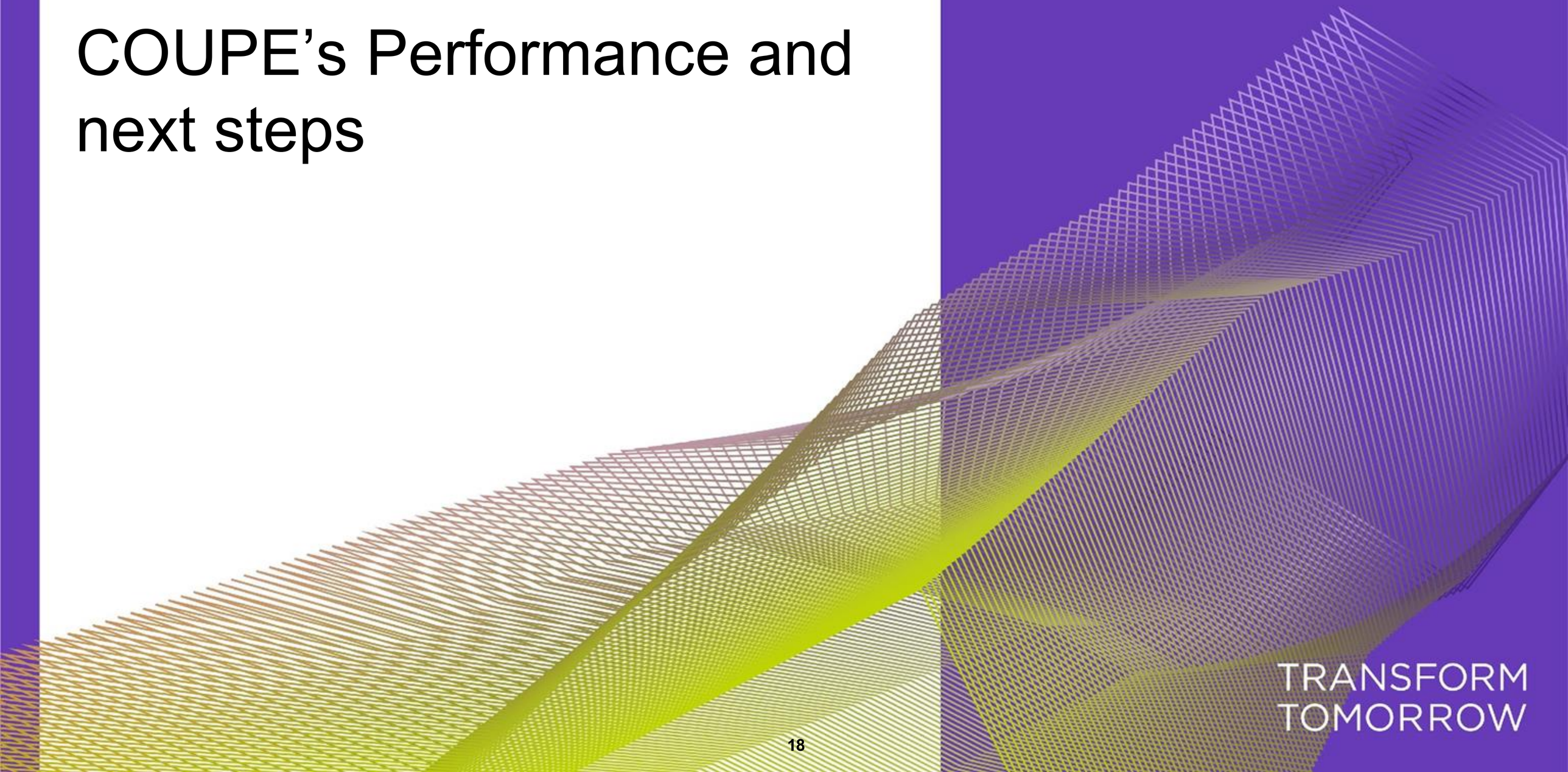


- **Scaling Strategies:**



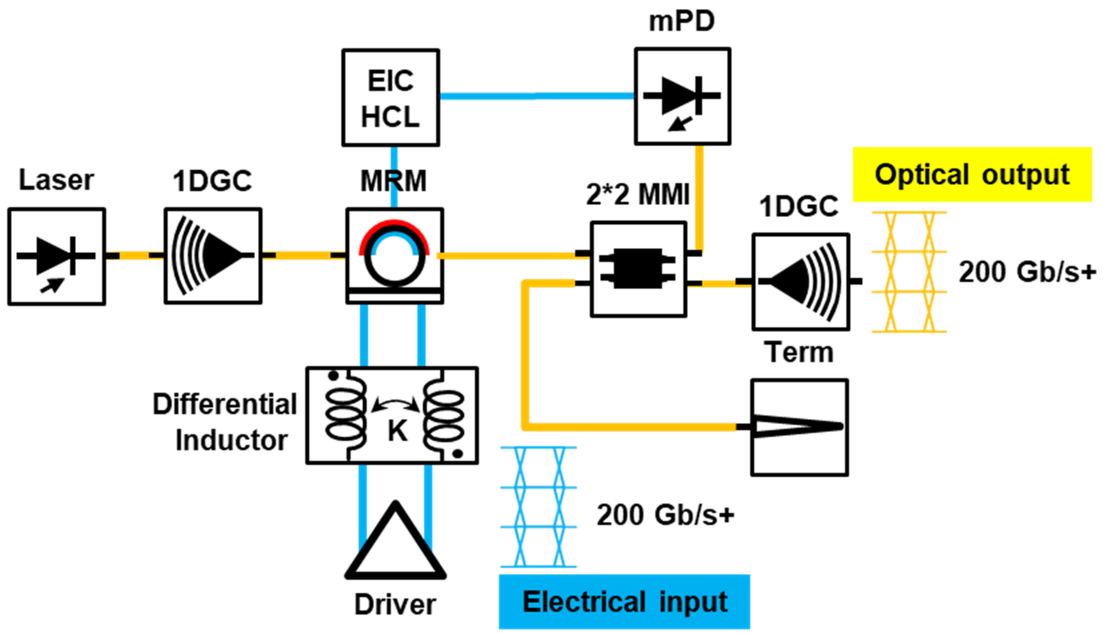
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COUPE’s Performance and next steps



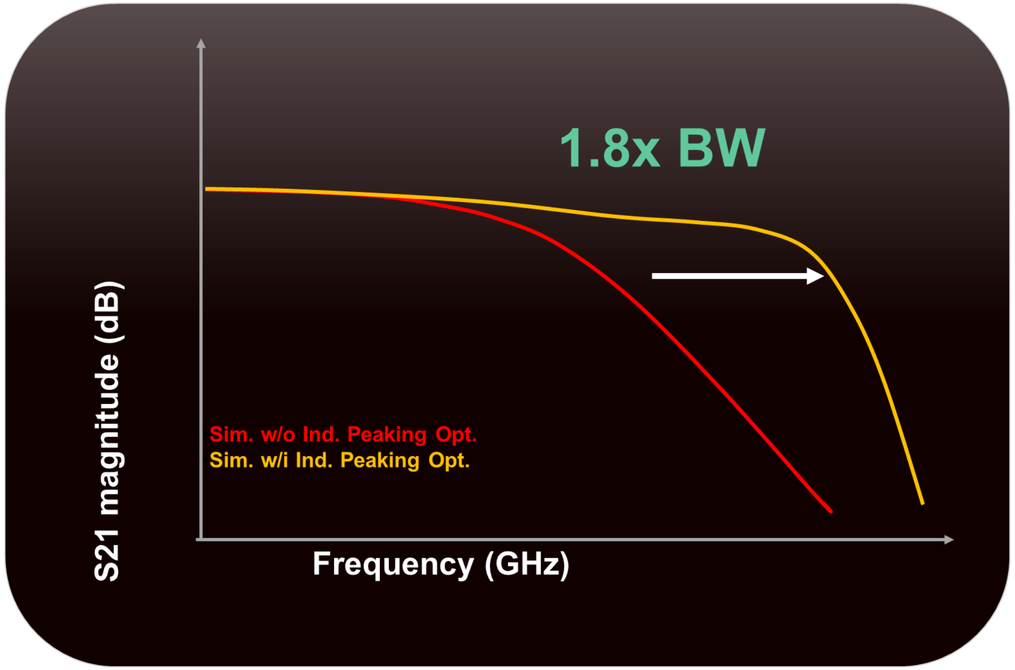
Boosting MRM Bandwidth

- Optimize inductive peaking, MRM and EIC driver optimization to improve MRM bandwidth by ~1.8x from simulation.



COUPE architecture

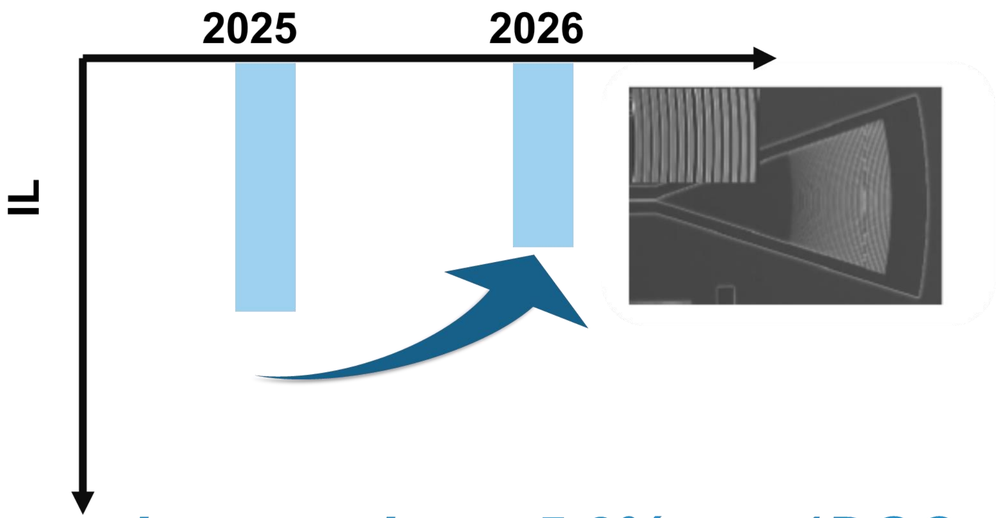
Inductive peaking optimization with MRM and EIC driver optimization



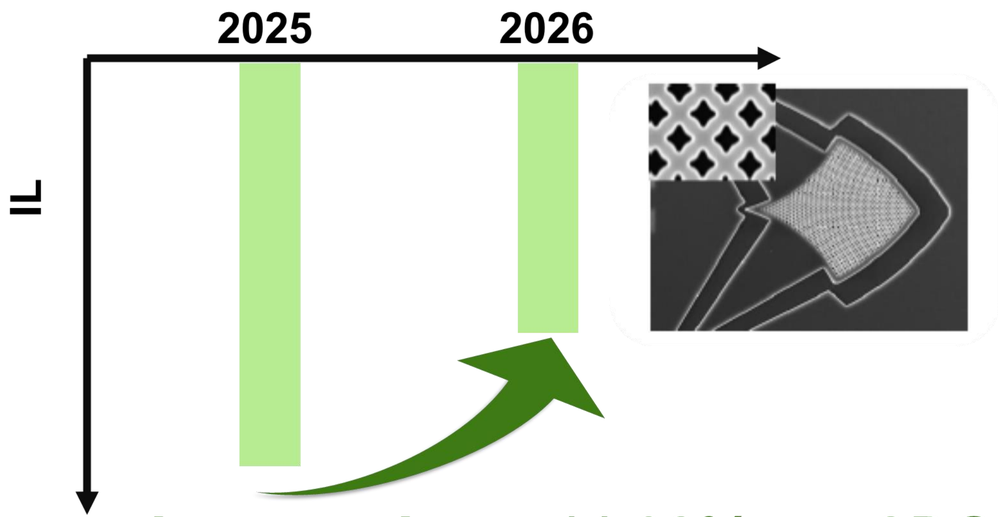
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GC Efficiency Improvement

- From 2025 to 2026, COUPE 1DGC and 2DGC insertion losses can be improved by 5.3% and 11%, respectively.



Improve Loss 5.3% per 1DGC

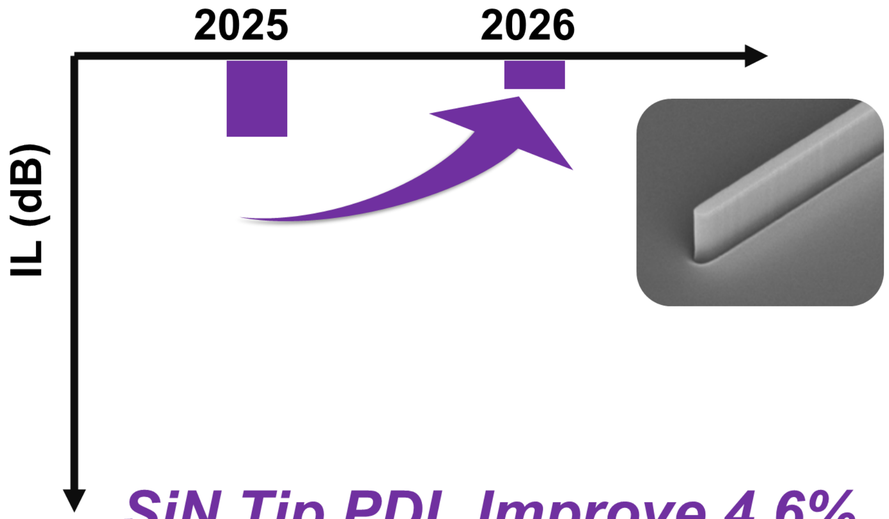


Improve Loss 11.03% per 2DGC

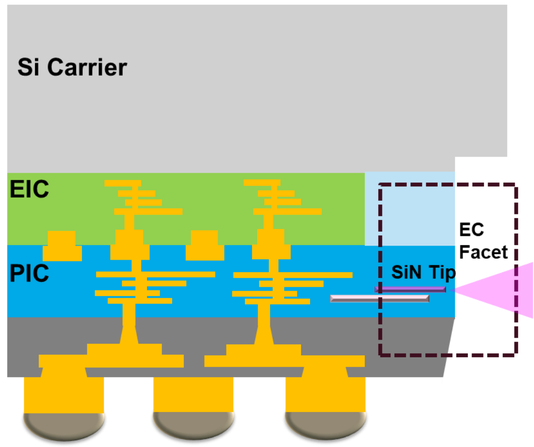
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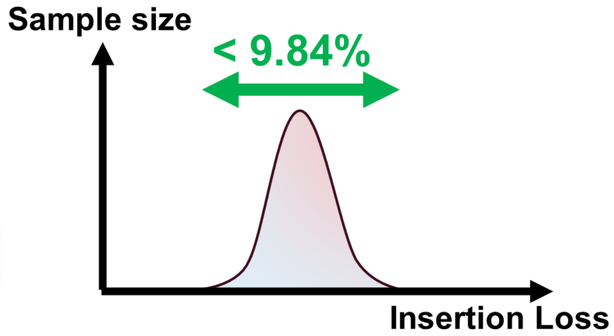
EC Efficiency Improvement

- From 2025 to 2026, improve SiN tip Polarization Dependent Loss (PDL) by 4.6%.
- SiN tip coupler loss within wafer range can reach < 9.8%.



SiN Tip PDL Improve 4.6%



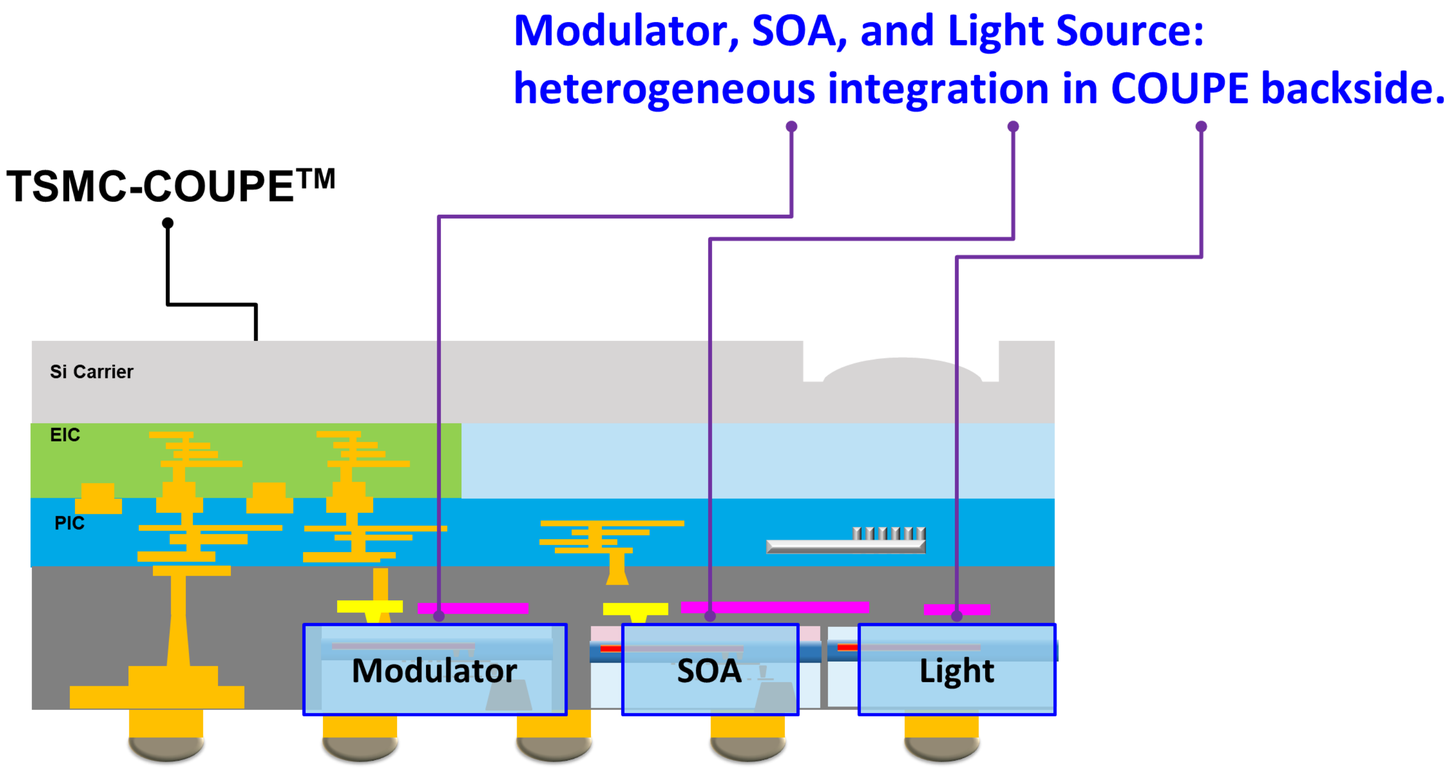


SiN Tip Coupler Loss Range < 9.8%
Within wafer

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Extending COUPE Heterogeneous Integration

- To improve the performance of COUPE, further heterogeneous integration of the modulator, SOA, and light source into the COUPE platform can be implemented.
- COUPE also functions as an optical interposer.



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Summary

- Driven by the bandwidth and power efficiency in AI and HPC, Optical I/O is a valuable option to pursue.
- Continue to improve COUPE platform performance to meet both CWDM and DWDM application.
- The integration of COUPE with CoWoS package for different applications will be realized through close collaboration between stakeholders or STCO (System and Technology Co-Optimization).

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