Advancing TFLN & InP Silicon Photonics Hybridization to Enable Next-Generation High-Speed Modulators.

Yannick LARVOR | Head of Photonics & Sensing Segment
SOITEC

Silicon Photonics Summit, Aug 31st, 2026

TRANSFORM TOMORROW

Agenda

01. Soitec introduction

02. Optical Interconnects market trends

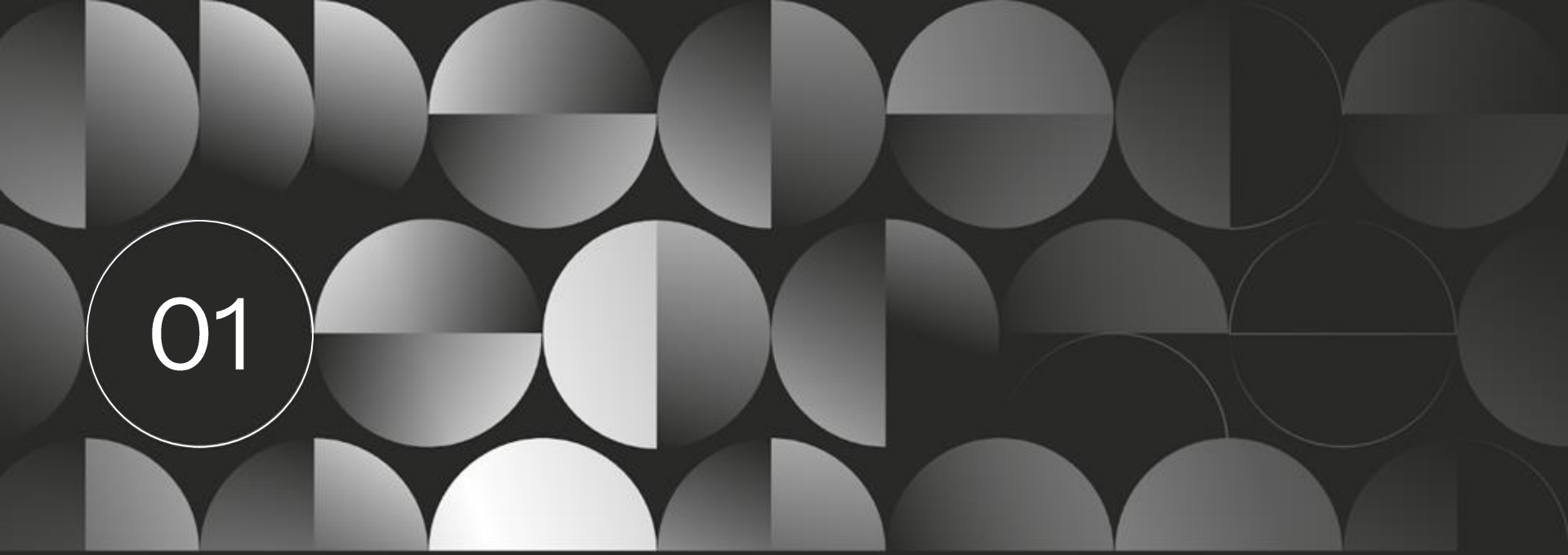
03. Photonics SOI: a universal SiPh host platform

04. Enhancing SiPh with heterogeneous integration

05. LNOI & InPOSi material platforms

06. Takeaways





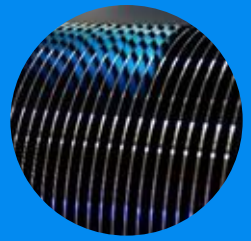
Soitec introduction

Soitec: a unique position in the value chain

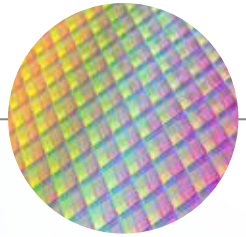


Bulk Materials

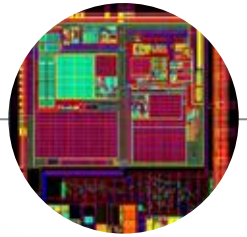
soitec



The leading supplier of Engineered Substrates



Foundries | Design | Fabless





Final Markets



Mobile Communications



Automotive & Industrial



Edge & Cloud AI

1992
Soitec is founded

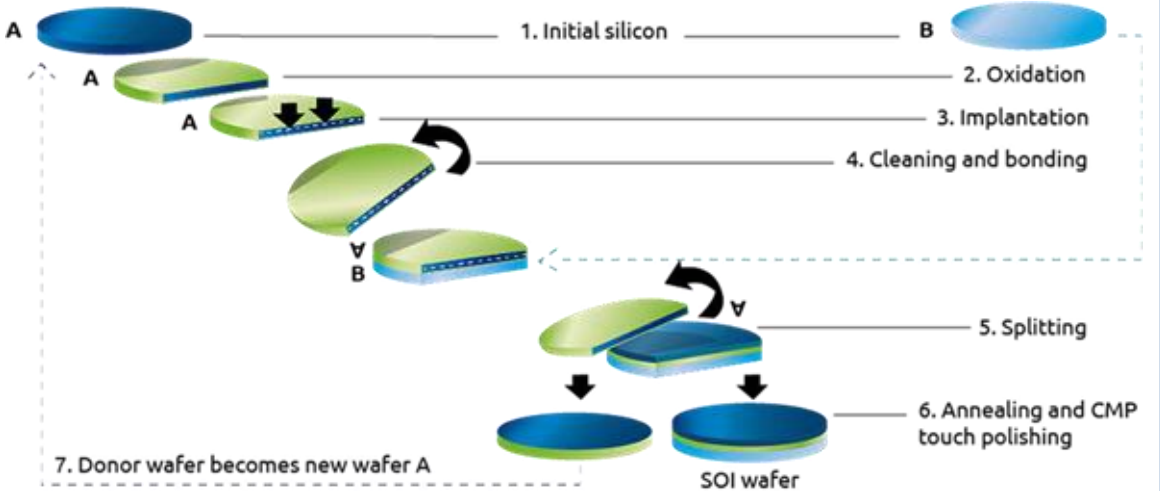
471
Patents in 2025

4 800
Active patents

~2 100
Employees

€592M
Revenue
(Fiscal year 2026)

Smart Cut™ and SOI substrates





Active layer



Functional/ insulator layer



Base wafer: mechanical support

Silicon or easy to handle & active

TECHNOLOGY

- Industrial manufacturability of SOI – high yield
- Drastic improvement in uniformity & quality
- Re-use of donor wafer increases cost efficiency
- Flexibility of material integration

Industrial footprint

France & Singapore operations



150mm
200mm
300mm



30 years of high-volume manufacturing experience

SOITEC BERNIN
FRANCE

B1
SOI 200mm

B2
SOI 300mm

B3
LTOI/LNOI
150/200mm

B4
SmartSiC 150/200mm
SOI 300mm

200mm



SIMGUI (Partner)
CHINA

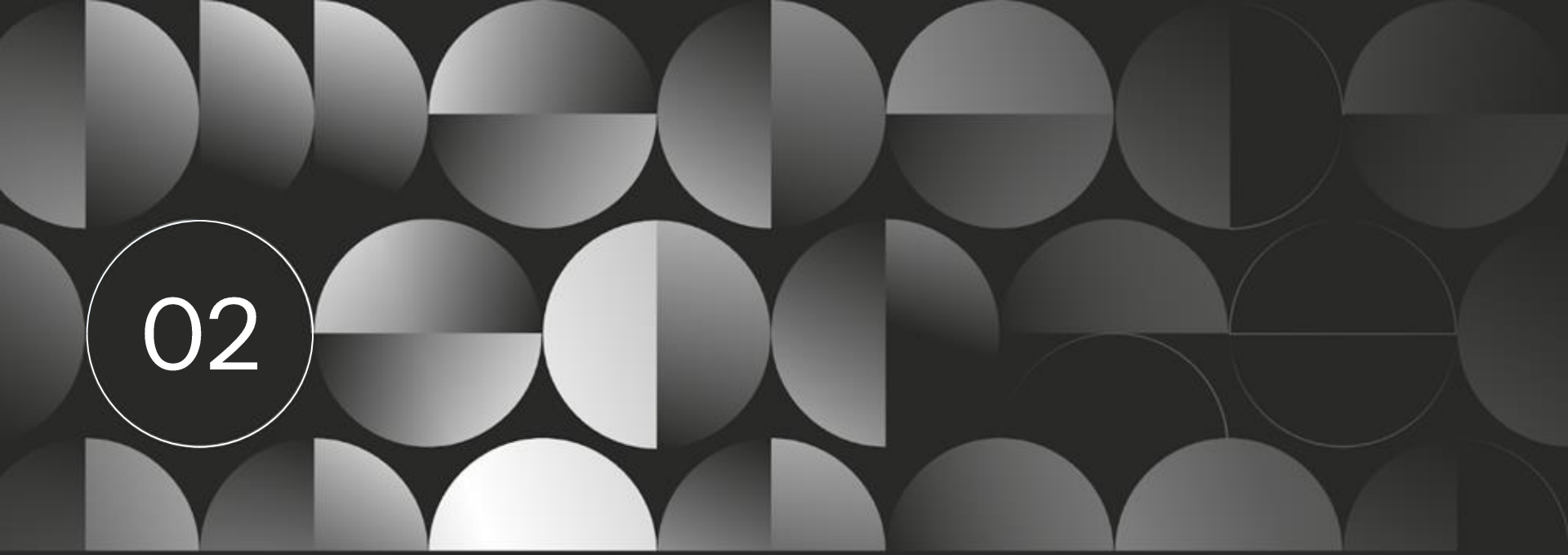
SOI 200mm

300mm



SOITEC PASIR RIS
SINGAPORE

PR1
SOI 300mm



Optical Interconnects market trends

AI Data Centers network are scaling through optics

RACK SCALE UP TODAY

100% Copper

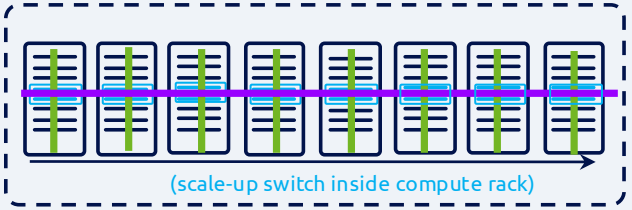


~10's XPU sharing "unified memory" within rack

Copper good enough

ROW-SCALE SCALE UP 2027~2028

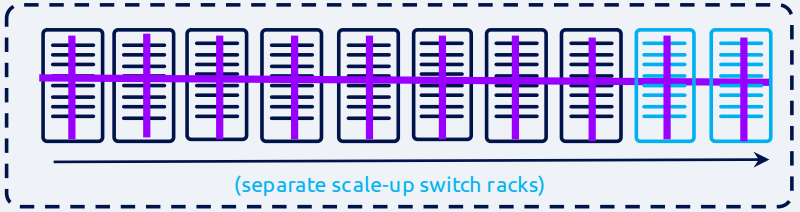
Hybrid Copper / Optics



~100's XPUs sharing "unified memory"
Copper in-rack, Optics across racks

ROW-SCALE SCALE UP from 2029 onwards

100% Optics



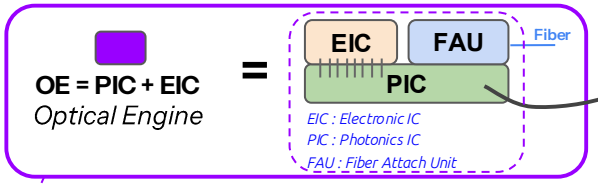
~1000 XPUs sharing "unified memory"
All Optics within rack and across racks

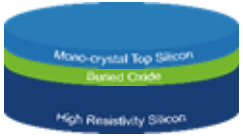
Optical interconnects provide multiple benefits:
Disaggregation, higher bitrate, better power efficiency (pJ/bit), better latency and interconnects density

Scale-out & Scale-across have already moved to 100% optics
2027 → Scale-up interconnects steadily moving to optics

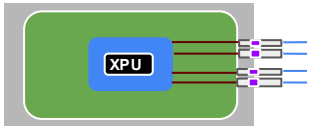
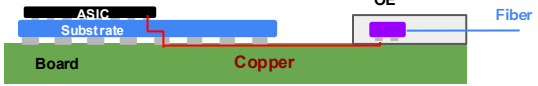
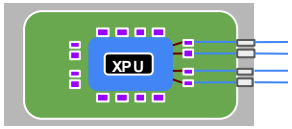
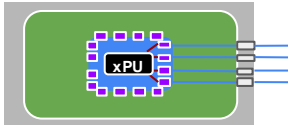
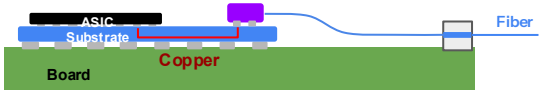
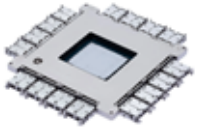
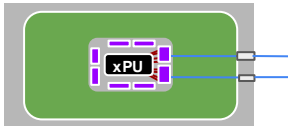
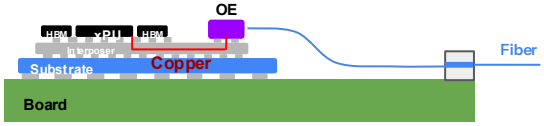
Optical interconnects use case mapping

Reduce copper length, improve pJ/bit budget and increase shoreline



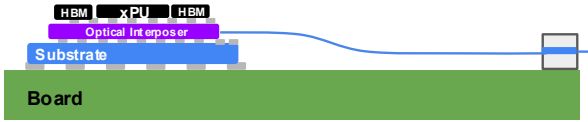


PIC based on Photon-SOI

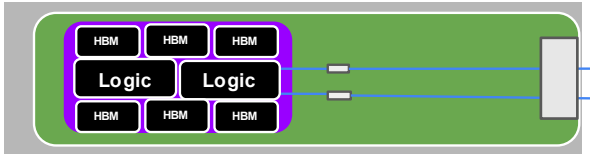
TOP VIEW	CROSS VIEW			
		**Pluggable Optics PO & LRO, LPO** *(OE inside a module)*		***Scale-out Scale-across Scale-up***
		**NPO (Near Package Optics)** *(OE on PCB)*		***Scale-up***
		**CPO (Co-Packaged Optics)** *(OE on Substrate)*		***Scale-out Scale-up***
		**Optical I/Os** *(OE on interposer)*		***Scale-up***

Photonics Interposer : the next opportunity

Use a package-scale active silicon photonics interposer to connect chiplets



(The PIC is the interposer)

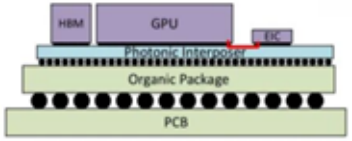


SiPh interposer identified system benefits

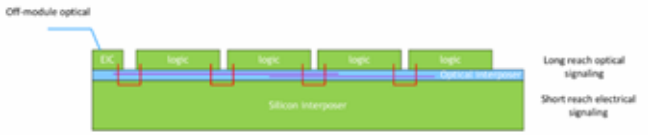
- Expanded shoreline to cope with ASIC IO bandwidth continuous increase
- Further reduction of latency and power consumption (3D integration).
- Disaggregation (e.g memory from logic chiplets)
- OCS for dynamic routing and reconfigurability between chiplets.



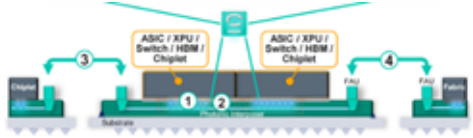
Source : Lightmatter Passage



Source : NVIDIA (ISSCC'26)



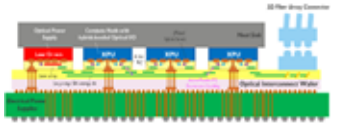
Source : NVIDIA (OIP'26)



Source : Marvell / Celestial AI



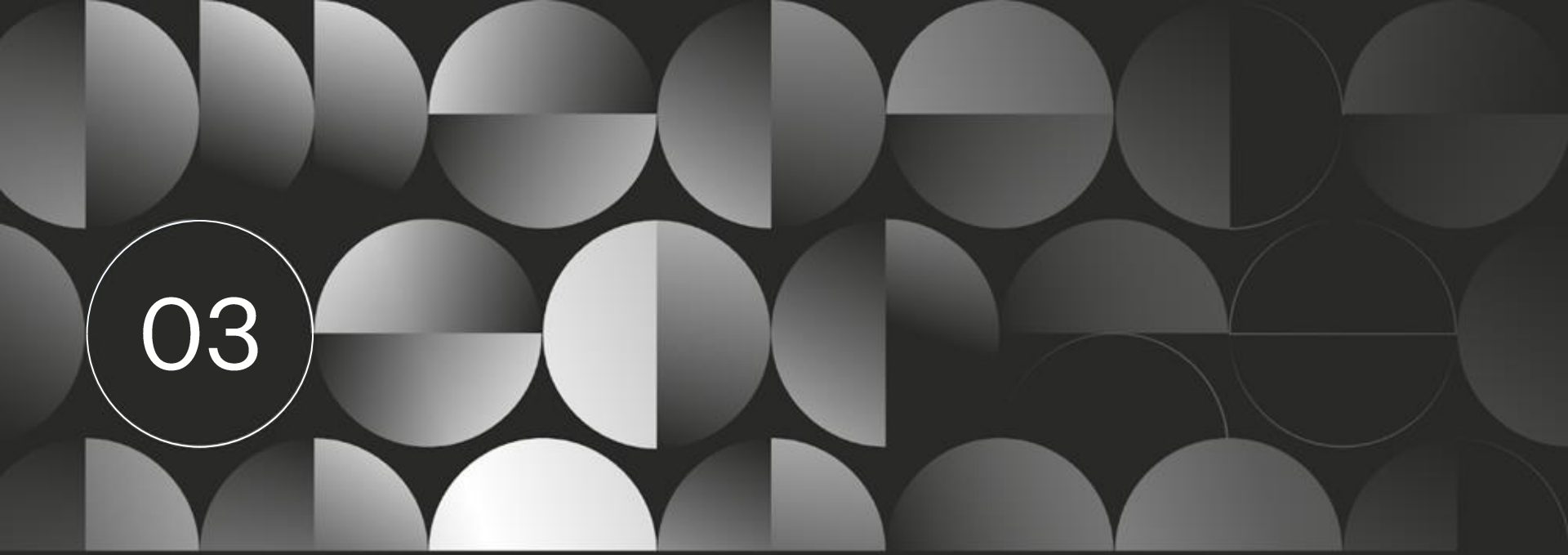
Source : CEA LETI (LID'26)



Source : IMEC (OCP EMEA 2026)

A SiPh active interposer is the universal photonics host platform
LNOI / InP hybridization to boost performances and/or add new future-ready functions

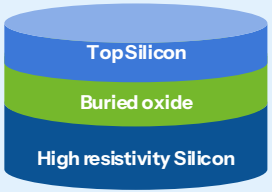
soitec



Photonics SOI: a universal SiPh host platform

Soitec Photonics SOI products portfolio

soitec Photon-SOI 200



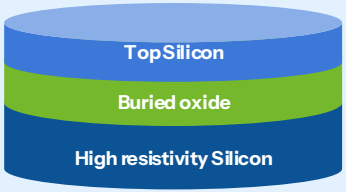
- Sub-µm Si waveguides
- >120nm SiPho process nodes
- Ideal for lower process cost





Pluggables	3D Sensing
NPO Optical Engine	Short-range LiDAR

soitec Photon-SOI 300



- Sub-µm Si waveguides
- Advanced SiPho process nodes (down to 40nm)
- Advanced packaging
- Ideal for high-speed & compute-intensive app.

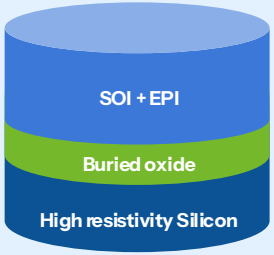






Pluggables	Machine vision	Quantum
xPO Optical Engine	Automotive LiDAR	Optical computing

soitec Photon-SOI + EPI



- Multi-µm Si waveguides
- Legacy Si-Pho nodes (>200nm)
- Low dispersion / high-power
- Ideal for hyperspectral sensing

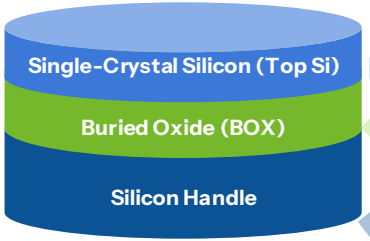


Sensing
Transceivers

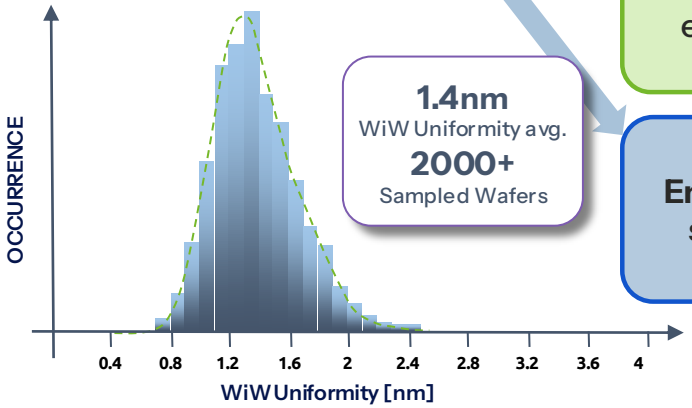
Soitec Photonics SOI value proposition

Material uniformity and quality for high-performance Photonics

Photon-SOI 300

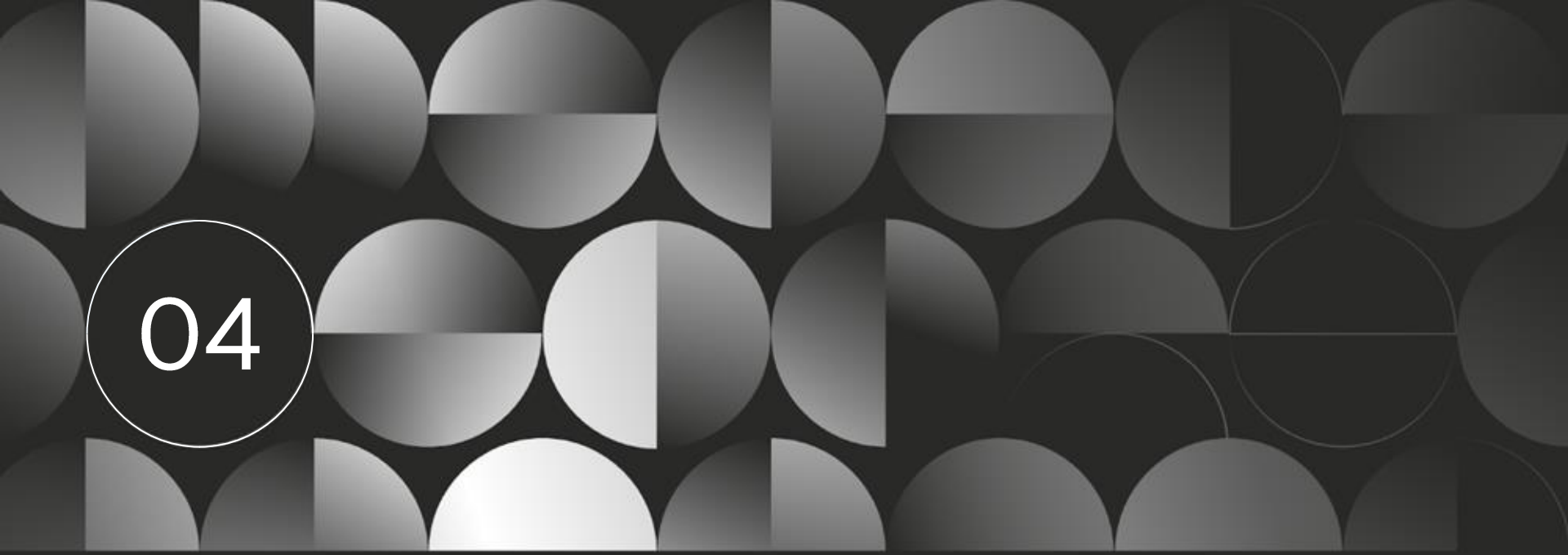


Top Si thickness mapping ellipsometry 41pt mapping:



1.4nm
WiW Uniformity avg.
2000+
Sampled Wafers

Core value for Photonics device:	Substrate control parameters:
Minimizes optical loss and dark current, ensures **predictable phase management.**	• Thickness, refractive index • Surface roughness • Resistivity • Defectivity
Prevents optical/dielectric leakage and eliminates interface charge trapping.	• Thickness, refractive index • Oxide charge/trap density • Si/SiO_2 interface quality
Ensures RF signal integrity and supports reliable packaging.	• Resistivity • Defectivity (BMD) • Bow, stress • Charge trapping



Enhancing SiPh with heterogeneous integration

Why Silicon Photonics hybridization?

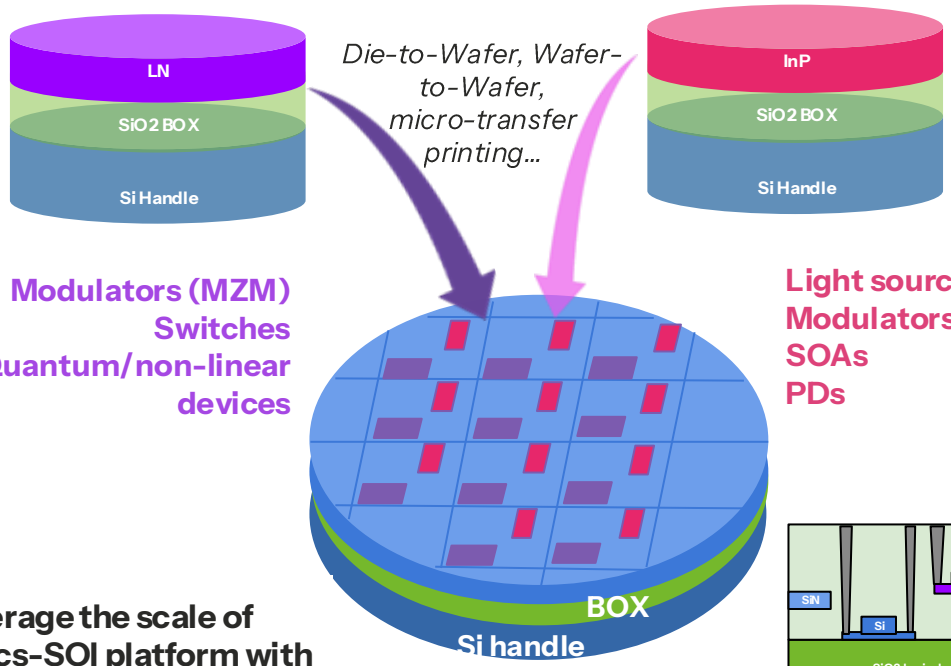
Next generation optical interconnects must improve on three main fronts

Faster, Denser and more energy efficient optical interconnects

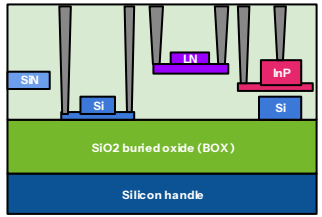
Higher modulation speed
400G/lane
Enable next generation of AI networking

Better energy efficiency
pJ/bit
Reduce power while scaling bandwidth

More integration
Laser, Switches…
New future-ready functions at optimal TCO

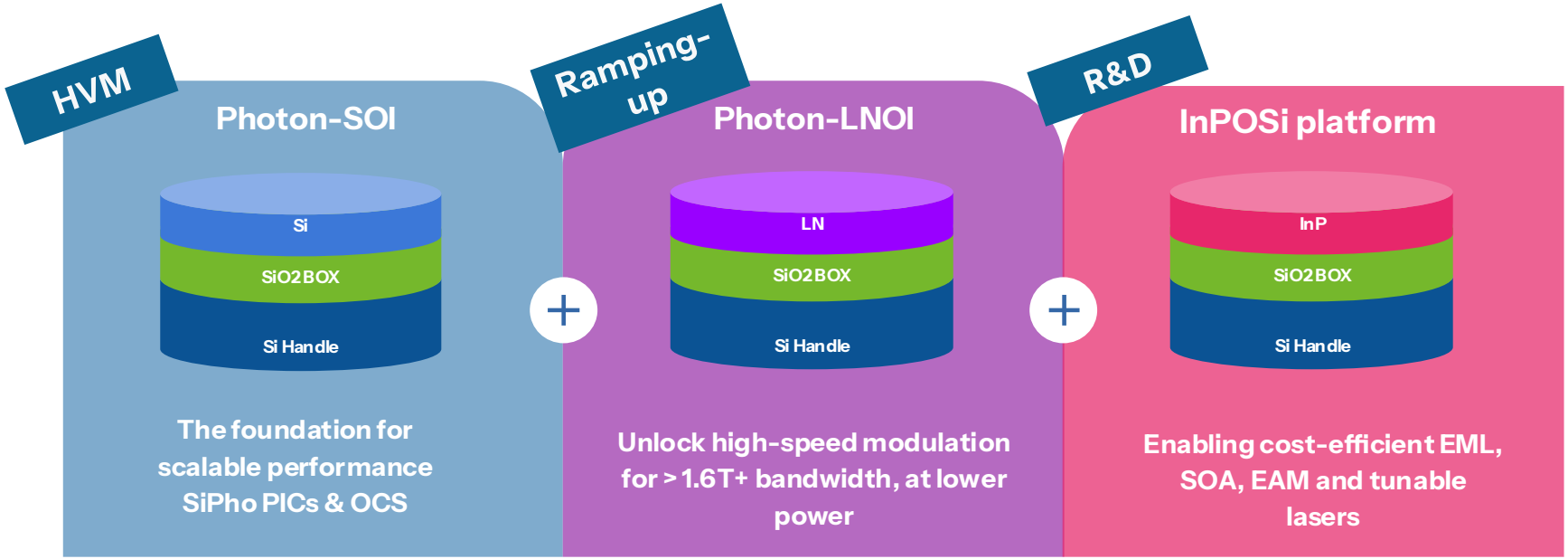


Leverage the scale of Photonics-SOI platform with efficient and economical use of high-performance LN and InP materials.

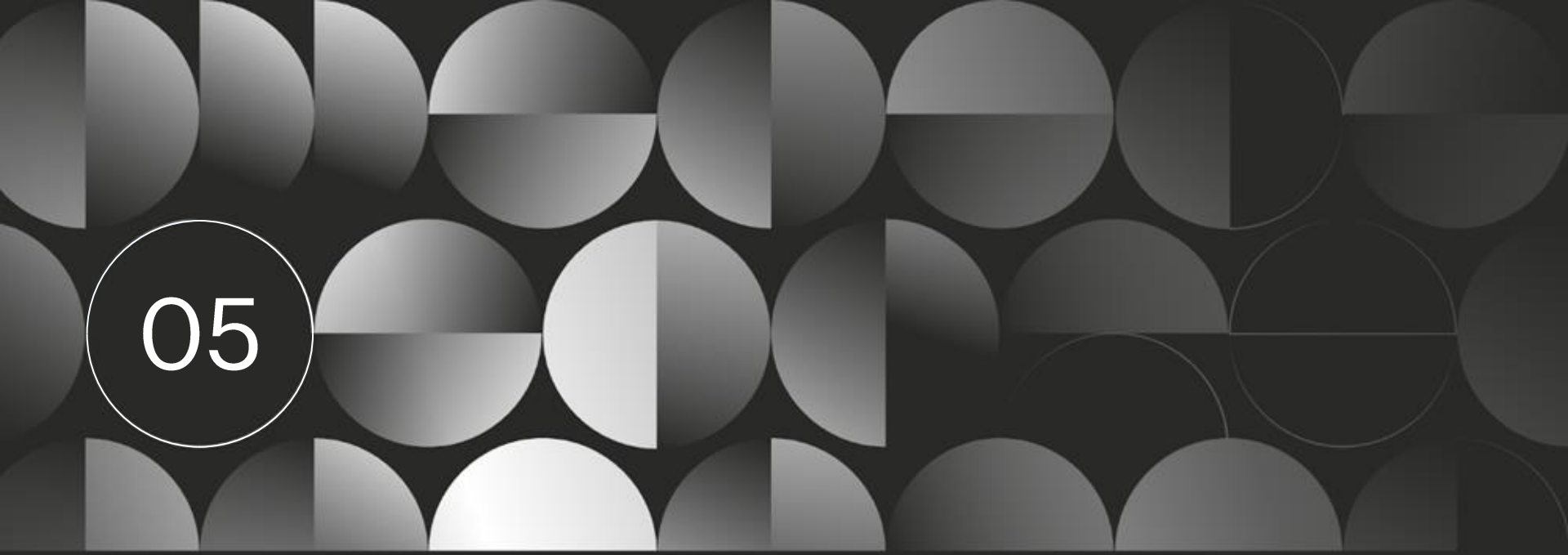


Soitec offering for hybrid/heterogeneous integration

Towards the universal Photonics backbone



Three platforms for standalone or heterogeneous integration to unlock next-gen photonics devices

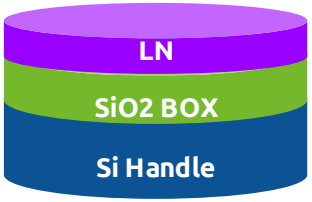


LNOI & InPOSi material platforms

LNOI motivations

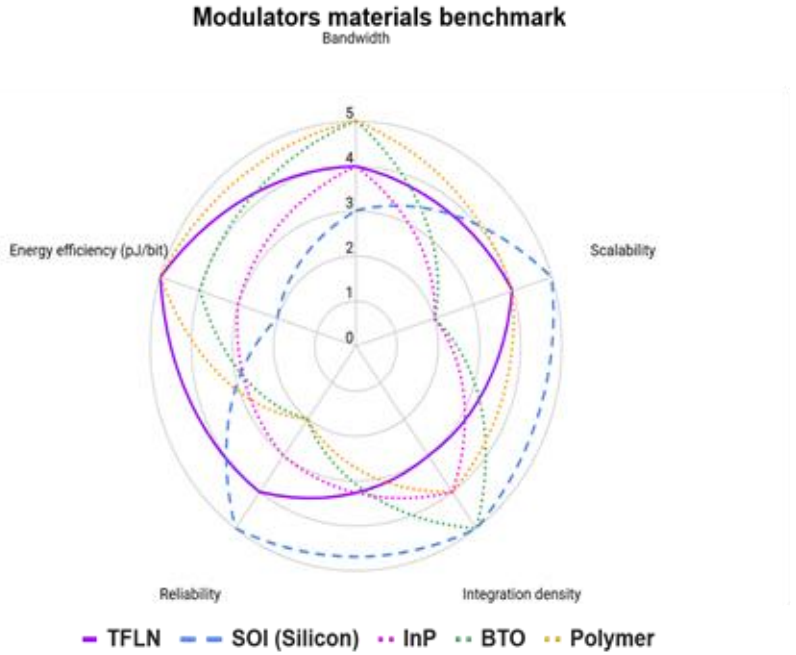
Need for faster, power-efficient modulators for next gen optical interconnects

- **Demand for 1.6 optical transceivers is accelerating and emergence of 3.2T modules from 2028 onwards**
- **Doubling lane speed from 200G to 400G request new modulation material.**



Higher modulation speed
□ 400G / lane

Lower energy consumption
~ -15% wrt Silicon



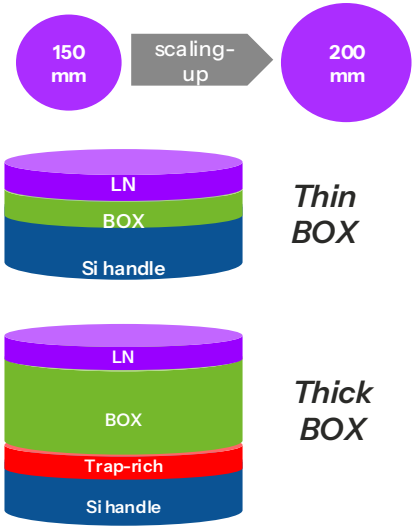
TFLN (LNOI) provides energy efficiency and bandwidth to enhance SOI/SiPh Reliability and Scalability vs. InP, BTO, Polymer...

LNOI platform offer for TFLN devices

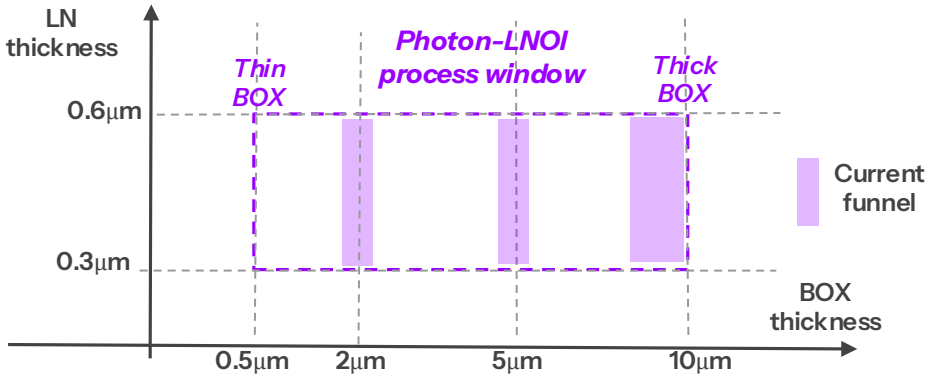
Integration schemes and respective benefits

Product configuration:

- X-cut LN
- High resistivity Si handle
- Trap-rich option for RF performance







SmartCut™ LNOI	Thin BOX ~ 0.5-2µm	Thick BOX ~ 4-10µm
Integration architecture	**Heterogeneous** integration on SOI PICs (W2W, D2W, TP)	**Monolithic** platform Standalone PICs
Key benefits	Higher yield for LN transfer CMOS compatibility	Reduce RF modulator loss Improves optical edge coupling

InPOSi motivations

Need to scale InP material towards CMOS-like usage

Material scarcity

Make several InPOSi wafers from one InP bulk



Manufacturability & integration/packaging

Improve manufacturability & integration thanks to :

- Reduction in mechanical fragility
- Higher Structural Stiffness (Minimized Bow & Warp)
- Only Si backside grinding

Thermal

Thermal Conductivity:

Silicon is 2x better than InP & thinning possible <<100um

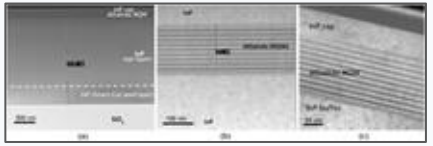
Enablements:

- Increase laser power density
- Improve laser wavelength drift over temperature and thermal electro coupler design

Device

Explore performances improvement

Optimize process flows.



J. Appl. Phys. 138, 105305 (2025)

Soitec is partnering with InP supply chain leaders to demonstrate InPoSi benefits across materials, device performance, packaging, and thermal management.

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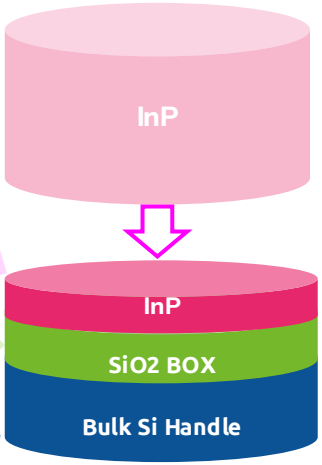
InPOSi technology substrate platform

R&D platform scope and value proposition

InP seed layer
- Doping : n-type (Sulfur) or S.I. (Fe) or p-type
- Thickness : 0.3µm to 0.5µm
- Epi-ready

Buried Oxide (BOX)
- Thick BOX (0.5 to 2.0µm)
- Thin BOX (< 0.2µm)
- **No BOX**

Handle Si
- Standard bulk Si
- Advanced Si (High-Resistivity, trap-rich…)

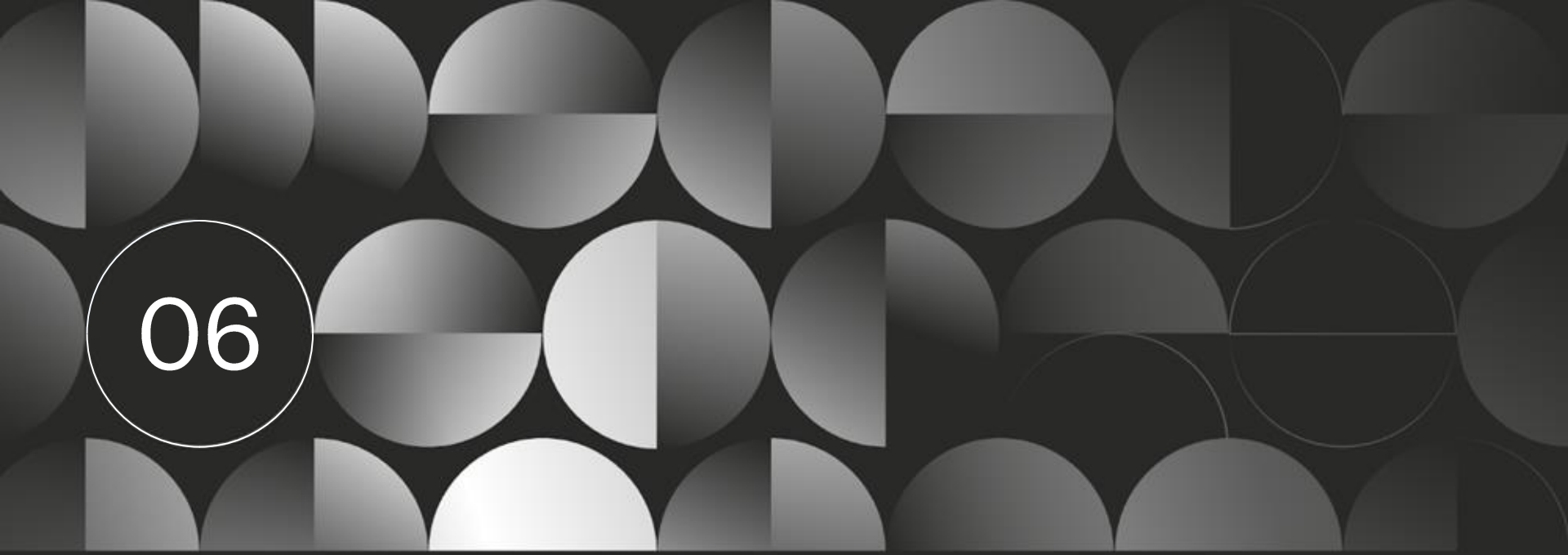




InPOSi value proposition:

- **Supply security & scalability**
- **Thermal excellence**
- **Yield & manufacturing**
- **Cost optimization**

Soitec InPOSi: Efficient InP Scaling for High-Performance Heterogeneous Integration of III-V in Photonic Devices



Takeaways

Takeaways

- **Photonics for AI scaling starts at material level:** Reducing optical bottleneck to maximize GPU utilization and slash cost-per-token.

- **Soitec substrates roadmap enabling silicon photonics hybridization:**
  - Photon-SOI: nm-level top Silicon uniformity for a universal silicon photonics host
  - Photon-LNOI: Unlocks 400G/lane while enabling ~15% power savings (at pJ/bit level)
  - InPOSi: Enable native III-V lasers and active devices onto CMOS lines, improving yield, cost and thermal performance.

- **Proven industrial HVM scale:** Soitec multi-site SOI manufacturing securing high-yield volume for hyperscalers.

- **Bright future for Silicon Photonics:** Powering high-volume AI datacom today, while establishing the material foundation for emerging new segments (e.g LIDAR, biosensing, quantum …)

semi | SEMICON TAIWAN



Thank you

Let's accelerate the Silicon Photonics market adoption *together* !

Part of this work is supported by
European CHIPS JU Project "Starlight"

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STARLight

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