矽光子異質整合封裝與測試之技術趨勢與挑戰

Technology Trends and Challenges in Packaging and Testing for SiPh Heterogeneous Integration

LIGHTMATTER

Jesse Wang
Director, Supply Chain Operations
2026/05/28

$850M RAISED

Fidelity
Google Ventures
Sequoia
Spark Capital

Viking
T. Rowe Price
Matrix Partners
SIP Capital

MIT
Stanford

Mountain View (HQ)

Boston

Hsinchu, Taiwan

Toronto

320 EMPLOYEES

Nicholas Harris, PhD
Founder, CEO

Darius Bunandar, PhD
Founder, Chief Scientist

Thomas Graham
Founder, Head of ML

Simona Jankowski
CFO

Ritesh Jain
SVP, Engineering & Ops

Bob Turner
SVP, Sales & Solution Arch

Roy Kim
VP, Product

Sujatha Wagle
VP, Supply Chain Ops

Beth Keil
SVP, People

Boon Tan
VP, Product Engineering

Colin Sturt
General Counsel

Kaushik Patel, PhD
VP, Photonics & Si Eng

Steve Klinger
VP, Ecosystem & Alliances

Praveen Kukkamalla
VP, Sales

Kurt von Hausen
VP, Cloud Services Sales

405 PATENTS

Granted & Pending

CO-PACKAGED OPTICS INDUSTRY ECOSYSTEM

PIC design

BROADCOM, NVIDIA, MARVELL, intel, AyarLabs, COHERENT, cisco, RANOVUS, LUMENTUM, nubis, LIGHTMATTER, celestial AI

ASIC & xPUs design

NVIDIA, BROADCOM, MARVELL, intel, AMD

Foundries

PIC

GlobalFoundries, tsmc, SILTERRA, intel Tower, amf

ASIC & xPU

tsmc, intel, SAMSUNG

Packaging / System assembling / Testing

ASE HOLDINGS, FOXCONN 鴻海科技集團, fabrinet, SPIL, Amkor Technology, JABIL, SAMSUNG, TERADYNE, FormFactor

SOI wafer & Epi-wafer

soitec, Shin-Etsu, GW, IQE

Light Source (Device)

CW-DFB

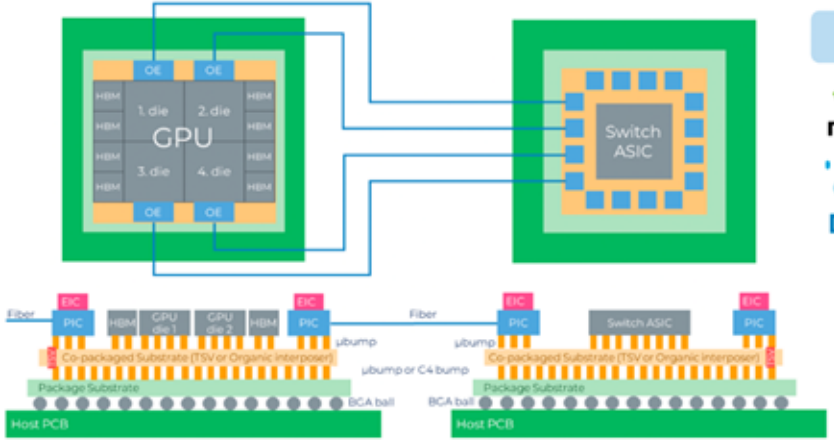
LUMENTUM, COHERENT, BROADCOM, SCINTIL, intel, OpenLight, sivers, LIGHTMATTER

Quantum dot

innolume, NRC · CNRC, QD LASER

Comb

SCAPE PHOTONICS, Pilot, enlightra, AyarLabs



CPO Equipment (AI server or switch)

NVIDIA, Micas Networks, Ruijie 锐捷, cisco, H3C, DELL Technologies, Hewlett Packard Enterprise, SUPERMICRO, GIGABYTE, Inventec, wistron, wiwynn, ACT, Lenovo

End customers (CPO users)

aws, Microsoft Azure, Meta, OpenAI, X, TESLA, SoftBank, ORACLE, Tencent 腾讯, Bai 百度, ByteDance, Alibaba Group

ELSFP (Module)

BROADCOM, cisco, COHERENT, molex, O-Net

EIC & DSPs, Retimers, SerDes, PHY

MARVELL, CREDO, MACOM, SEMTECH, BROADCOM, maxim integrated, MaxLinear, ALPHAWAVE SEMI, Astera Labs

Connectors

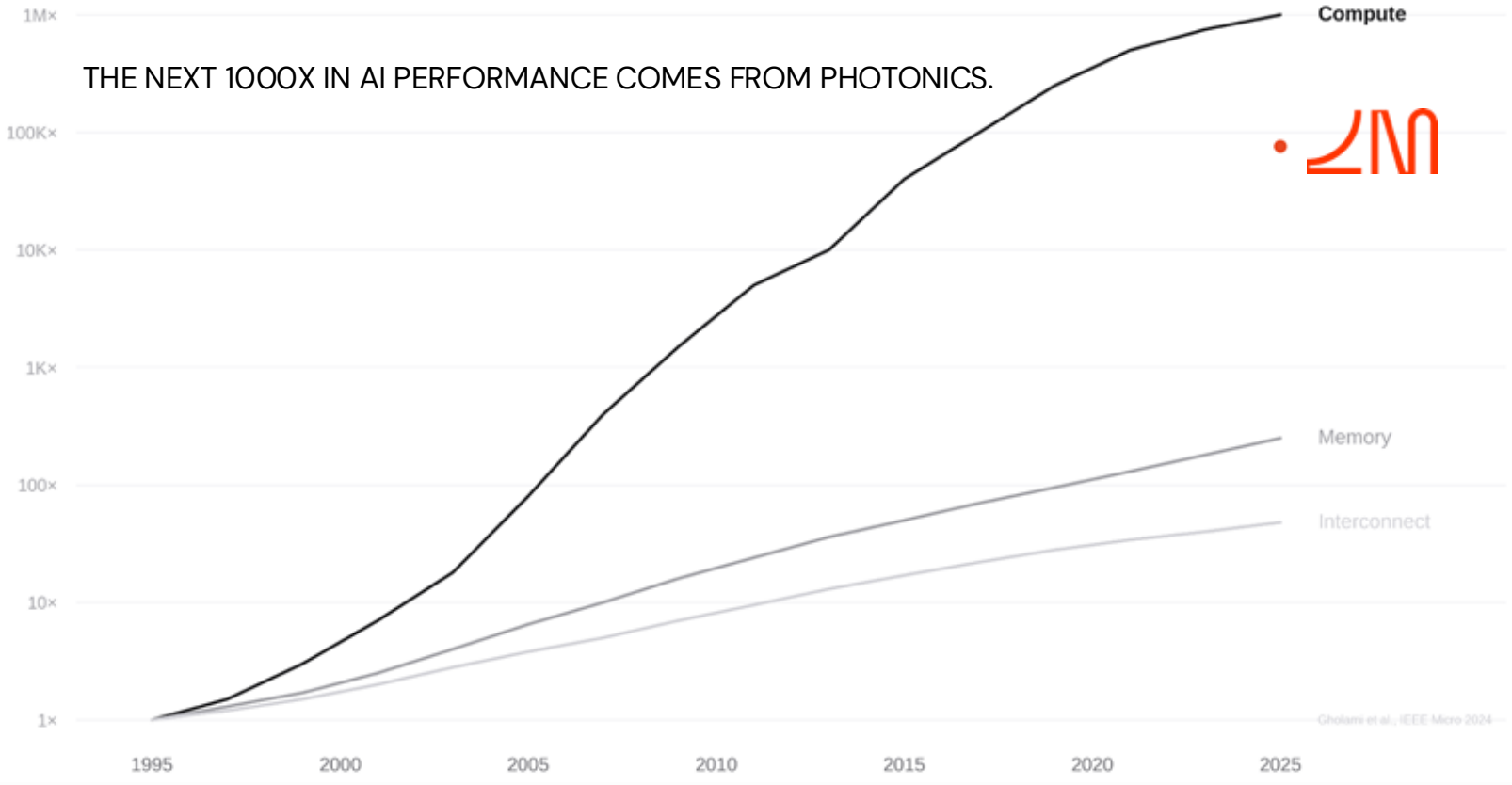
TOS 太辰光通信, molex, USCONEC, samtec, TE, SENKO Advanced Components, TFC 天孚通信

Fibers

CORNING, SUMITOMO ELECTRIC, HENGTONG GROUP, YOFC, Fujikura

*non-exhaustive list

THE NEXT 1000X IN AI PERFORMANCE COMES FROM PHOTONICS.

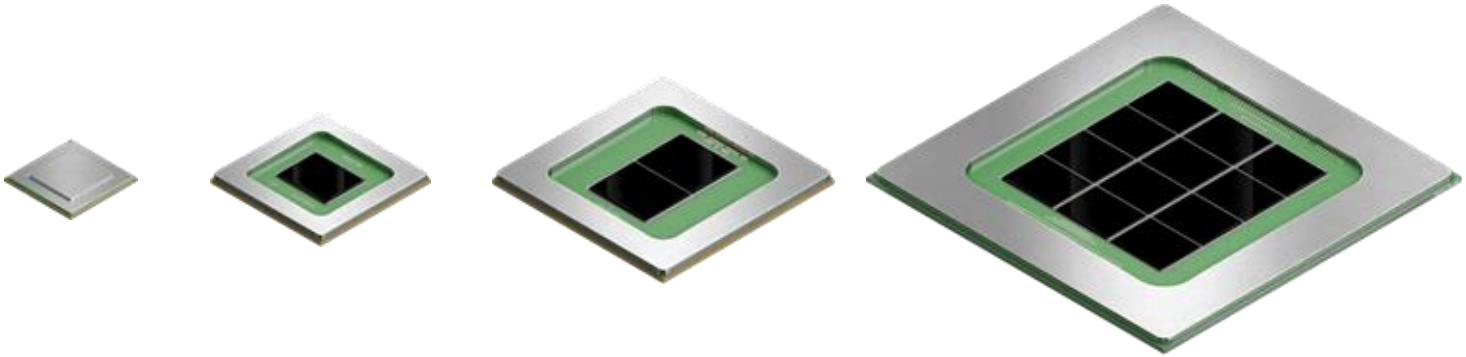


The last 1,000x in AI performance was all about compute.

The next 1000x is all about interconnect.

CHIPS ARE GETTING BIGGER

I/O at the shoreline is not enough
3D-stacked photonics is the future

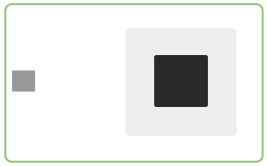
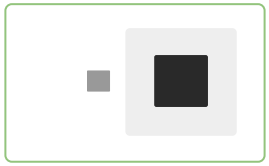
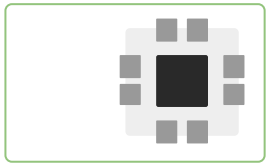
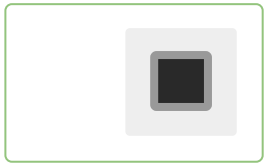


2000 2010 2020 2030

The Promise of Silicon Photonics

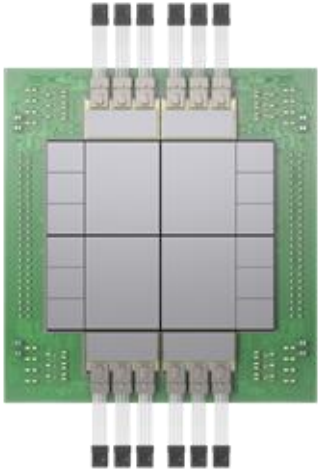
Moving Closer to the Chip

PCB
Chip Package
Optical Engine
XPU/Switch

	2025	2027	2028	2029+
				
	GEN 1 **Pluggables**	GEN 2 **NPO/OBO/XPO**	GEN 3 **2D CPO**	GEN 4 **3D CPO/Interposer**
Power Efficiency	17-20 pJ/bit	8-15 pJ/bit	6-10 pJ/bit	1-3 pJ/bit
Bandwidth	1x Speedup	2x Speedup	8x Speedup	100x Speedup
		• Pre-packaged OE (PIC+EIC) • LR SerDes, Re-timer	• I/O chiplet (PIC+EIC) • In-package, XSR SerDes	• 3D stacked PIC/EIC chiplet • Standard pkg, UCIe • Advanced package, OCS

From NPO to 3D Interposers, Lightmatter has the 10 year roadmap for photonics in validation racks today

Advantages of CPO Technology



Reliability:

- Fewer Failure Points: It reduces discrete components and physical connectors, common points of failure in massive clusters.
- Thermal Stability: The integrated nature allows for unified cooling strategies, provide more stable temperature management for sensitive optical components.

Serviceability:

- Encouraging results with Pluggable Laser Sources (Remote Las Module)
- Detachable Fiber Attach Unit (dFAU)
- Detachable Optical Engine

Why Hyperscalers Are Focusing on CPO Now

Power per bit must drop sharply

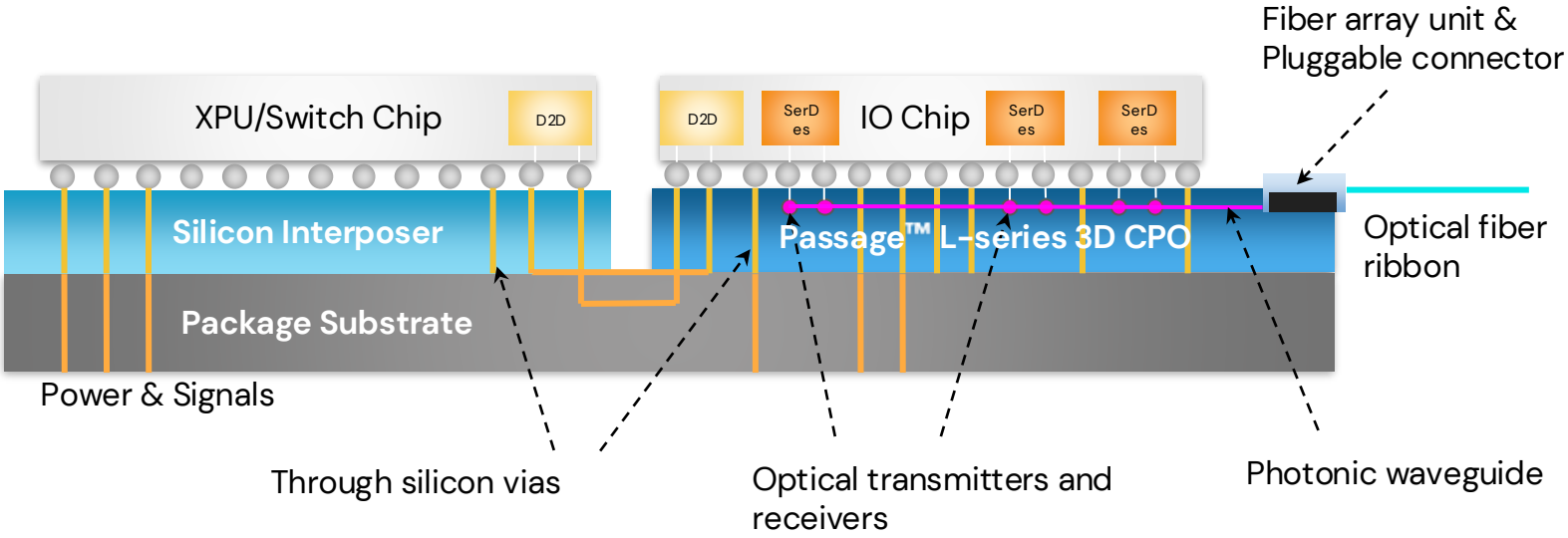
Cabling complexity must collapse

Reliability must improve at million-link scale

System density must rise without copper/thermal overload

CPO Solves All 4 Simultaneously:
Up to 1K XPUs at ¼ the power, 4X the Bandwidth, 5X Reliability

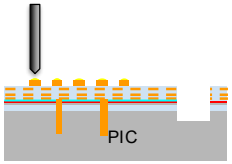
3D Stacking Needs Compact Optical Devices



Standard processes today

- Bump pitch: ~120 µm
- Bump size: ~80 µm
- Area for a transmitter/receiver: 0.015 mm²

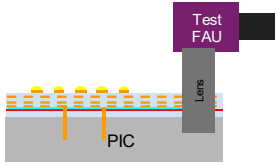
Integrated Assembly and Test Process Flow



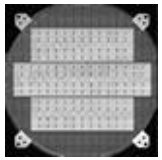
Wafer level PIC Test

Ship

Wafer level Lens attach



Wafer Electrical –Optical coupler test



EIC Si attach

TSV reveal, RDL, Bumping

Wafer level Assembly

KG OE

Ship

Wafer Electro-Optical Engine test

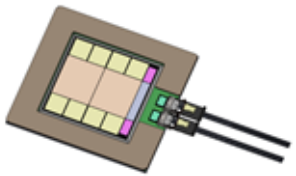
Singulation

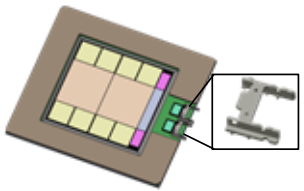
xPU + OE attach, Underfill

d-FAU socket attach

Stiffener attach, ball attach

Package electro-optical test





Known Good OE Chiplet

OSAT partners

ASE

Amkor Technology

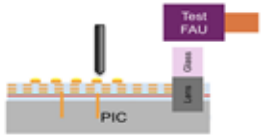
Assembly Operations

Test Operations

Test Point Flow

TP1

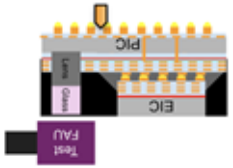
PIC Wafer Level Test (vertical coupled)



EE, OE, OO main circuit

TP2

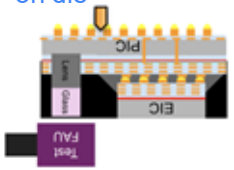
Bonded OE (PIC+ EIC stack) on wafer



EE, OO Main circuit, OE main circuit

TP3

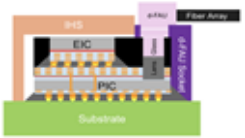
Singulated OE (PIC+ EIC stack) on die



EE, OO Main circuit, OE Main circuit

TP4

Packaged OE/SLT



OE main circuit, High speed

ADVANTEST TECHNOPROBE MPI CORPORATION ficontec FormFactor

Focus Areas for CPO development

KGOE Integration

Delivering Known Good Optical Engines (KGOE) for seamless mainstream packaging integration.

Cost Optimization

Economic solutions for Package, Assembly, and Test phases in high-volume flows.

Fiber Attach

Driving breakthrough innovations in Fiber Attach Technology and detachable interfaces.

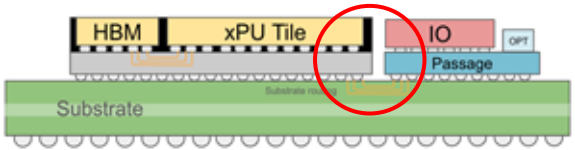
HVM Equipment

Deploying HVM-friendly optical attach equipment and low-cost metrology systems.

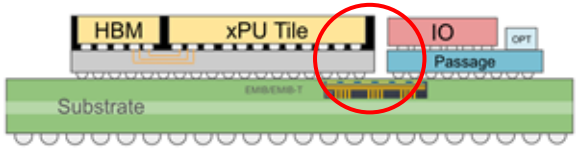
Materials & FAU

Utilizing HVM-friendly materials and standardized FAU solutions for scalability.

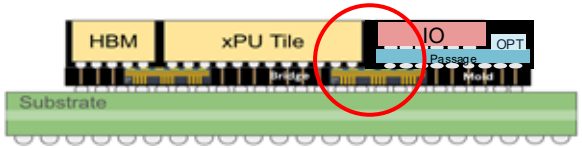
Deliver Known Good Optical Engines



xPU to OE link: routing on organic substrate



xPU to OE link: routing on Silicon Bridge →
EMIB Package Technology



xPU to OE link: routing on Silicon Bridge or Si Interposer
→ CoWoS_L/S Package Technology

Deliver Cost Effective Solutions

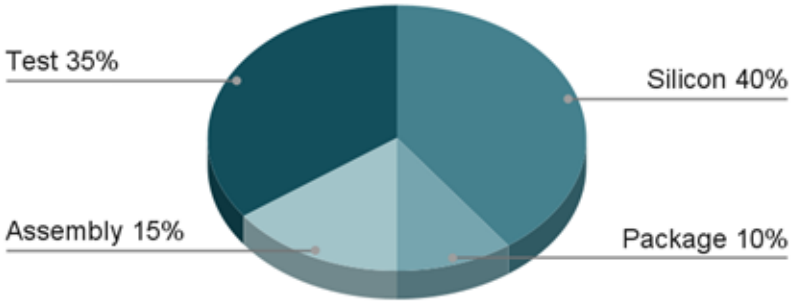
Backend Costs (PAT) are High. Driven by

- Assembly yield concerns due to fiber attach
- Higher test times
- Lack of standardization

Key Vectors:

- Design product with DFT/DFM upfront
- Drive Innovation in fiber attach
- Equipment & material development to improve throughput in assembly and test

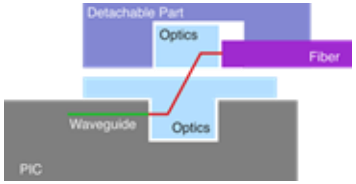
SiPho Cost Breakdown



Note: Graph shown for demonstration purposes only

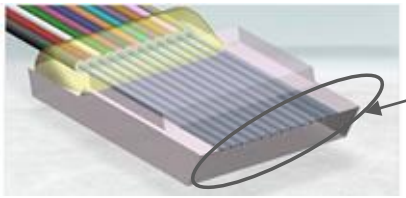
Deliver Scalable Fiber Attach Solutions

Key Performance Indicators for HVM



Wafer Level Optical coupler

High Yield	✅
Meet Product Performance	✅
High Throughput (UPH, units per hr)	✅
Known Good OE	✅
Scalable across package arch	✅
Serviceability	✅



FAU facet with PM fiber

FAU cost

- FAU is one of the main BOM cost
  - manual manufacturing process
- Automated PM fiber orientation
- Automated fiber insertion into MT ferrule
- Standardization of connector spec

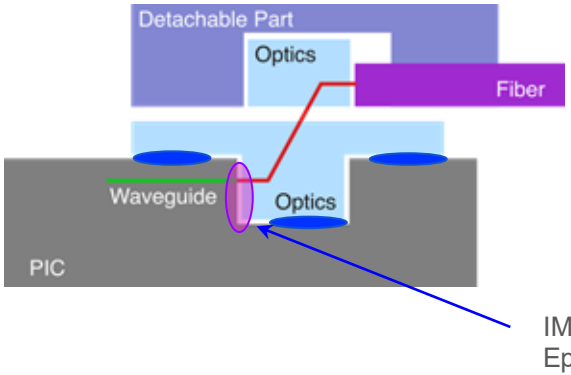
Deliver Scalable Solutions for HVM

Equipment

- Transition to automated alignment in seconds, not minutes
- Parallel processing: handling, alignment, dispense and UV cure
- Re-configurable to support multiple products

Materials

- Single epoxy for the entire OE
- Reflow compatible materials
- Fast UV cure (<5 sec) instead of 30 sec to minutes
- Low Tg (conforms with warpage change)



LM Methodology & Partnership for HVM Readiness

Design/Architecture

- SI/PI
- Substrate Design
- Design for manufacturing /Reliability
- Thermal analysis
- Mechanical Design /Analysis
- Optical Analysis

Assembly/Test

- 2D and 3D Heterogeneous Integration & process dev.
- Wafer Electrical Sort and Optical Characterization
- Wafer and component test points through the process flow

Yield/Data Management

- Database with lot/unit level traceability
- Best known methods development to manage yield analysis
- Failure analysis and corrective action including binning strategies

Reliability/Validation

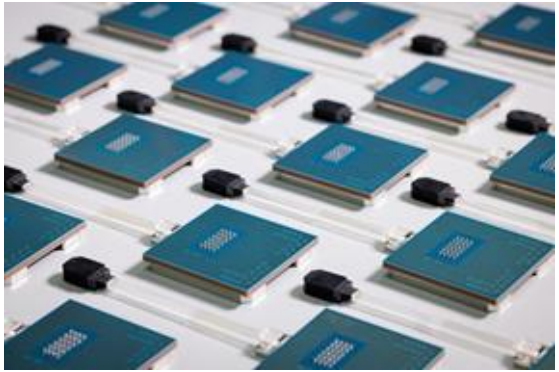
- Electrical and Compliance Tests – ESD, Latch Up, EMI/EMC
- Package/Environmental – TC, UHAST, HTS, S/V, Fiber Integrity
- Operational – HTOL
- Failure rate and Lifetime prediction

KEYSIGHT TECHNOLOGIES · cadence · Ansys by Synopsys · MathWorks · 3DS · ASE
Amkor Technology · FormFactor · ADVANTEST · Telcordia Technologies · JEDEC

Lightmatter's Leadership in Photonics

10-year roadmap In sIlicon today

M1000 3D photonic superchip with record-breaking 114Tbps bandwidth



Leading bandwidth density

World's first 16-wavelength DWDM link: 800G/fiber bidirectional & 1.6T/fiber unidirectional

Rackscale quality and reliability

Validation data center with hundreds of photonic interconnects

3D Photonics Ecosystem

Custom ASIC Partners — GUC and others

Passage™ SerDes EIC Partners — cadence, Qualcomm, SYNOPSYS

Passage™ PIC — LIGHTMATTER, tsmc, Tower Semiconductor

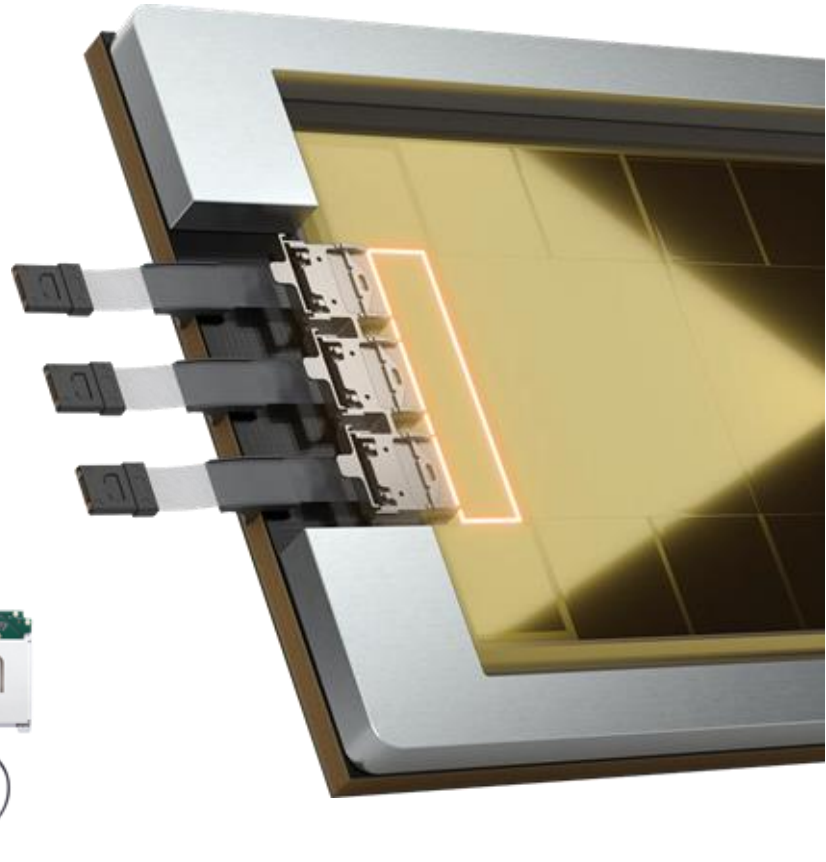
Detachable Fiber Array Unit — SENKO, 波若威科技 BROWAVE CORPORATION, TwinstarTech

Guide® VLSP™ Light Engine

ASE

Amkor Technology

tsmc



THANK YOU!