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# The Silicon Heartbeat of the AI Economy

## The Efficiency Paradox in Next-Gen Data Center Silicon

Bhushan Chitlur

CHIEF ARCHITECT DATACENTER & AI

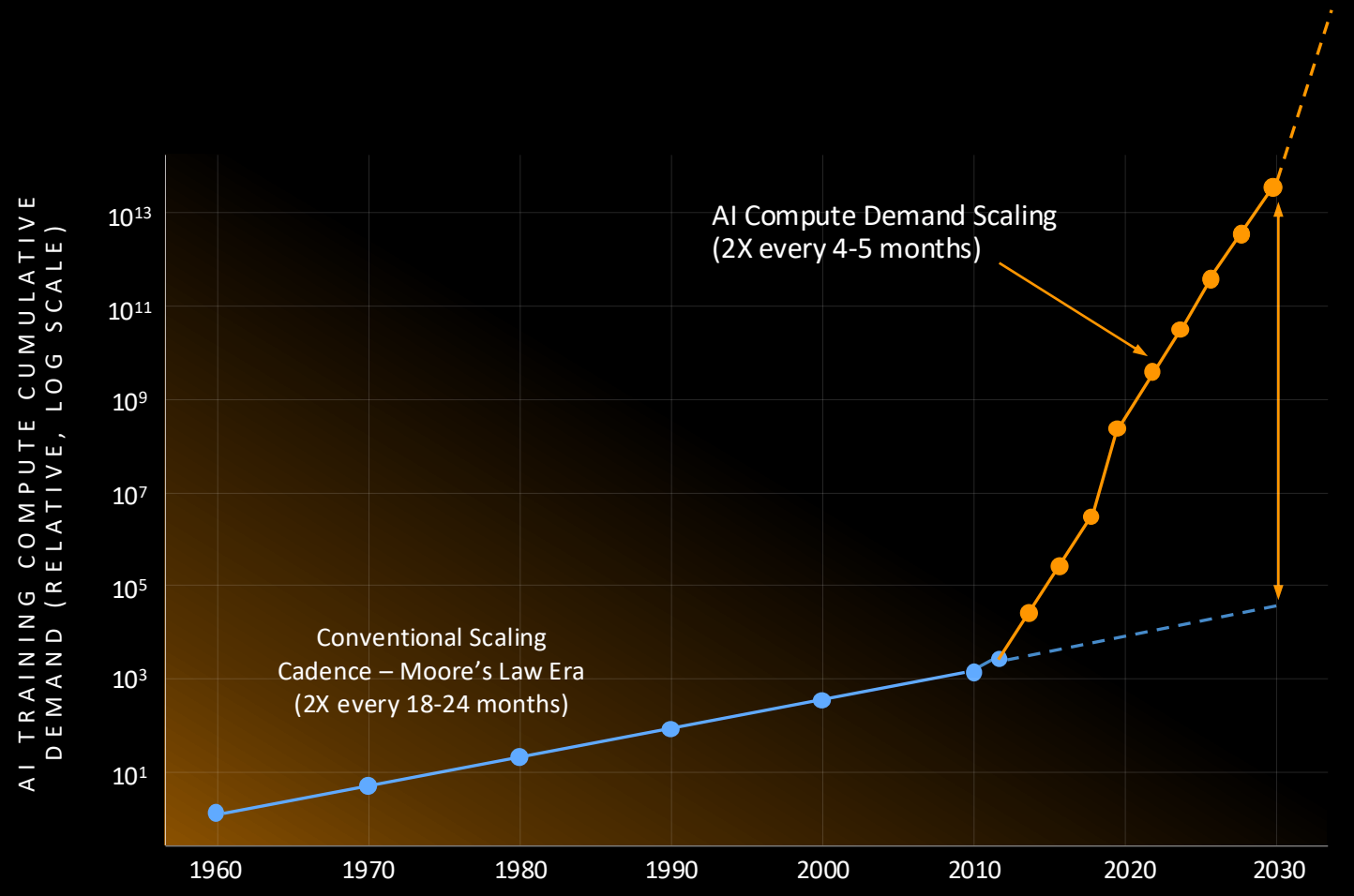
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# AI Compute Demand Is Accelerating Faster Than System Scaling

## A new strategy is required

Needed to close the computing demand gap:

- Investments in infrastructure
- Innovations in architecture (Rack, Systems, XPUs, Memory, Interconnect)




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*2026-2030 values illustrative / extrapolated*

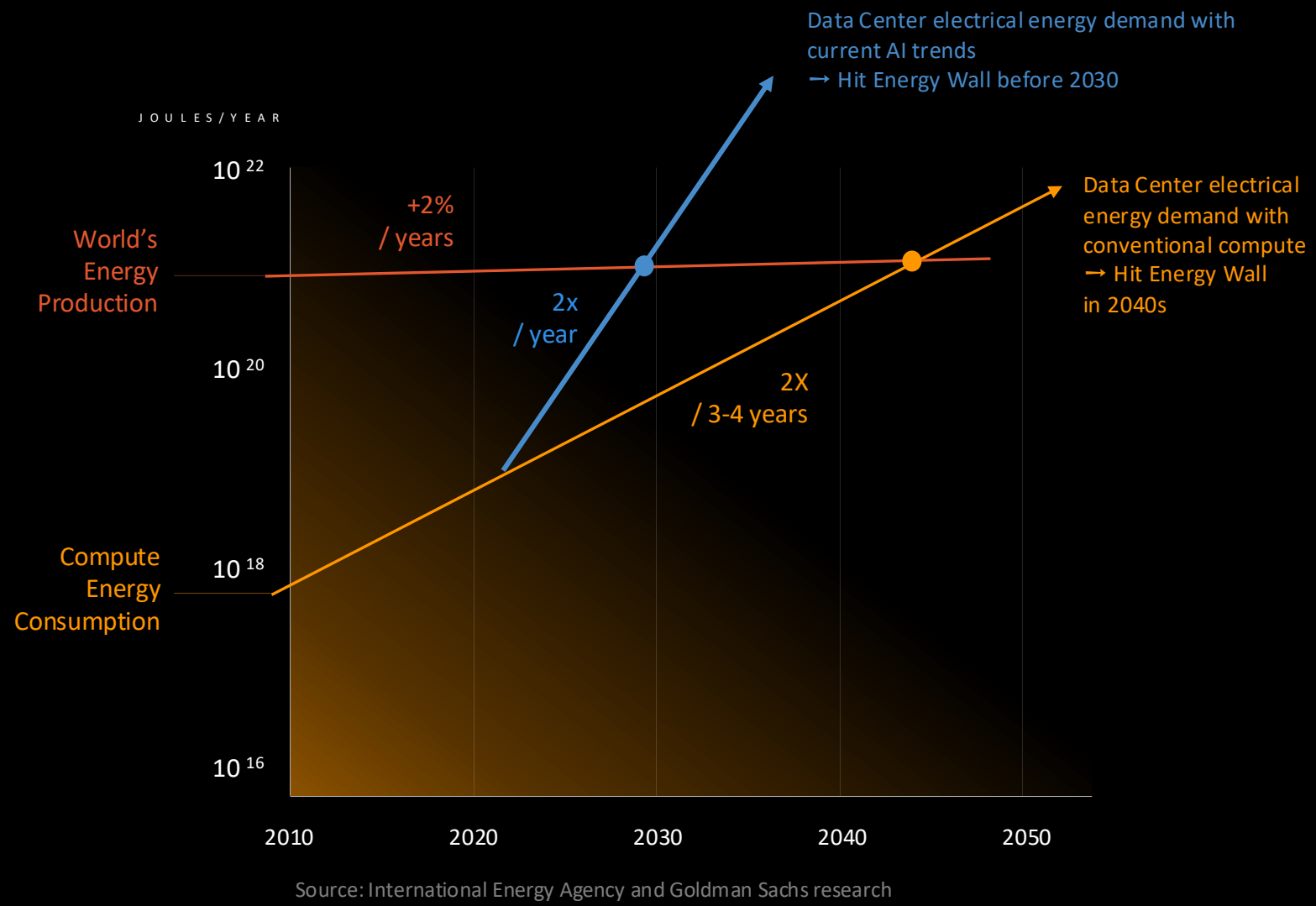
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# Energy Is Our Most Significant Constraint … and Our Greatest Opportunity

The energy wall is a global, unavoidable constraint

We need to make energy a first-class metric and design priority

This constraint is our greatest catalyst for innovation

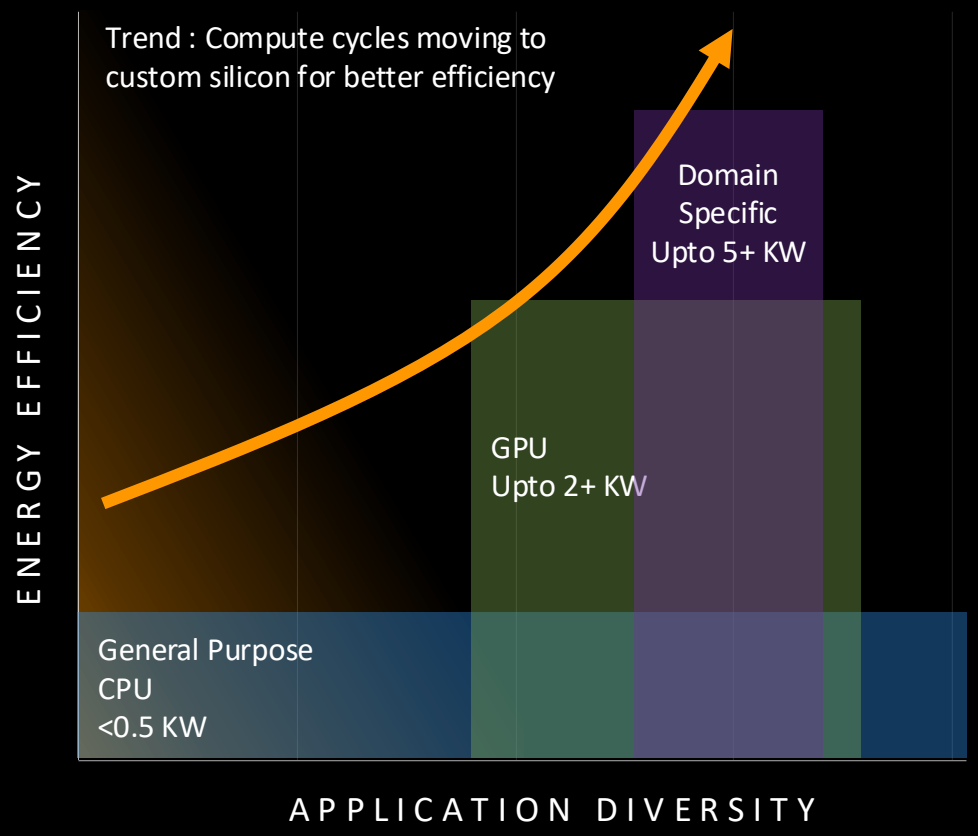



Source: International Energy Agency and Goldman Sachs research

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# Energy Efficiency Trends and Enablers




ENERGY EFFICIENCY ENABLERS

**Wave 1** : General Purpose CPU (<1x Reticle)

Single core/thread → multi-core/thread/virtualization
Moore's Law scaling

**Wave 2** : GPU (<10x Reticle)

Embarrassingly parallel SW
Device/Node/Rack level parallelism (scale up/out)

**Wave 3** : Domain Specific Architectures (<40x Reticle)

Custom Compute pipelines
Heterogenous 2.5D/3.5D, Wafer scale integration
Optics and bidirectional interconnects

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# Heritage of Innovation

## Data Center Update

IP AND PRODUCT INVESTMENTS → DATA CENTER FIRSTS → IP AND TECHNOLOGY EXPANSION →

**2011** Enterprise & Data Center Investments

**2016** Enterprise Switch Launched

**2020** World largest InFO PKG (91x91mm^2) volume production

**2022** World 1st Hybrid CoWoS (85x85mm^2) volume production

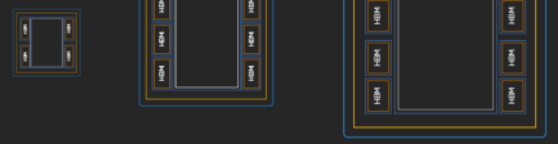
**2024** Long Reach Customizable 224G SerDes

**2025** NVLink Fusion Intel EMIB

**2026** First production design ships in Q4

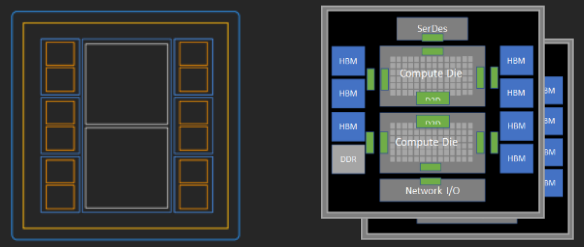
TAPE-OUTS-> INTEL I16 TSMC N3P TSMC N2P TSMC A14

VOLUME PRODUCTION



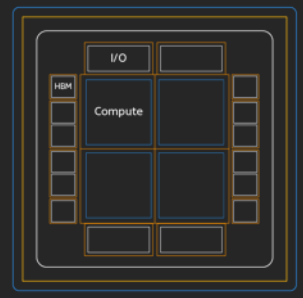
MCP 1x 2x

DESIGN PHASE




3x+ 5x+

ARCHITECTURE PHASE




9x+

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# MediaTek Data Centered Solutions Overview

Strong Data Center Growth – A Breakout Year

2026

~~$1 Billion (USD)~~

$2 Billion (USD)

~~2028~~ 2027

TAM

$70B-$80B

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15%-20%




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# MediaTek: One Partner from Workload to Rack

From Workload analysis to Silicon to Rack design, MediaTek delivers a fully co-optimized, end-to-end design journey to achieve the best Perf/TCO

WORKLOADS › ARCHITECTURE & SILICON › RACK/CLUSTER INTEGRATION




Algorithmic analysis and innovations




Heterogenous silicon integration
2.5D/3.5D/Wafer Scale
Memory, Optics



Custom Rack/Cluster design

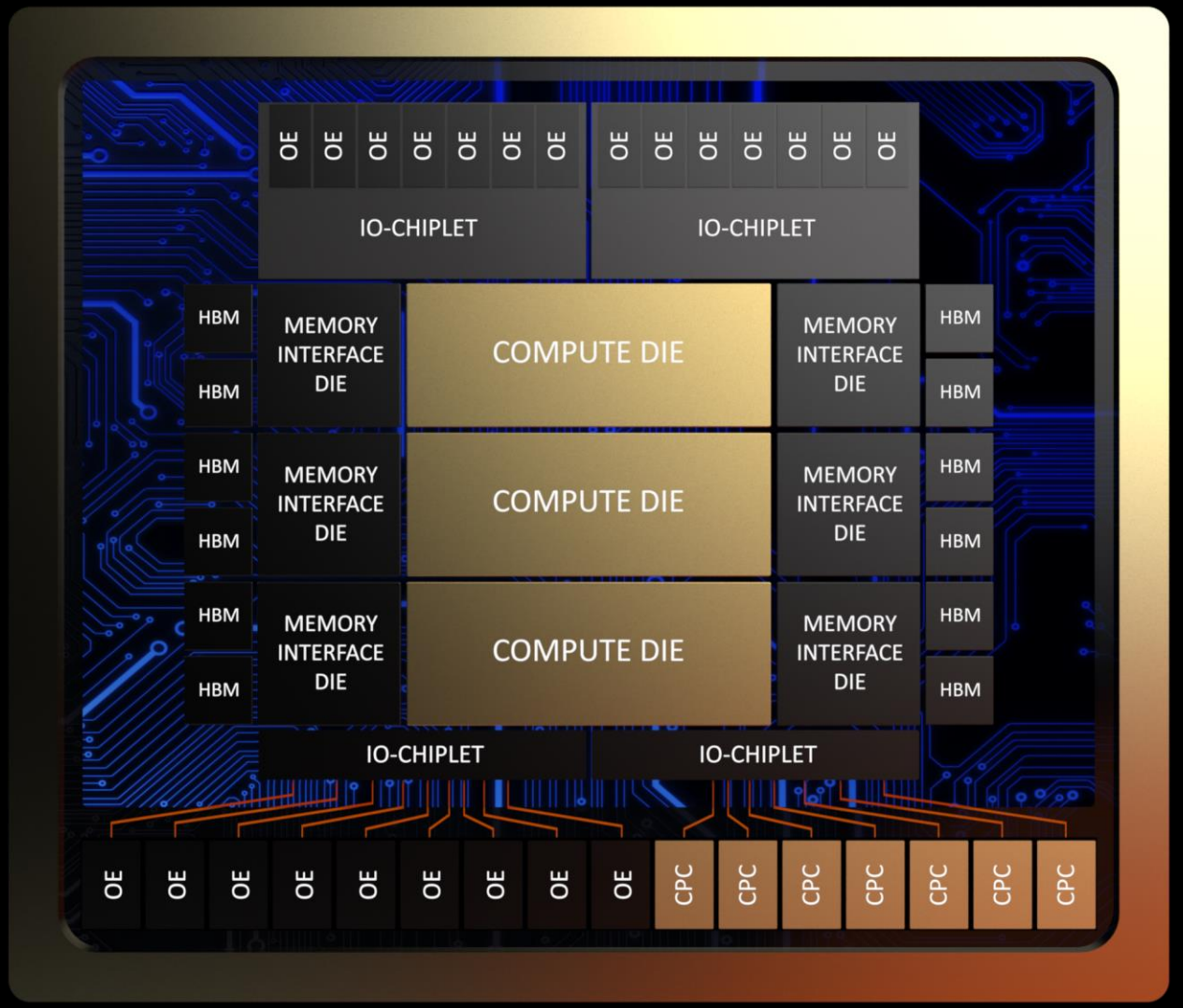
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# xPU

**BETTER** Perf/Watt and Perf/TCO with **LARGER** and more **COMPLEX** integrations

MediaTek is investing in technologies and IPs to enable industry leading 10x+reticle designs solutions



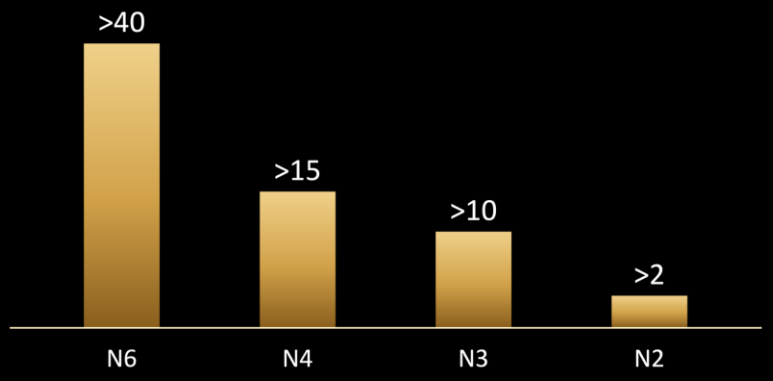


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# MediaTek Capabilities for Improving Compute Perf/W

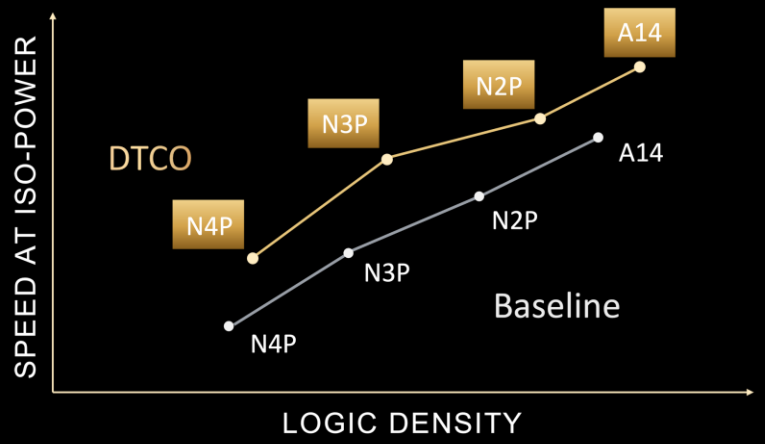
## EARLY NODE ADOPTION

MediaTek Tape-outs per TSMC Node



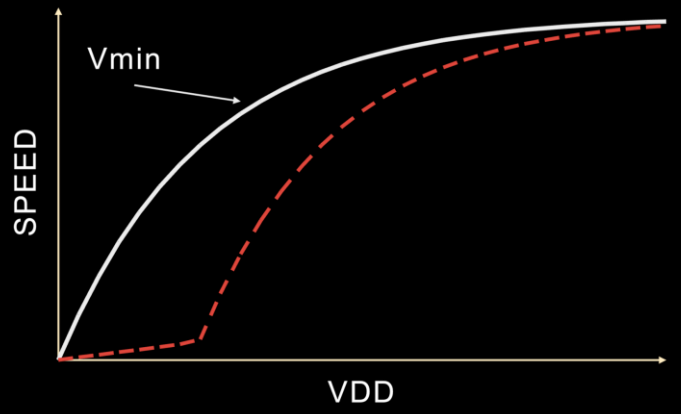

1st wave of 2nm tech adoption in 2025
A14 Test Chips in mid-2026

## DTCO




Process entitlement with additional Design Technology Co-optimization (DTCO)

## LOW VOLTAGE DESIGNS

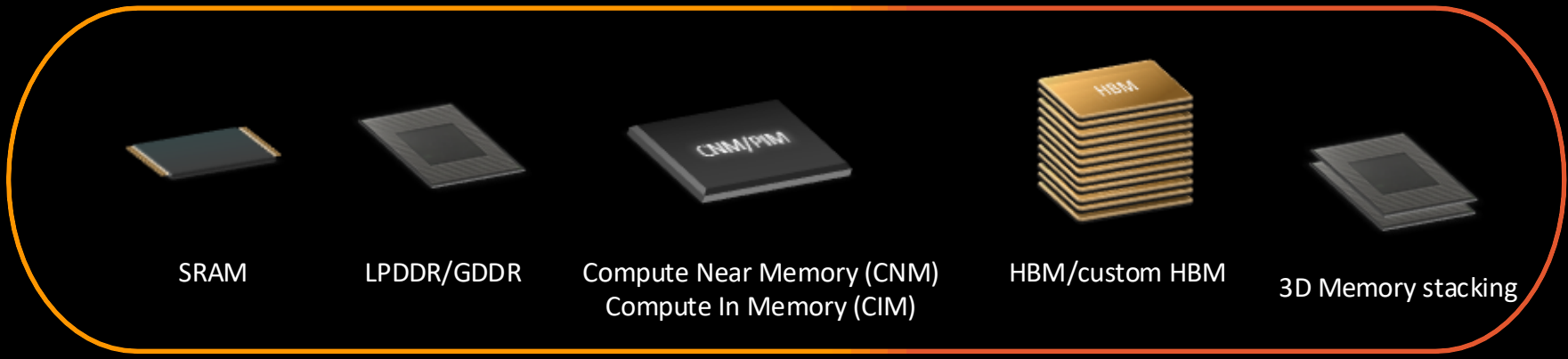



Low Voltage designs for better Performance/Watt

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# Memory: A Critical Enabler For xPU




Training and inference specific memory innovations are critical for step jumps in performance

MediaTek memory solutions for xPU Perf/W and Perf/TCO

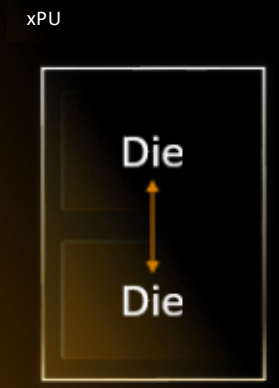
- Extending world's best performing LPDDR solutions with DC capabilities
- Leading edge best in class custom SRAM solutions
- Standard and Custom HBM development
- 3D stacked memory for large capacity and BW


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# MediaTek Interconnect Technologies and IP

Interconnect solutions that span from die to rack for best in class perf, power and reach

## ON PACKAGE
Die-to-die interconnect



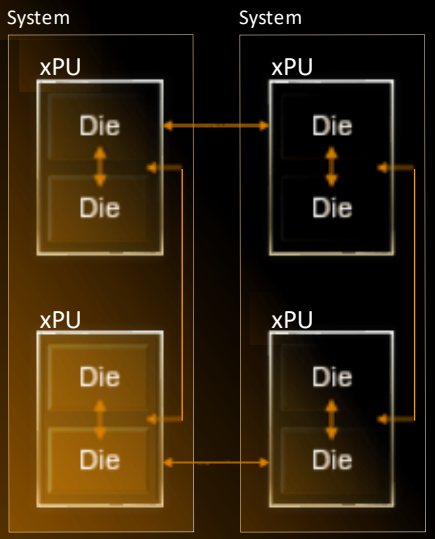

TECHNOLOGY
- UCIe
- Mlink

## ON BOARD
Chip-to-chip interconnect




TECHNOLOGY
- High-Speed SerDes (PCIe)
- uLED

## OFF BOARD
Board-to-board interconnect




TECHNOLOGY
- High-Speed SerDes (Ethernet)
- NPC/CPC Connectors
- Co-Package Optics


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# Advanced Packaging Technology Innovations

Critical for achieving larger integration




2.5D

<10,000 Sq. mm Si




3.5D

10,000-20,000 Sq. mm Si

- MediaTek's investments drive advanced packaging solutions to enable large complex heterogeneous integration.
- Advanced power delivery technologies (IVR, IPD) deliver higher power density and efficiency.
- System technology co-optimization (STCO) capabilities across Power Delivery, Thermals, Performance, and Packaging.

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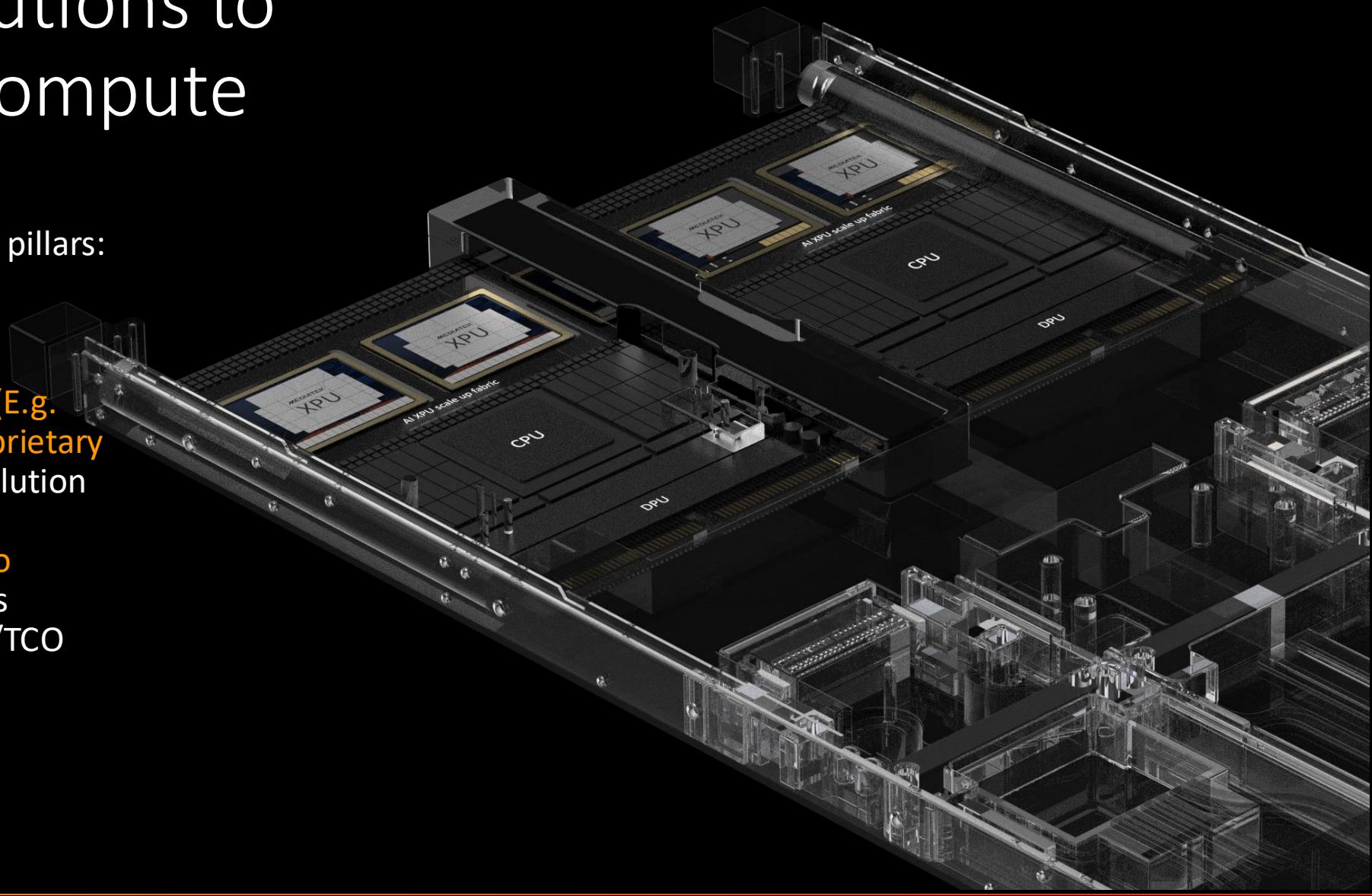
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# MediaTek Solutions to Scale Cloud Compute

Co-optimization across three pillars:
Compute, Scale-up, and
Scale-out Interconnect

Supports industry standard (E.g. UALink, ESUN, UEC) and proprietary interconnect (E.g. NVLink) solution

Heterogeneous integration to
enable new system use-cases
with improved performance/TCO




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# The Rack

## Building blocks of data centers

The de facto unit of compute consumption

Greater value through hardware/software vertical integration for Cloud AI and enterprise customer

Power, thermals and reliability dictate the performance

Effective monetization requires optimization of rack across different usages

**Perf/TCO and Reliability at scale** are critical metrics to achieve best-in-class data center efficiency




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# Strategic Partnerships with Industry Leaders

tsmc

EARLY TECHNOLOGY ENABLEMENT

- Advanced Nodes | DTCO CPO | SOW
- Early DTCO/STCO and 3DBlock partner
- Our collaboration has yielded worldclass D0 and capacity allocations

NVIDIA

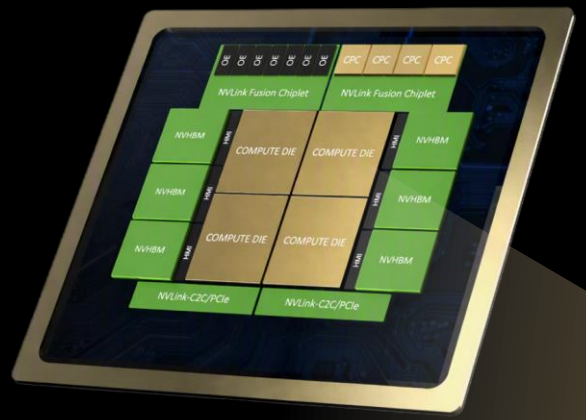
PRODUCT CO-DEVELOPMENT

- Automotive
- IoT
- AI Supercomputer
- Data Center
- Compute




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# MediaTek Rack Solutions




**ASIC Shell w/ Customer IP**
NVLink C2C Chiplet in MediaTek ASIC




**ASIC Shell w/ Customer IP**
PCIe/Ethernet in MediaTek ASIC



Leadership Compute Tray & Scale-Up

MediaTek ASIC Compute Tray and NVSwitch Tray in rack.

MediaTek ASIC OCP compute tray with Ethernet Interconnect and Ethernet Switch partners



Co-engineer custom rack solutions for leadership performance and power

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# The Value of MediaTek

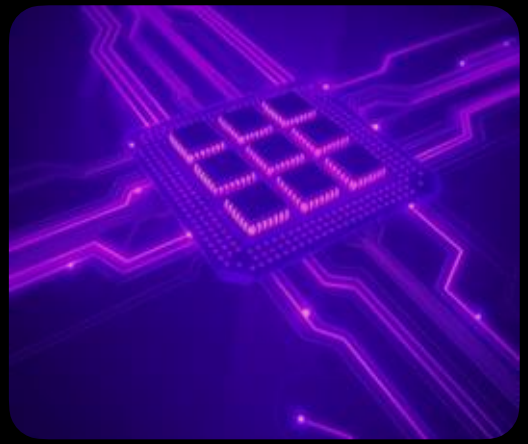
## Global Scale



### TECHNOLOGY LEADERSHIP

Process, Packaging,
Power, Connectivity

## Technology Optimization



### STRONG IP PORTFOLIO

SerDes, Optical,

High Speed I/O,
Die to Die Interconnect, Memory



### COLLABORATIVE ECOSYSTEM

Partnerships & Global Supply Chain

TSMC, NVIDIA, Intel,
SK Hynix, Micron, Samsung

## Relentless Execution



### STRATEGIC ENGAGEMENT MODEL

Fast Time to Market

Flexibility Across the
Technology Lifecycle

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# Sustaining the Next Decade of AI Infrastructure Growth

1. **Co-Optimize across the stack**
   Compute, memory, interconnect, and packaging - one roadmap.

2. **Support Open & Standards-based ecosystems**
   **E.g.** ESUN, UAL, UEC, NVLink Fusion , and OCP

3. **Efficiency at scale as the scoreboard**
   Perf/Watt and Perf/TCO — not peak FLOPs




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