Open Rack-Scale Optical Infrastructure for AI Scale-Up with Co-Packaged Optics

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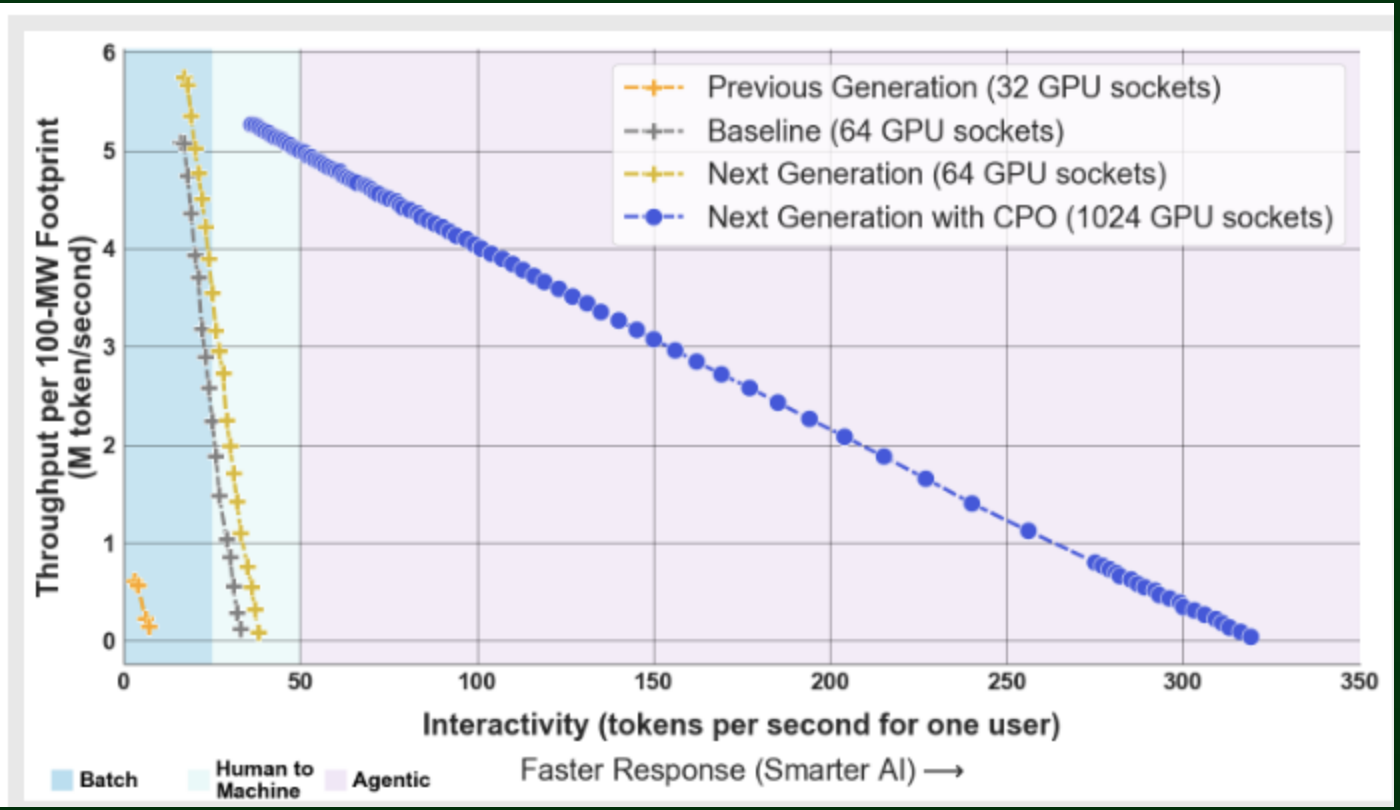
OCP FUTURE TECHNOLOGIES SYMPOSIUM

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San Jose, California

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Bigger models demand better efficiency, not just more ASICs (xPUs)

The scale-up domain size directly shapes tokens/sec/cluster



Why this matters

Larger models

need larger scale-up domains to stay efficient

Tokens/sec/cluster

is the metric that actually matters at fleet scale

1024-ASIC Scale-Up Pod

projects ~10x higher system performance vs. the smallest evaluated config

Communication-bound

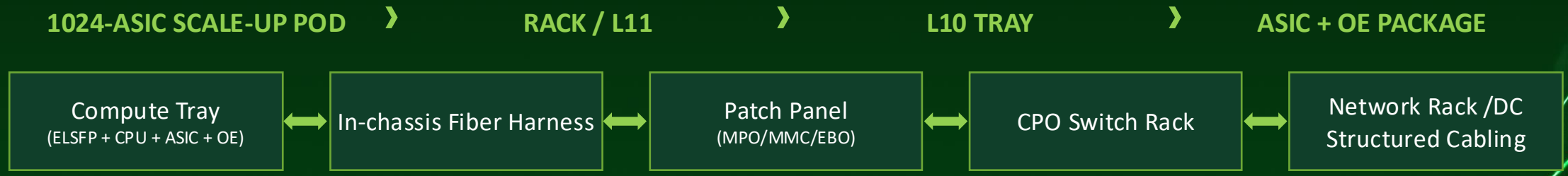
workloads benefit most from expanding scale-up reach across multi-racks

This is why we design top-down: start from the 1024-ASIC target, then work down through rack, tray, fiber, and multi-chip package.

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Integration Levels and Design Considerations

We drill top-down: from the 1024-ASIC scale-up pod to the ASIC + OE package



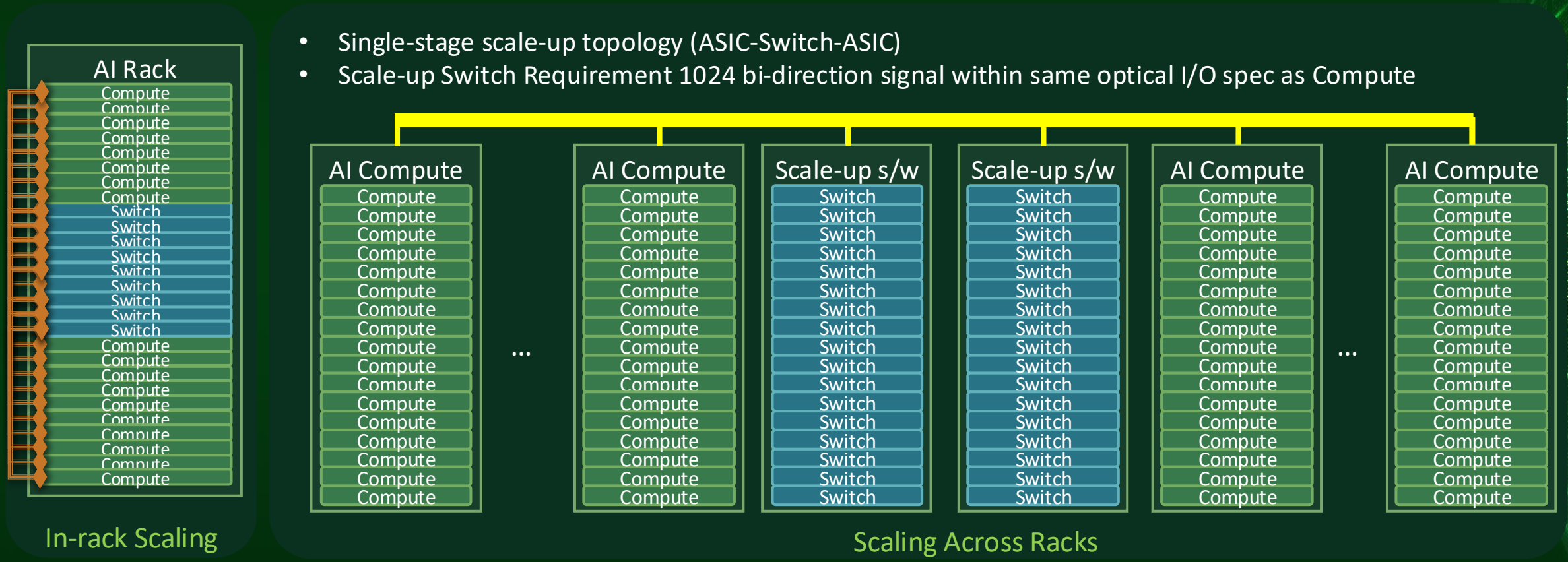
1	**Two thermal domains**	**ASIC/OE** heat vs. **ELSFP** temperature window
2	**Front-panel consumable**	ELSFP must remain hot-pluggable and reachable, reserved space for NIC, SSD, and BMC
3	**Fiber as structure**	**Bend radius**, PM Fiber orientation, service loops
4	**Fragmented power tree**	48 V/±400V/800V rear input versus 3.3 V at the front
5	**Cross-supplier test boundary**	Loss can originate across multiple ownership points

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Level 1 — The 1024 Scale-Up Pod

Translate high-density CPO I/O into structured rack-to-rack infrastructure

1024-ASIC SCALE-UP POD › RACK / L11 › L10 TRAY › ASIC + OE PACKAGE



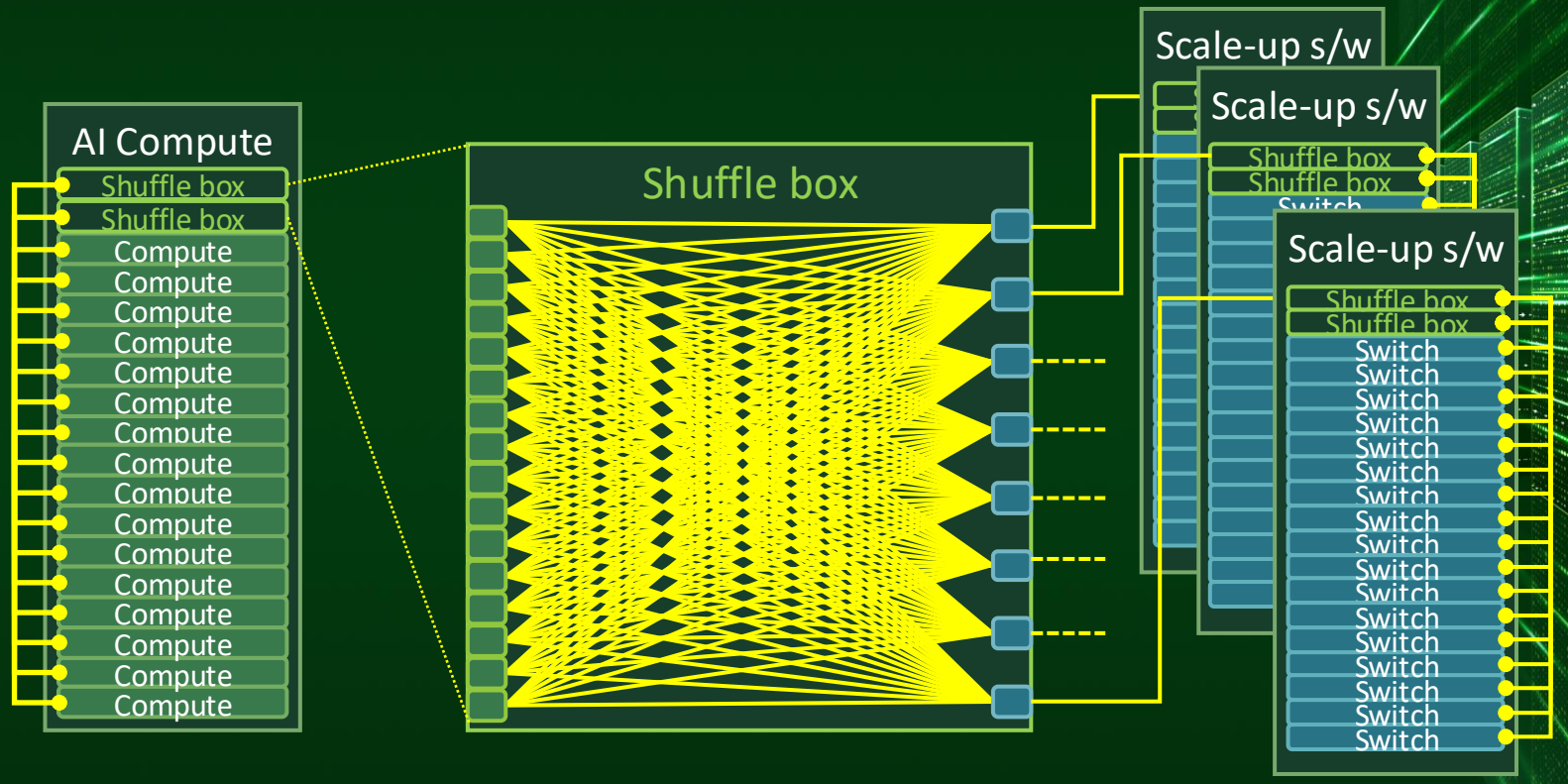
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Level 2 — Fiber Routing Architecture

Organize optical endpoints through a hierarchical physical structure

1024-ASIC SCALE-UP POD › **RACK / L11** › L10 TRAY › ASIC + OE PACKAGE

- **Every ASIC** connects to **every scale-up switch**
- Each compute rack houses **32 × 1OU compute trays**
- All ASIC scale-up fibers connect to the **in-rack shuffle box**
- **At least one fiber pair** provides a bidirectional link to each switch rack
- **32 × 1OU scale-up switch trays** and a shuffle bus per switch rack



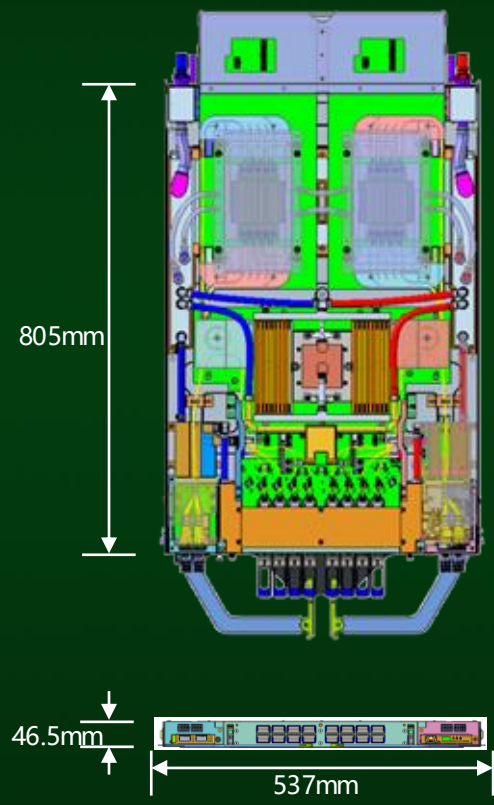
Each compute rack connects to every switch rack

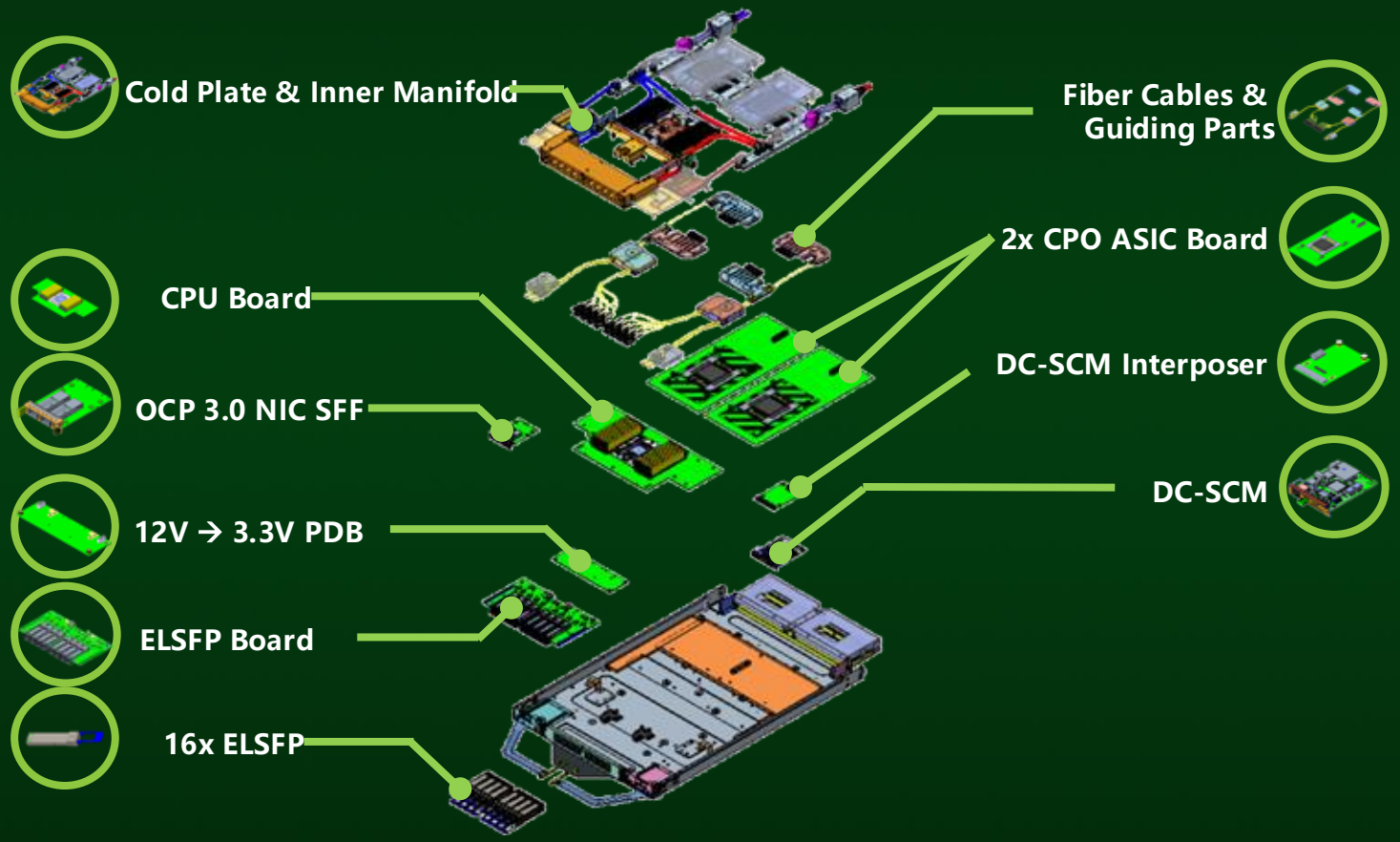
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Level 3 — The L10 Layout & Design

Tray design integrates optics, power, electrical signals, cooling, and control

1024-ASIC SCALE-UP POD › RACK / L11 › **L10 TRAY** › ASIC + OE PACKAGE





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Level 4 — Inside the Accelerator Multi-Chip Package

Optical conversion moves into the package, along with thermal and repair consequences

1024-ASIC SCALE-UP POD › RACK / L11 › L10 TRAY › **ASIC + OE PACKAGE**

8 Optical Engines on-package
- → High bandwidth, high radix
- → Low latency
- → Low end-to-end energy

I/O protocol converter chiplets
- → UCIe-A to UCIe-S
- → Scale-up protocol endpoint

8 HBM Stacks
- → Memory bandwidth expansion





- → Multi-rack scale-up connectivity
- → 200+ Tbps scale-up bandwidth per accelerator
- → Hundreds of scale-up links per accelerator
- → Microring architecture, OCI-MSA Optical PHY
- → UCIe-S die-to-die interface

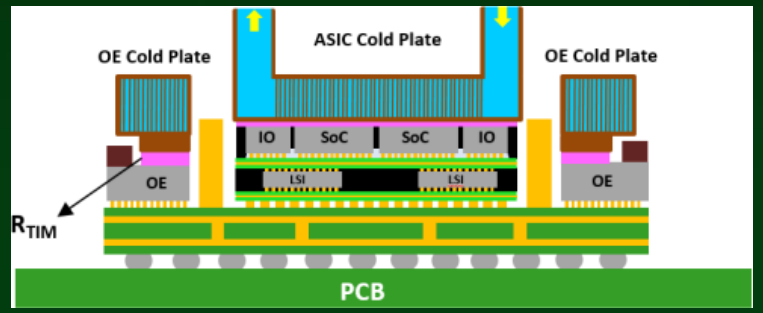
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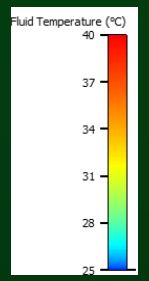
Level 4 — Package Thermal Simulation

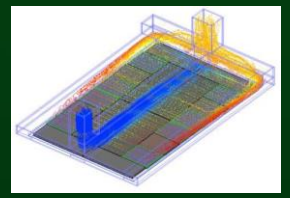
Thermal cross-talk onto the optical engines is negligible

1024-ASIC SCALE-UP POD › **RACK / L11** › **L10 TRAY** › **ASIC + OE PACKAGE**

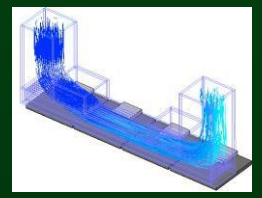
◆ Use Impingement type Cold plate thermal solution





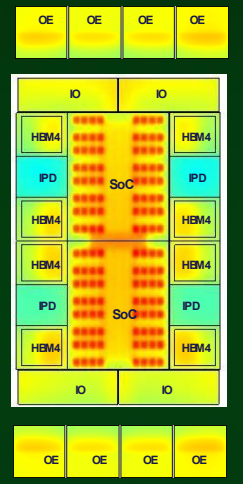


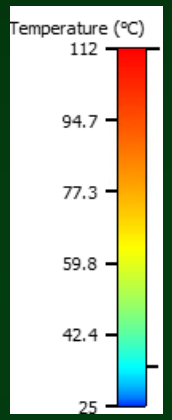
ASIC Cold plate
Flow rate: 4.5 LPM
Pressure drop: 11.2 kPa



OE Cold plate
Flow rate: 4.5 LPM
Pressure drop: 18.8 kPa

Active Surface Temperature
(Flow rate = 4.5 LPM)





Ta = 25 (°C) , R-TIM=5.2 (W/mK)		
Item	**Spec Tj (°C)**	**Flow rate 4.5 LPM Tj-max (°C)**
SoC	125	112
HBM4	95	75.4
IO	125	59.9
OE	100	69.8

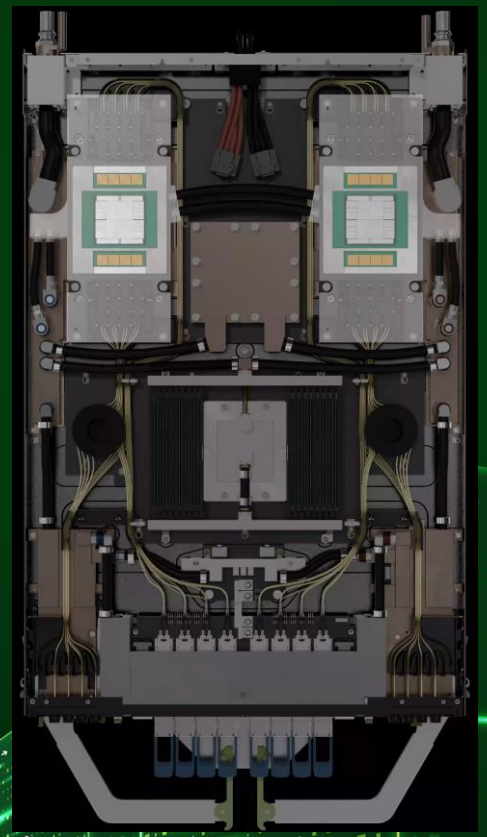
The impingement cold plate can meet the spec

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Call to Action

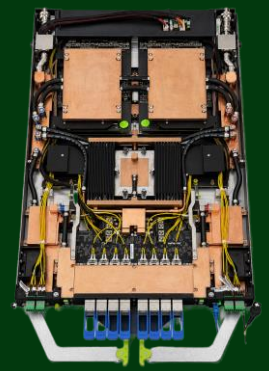
How do we deploy Short Reach Optical Interconnects for scale-up?

1. Common Physical Interface
2. Deployment and validation practices
3. System telemetry
4. Reference rack design



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Thank You!



LIVE CPO TRAY at #C74

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