Powering the AI Revolution: Navigating the 800V-to-Chip Frontier

Teng Long

Professor,

LITEON-EPIC

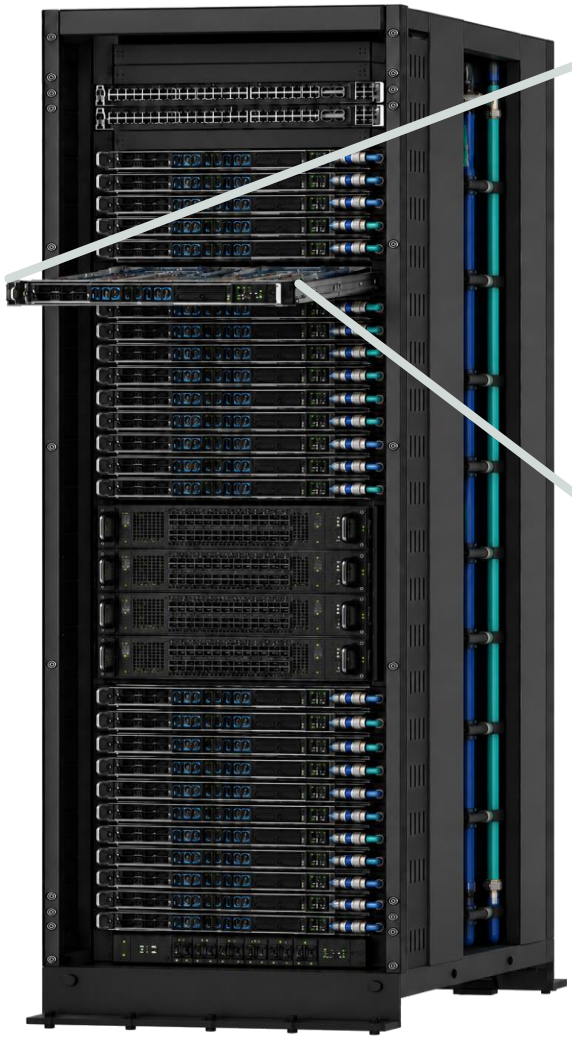
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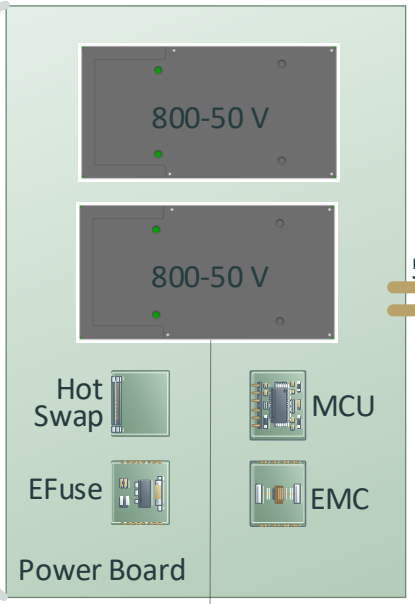


OCP FUTURE TECHNOLOGIES SYMPOSIUM

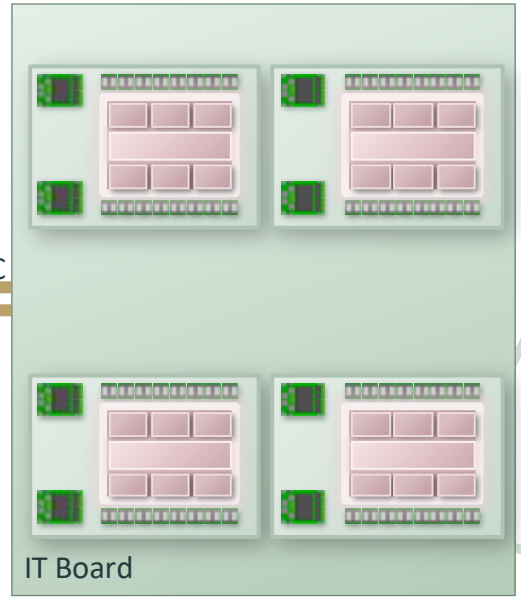
October 14, 2026
San Jose, California

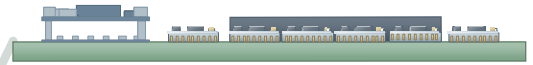
800V DC Rack-to-Chip Power Delivery

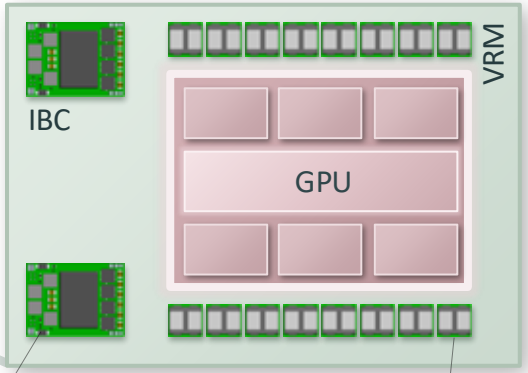


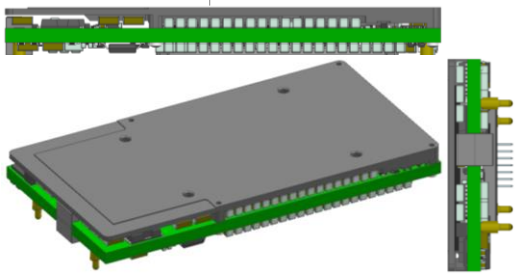


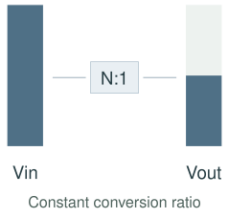
50 V DC

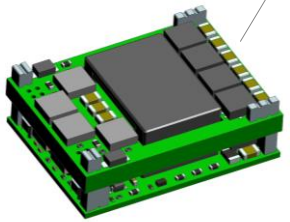


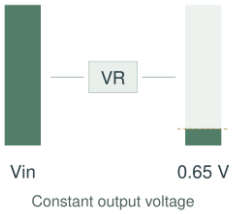


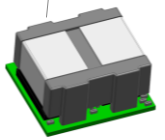




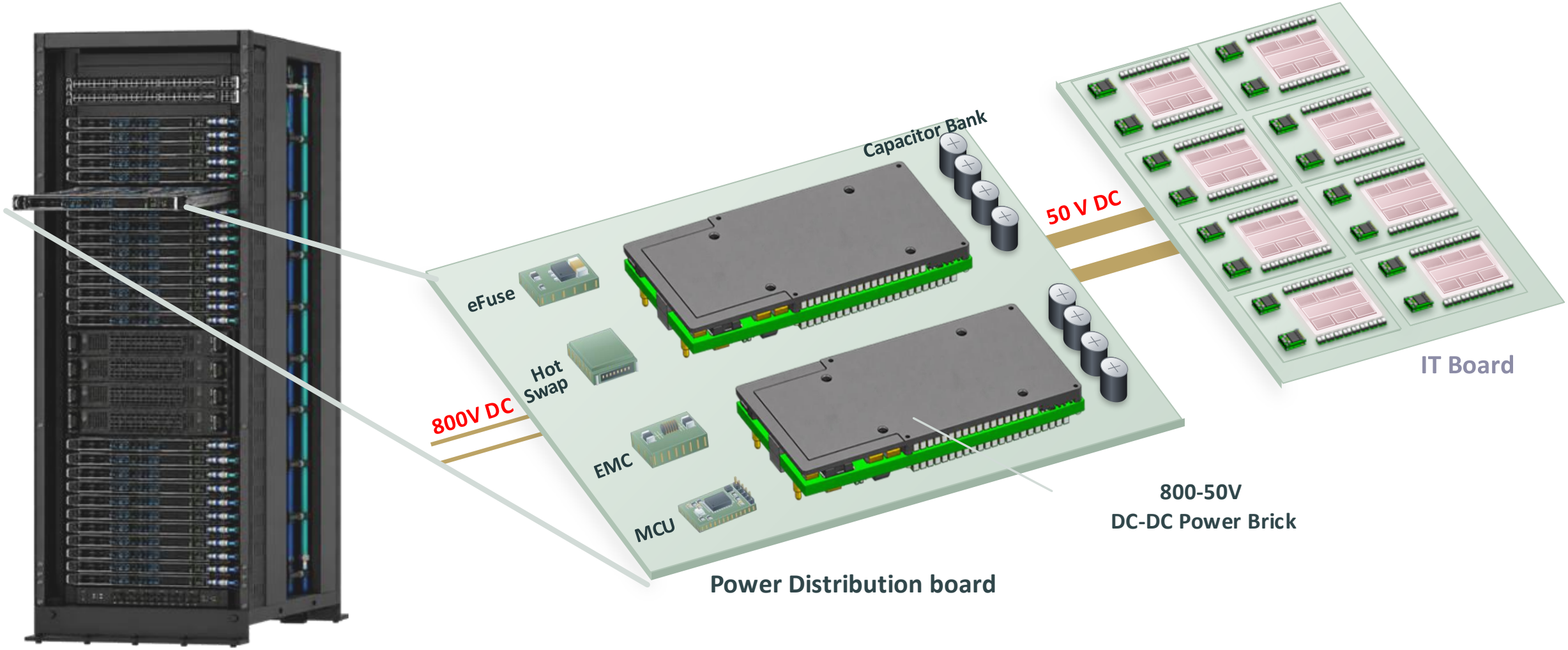




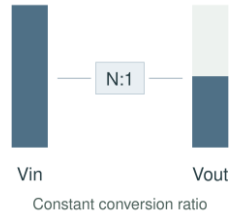


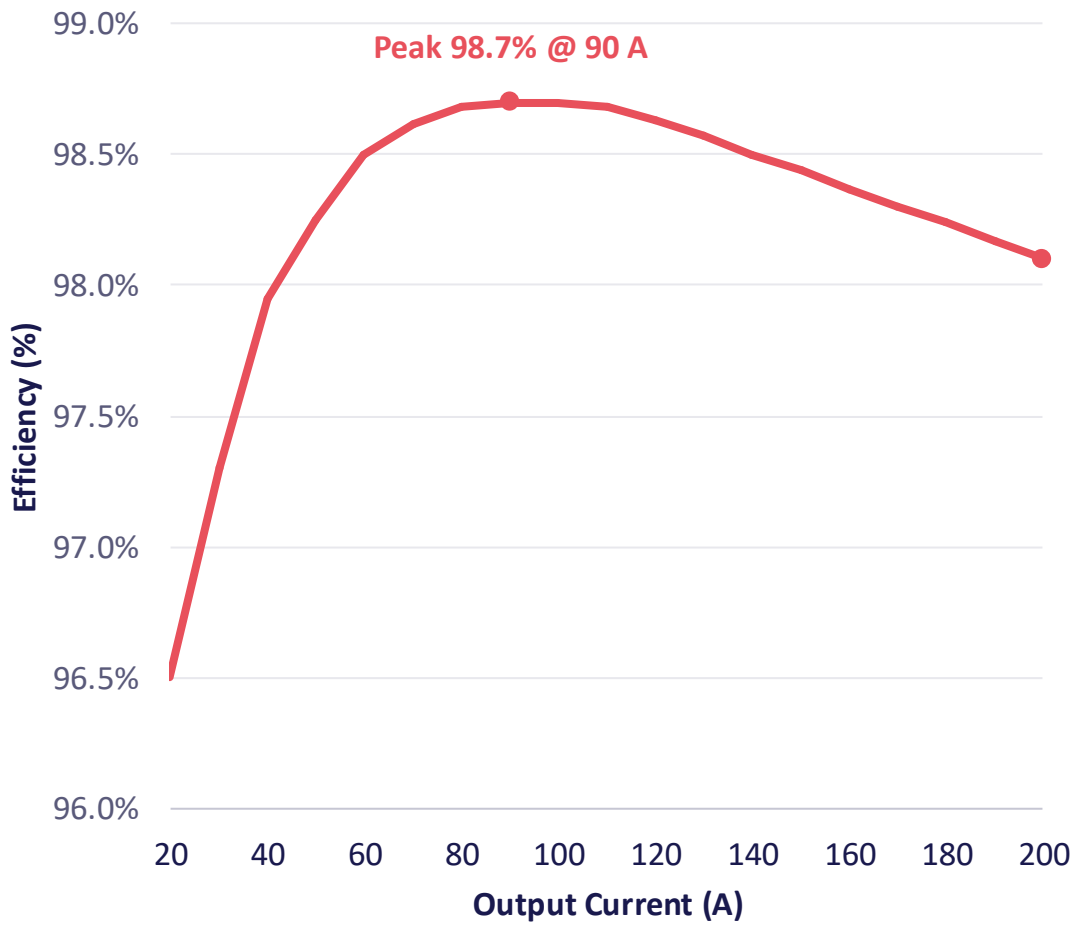


Power Distribution board (PDB) 800-50V



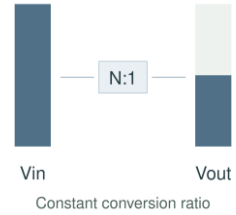
800-50V DC-DC Power Brick (Full-Brick 10kW)

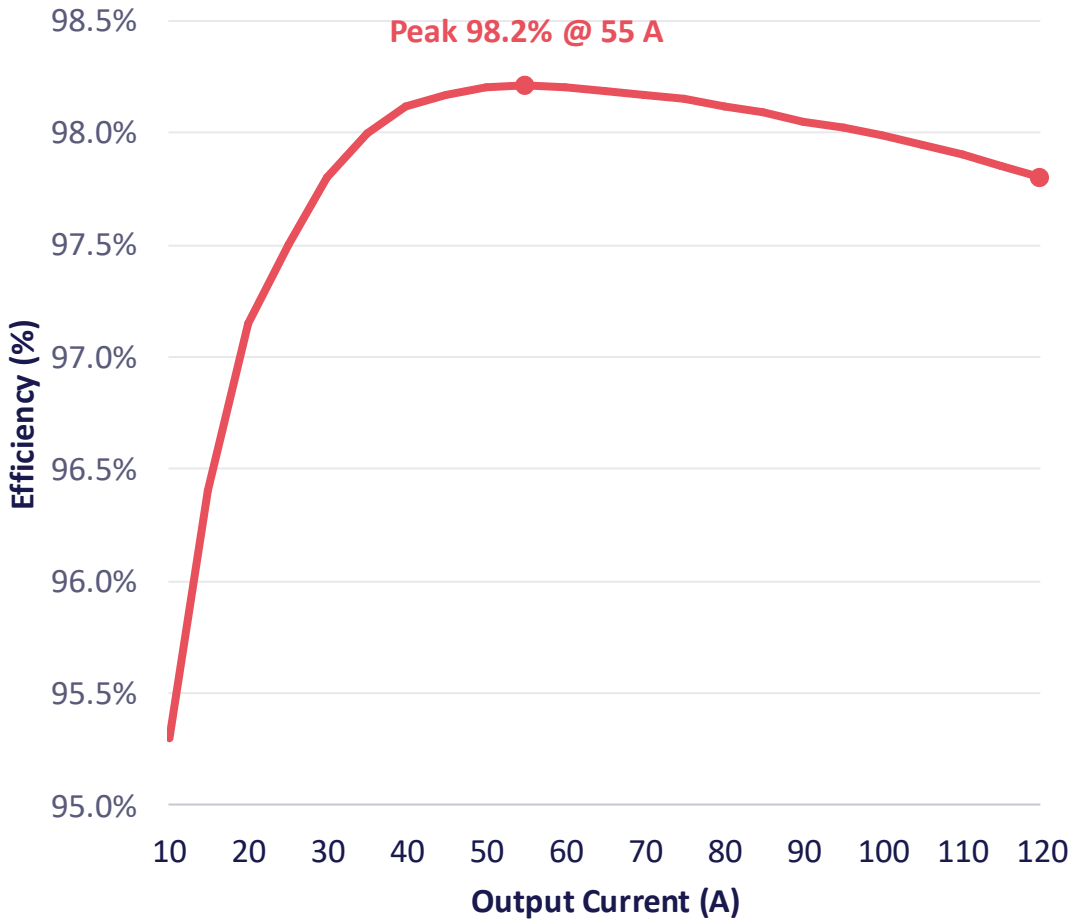




- Rating: **10kW full-brick**
- Power density: 1522 W/in^3
- Function: High Voltage Bus Converter (HVBC 800-50V)
- Efficiency: **peak 98.7%, full-load 98.1%**
- **2027: 12kW**

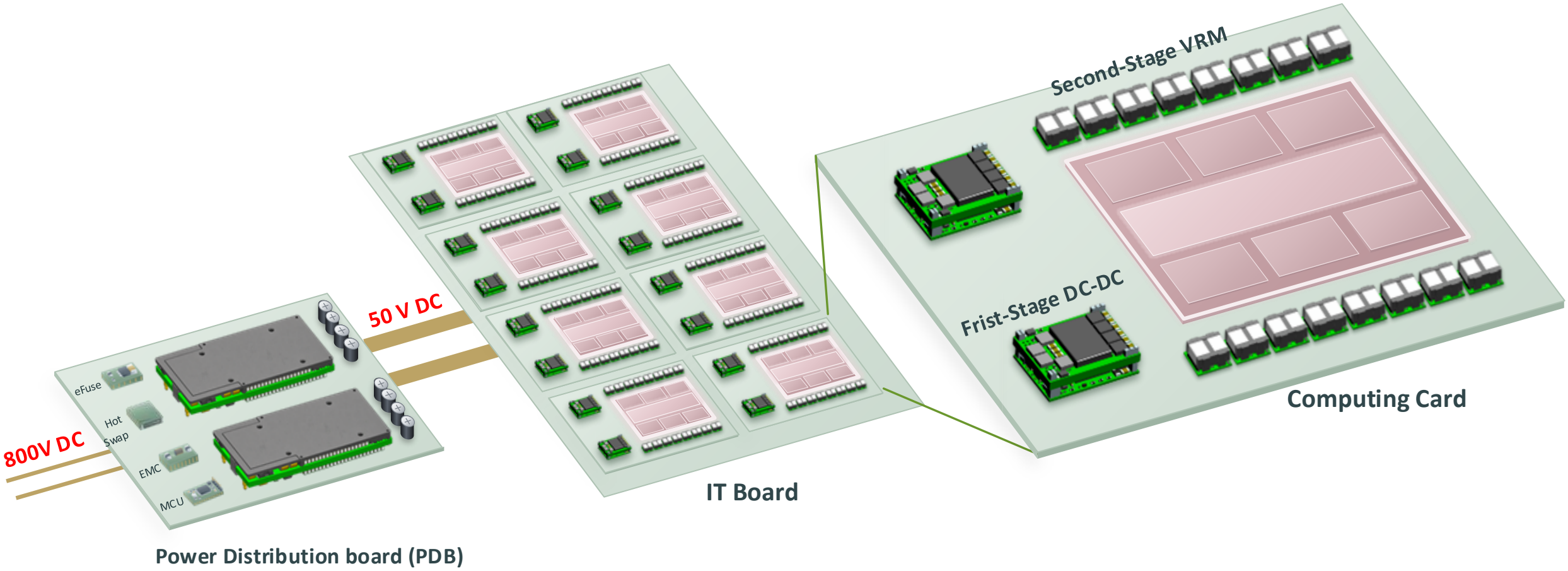
800-50V DC-DC Power Brick (Half-Brick 6kW)



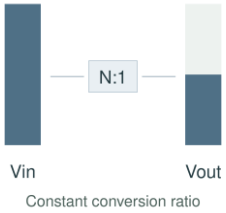


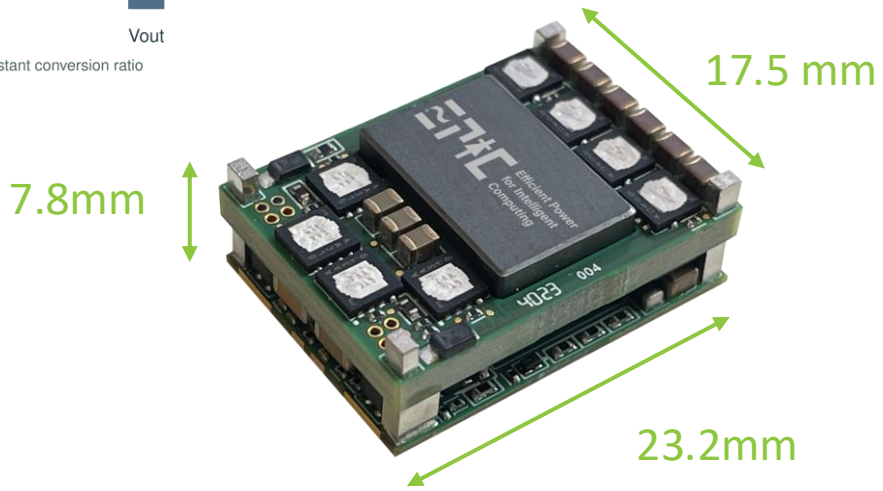
- Rating: 6kW half-brick
- Power density: 1746 W/in^3
- Function: High Voltage Bus Converter (HVBC 800-50V)
- Efficiency: **peak 98.2%, full-load 97.8%**

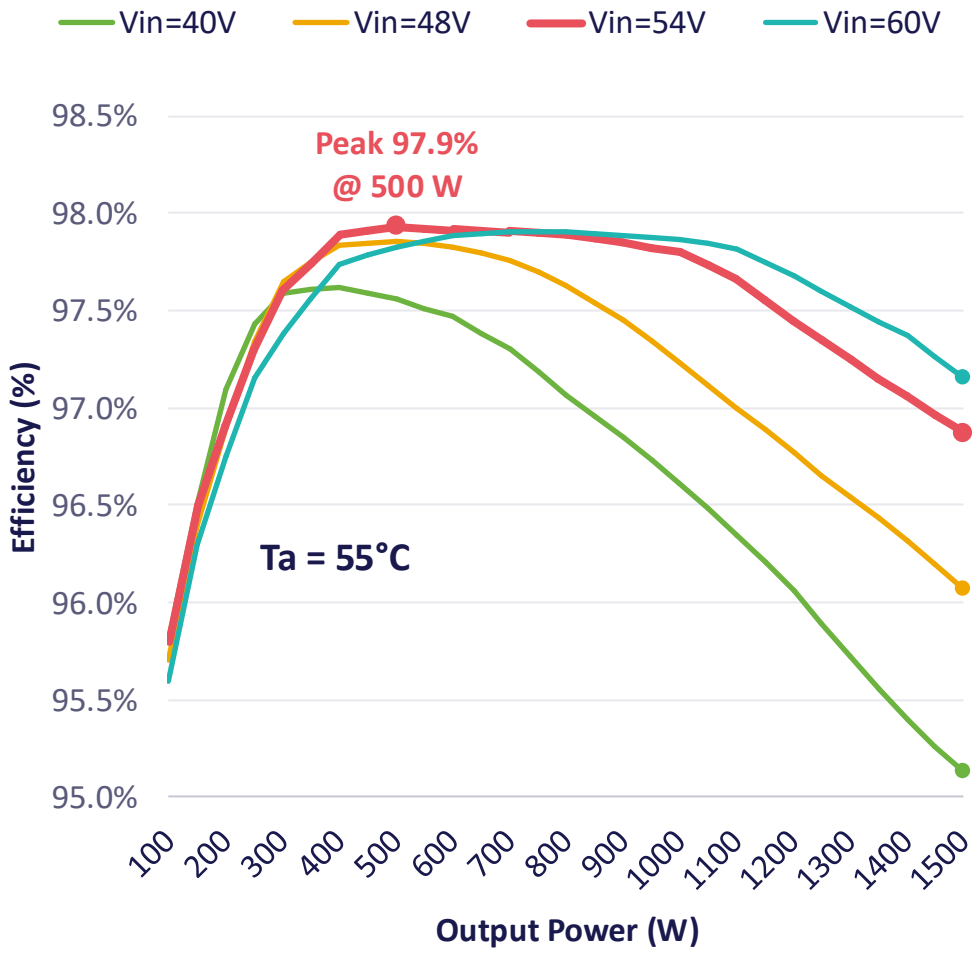
IT Board (50V) 2-Stage On-board Power Solution



First-Stage DC-DC converter for 12V Bus

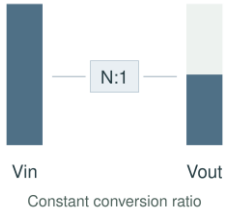


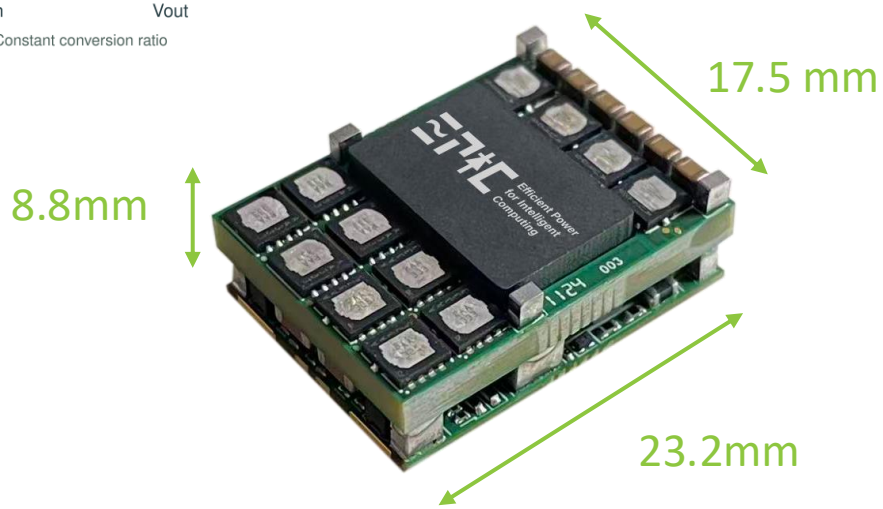


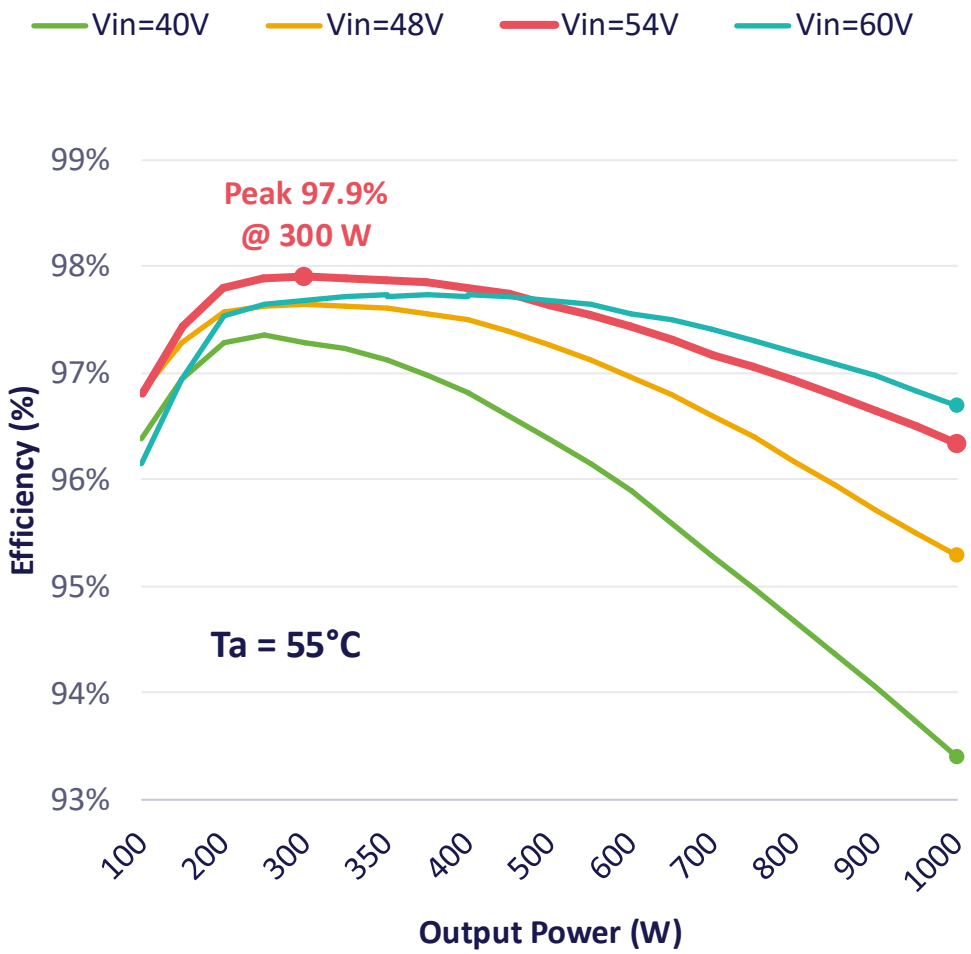


- **OCP compliance and qualification**
- Mature *LLC* topology varient, In: 40-60V, Out: 10-15V
- Rating: **1500W**, Size: 23.2x17.5x7.8 mm
- Power density: 7762 W/in^3
- Efficiency@54V input: **peak 97.9%, full-load 96.9%**

First-Stage DC-DC converter for 6V Bus

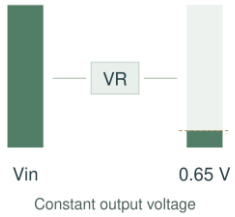


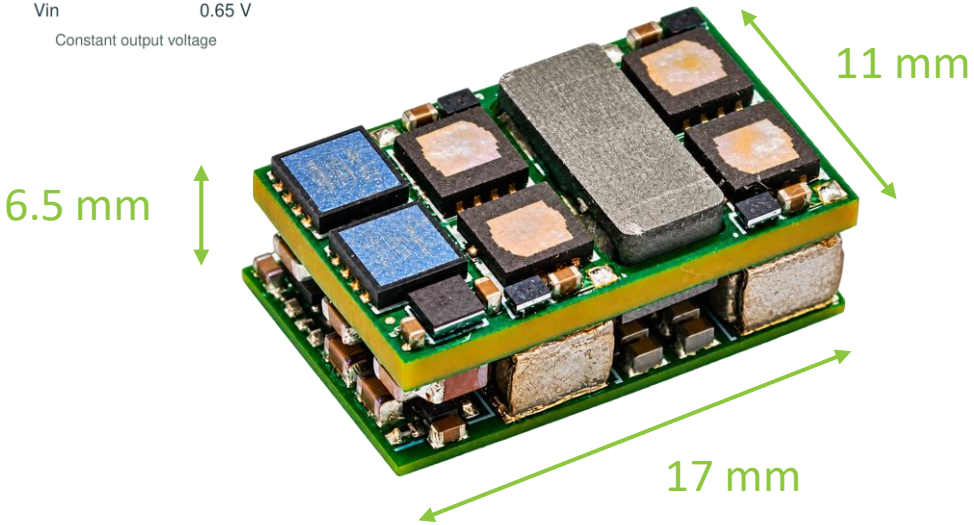


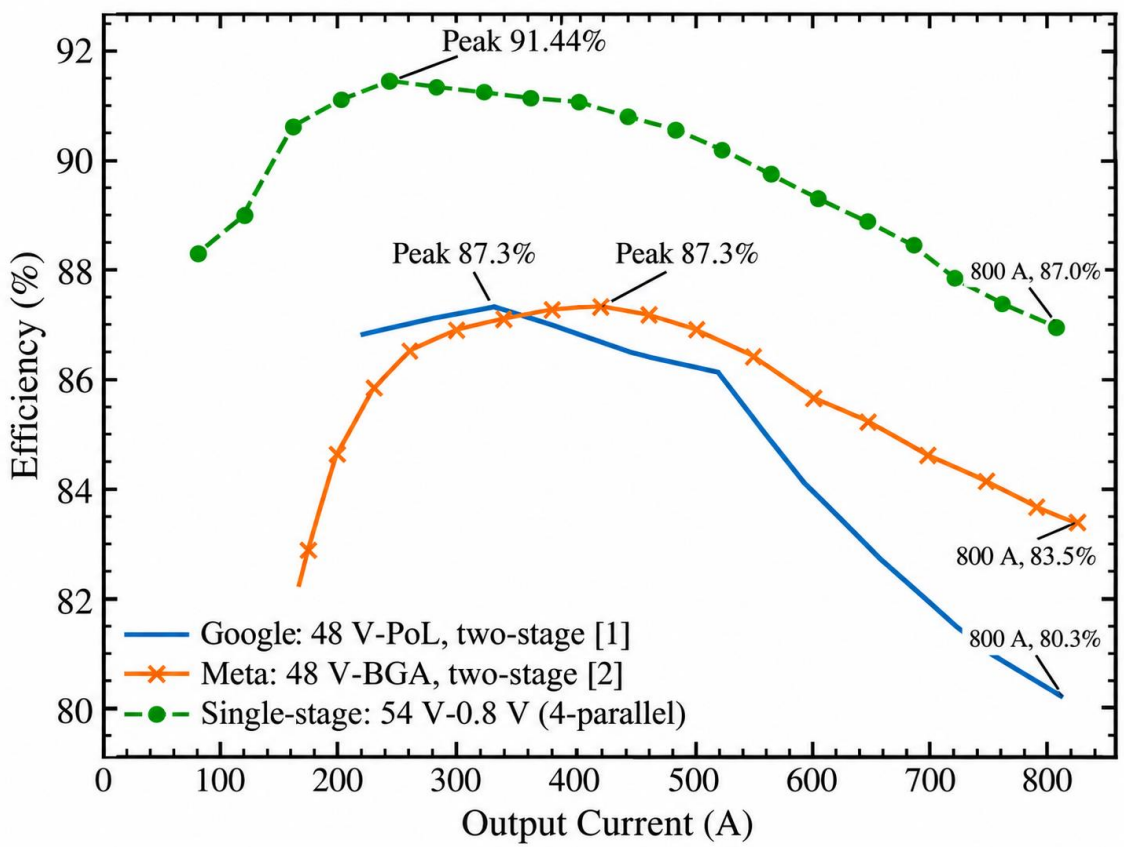


- **OCP compliance and qualification**
- Mature *LLC* topology variant, In: 40-60V, Out: 5-7.5V
- Rating: **1000W**, Size: 23.2x17.5x8.8 mm
- Power density: **4587 W/in^3**
- Efficiency@54V input: **peak 97.9%, full-load 96.6%**

50-0.8V Single-Stage Voltage Regulator Module





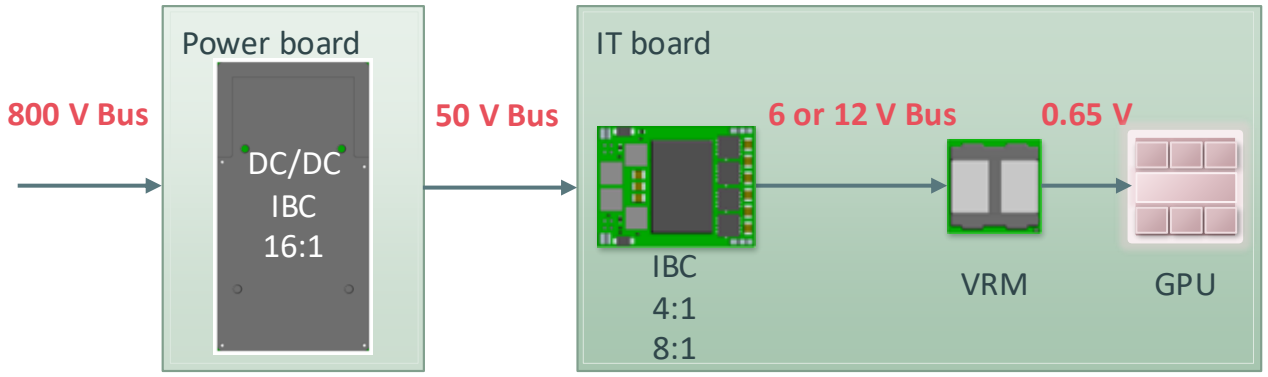


- Rating: 240A (single), regulated, 4 in parallel for 800A
- Current density: **1.28A/mm^2**
- Function: 54-0.8 **regulated and adjustable output voltage**
- Efficiency: **peak 91.4%,** full-load 87%
- **Significant higher efficiency and form factor than 2-stage**

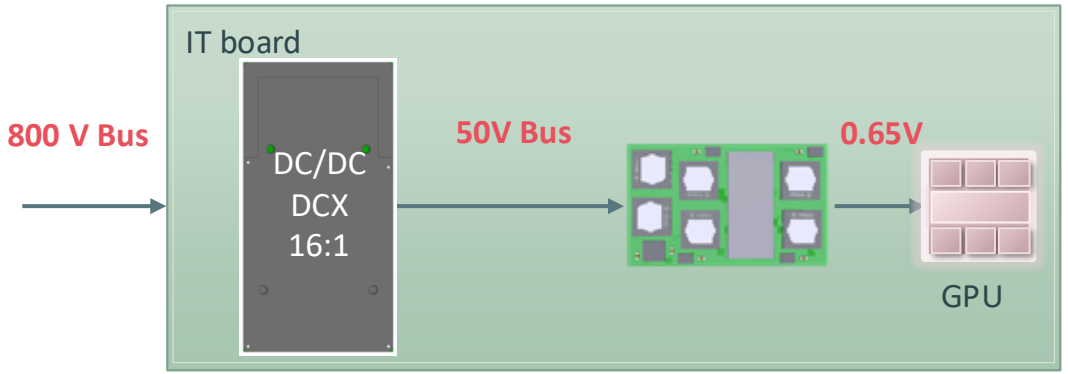
[1] H. Gan et al., "Vertical Power Delivery for 1000 Amps Machine Learning ASICs," APEC 2024.
[2] S. Zou et al., "Vertical Power Delivery Module Design and Integration for 850A AI ASIC," APEC 2026.

800 V DC Power Delivery Architecture Trends

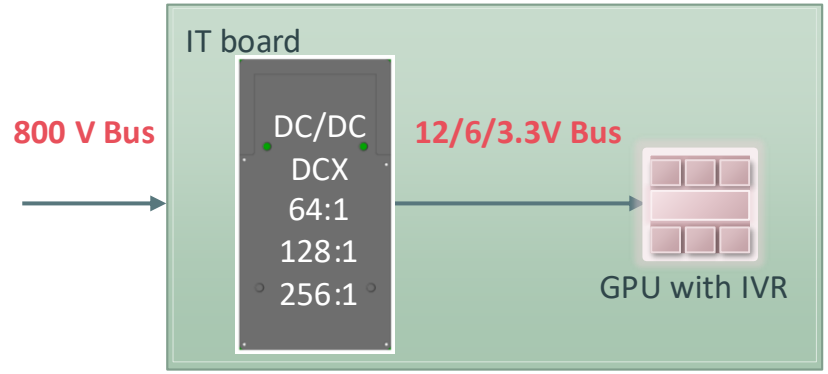
Baseline: two-tray, 3 stages from 800V to core



Trend 1: one-tray, two stages from 800V



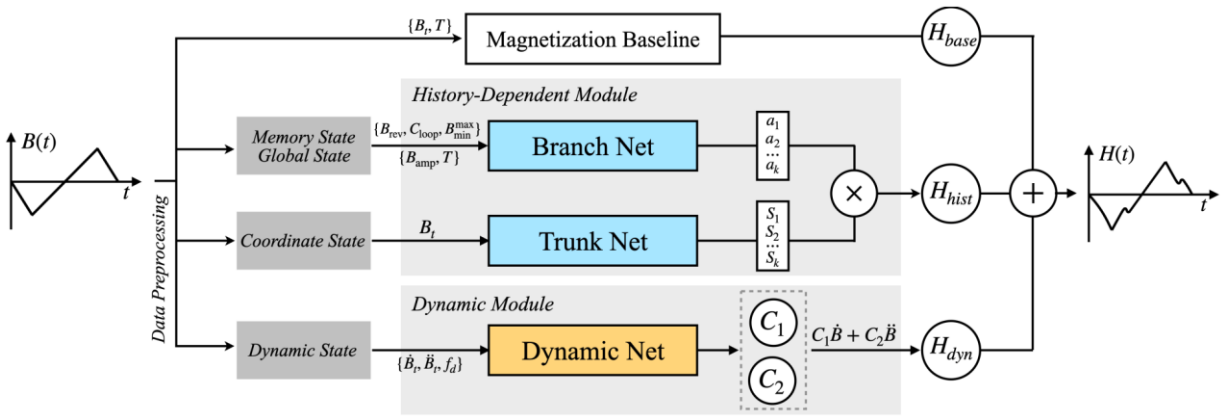
Trend 2: one-tray, single stage using IVR at core

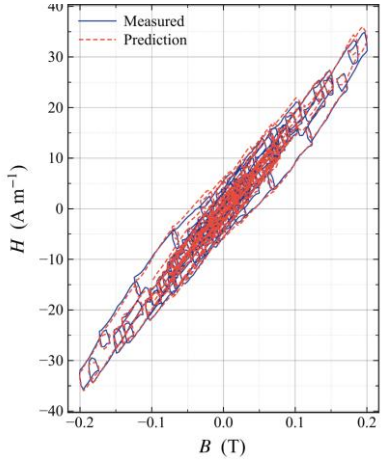


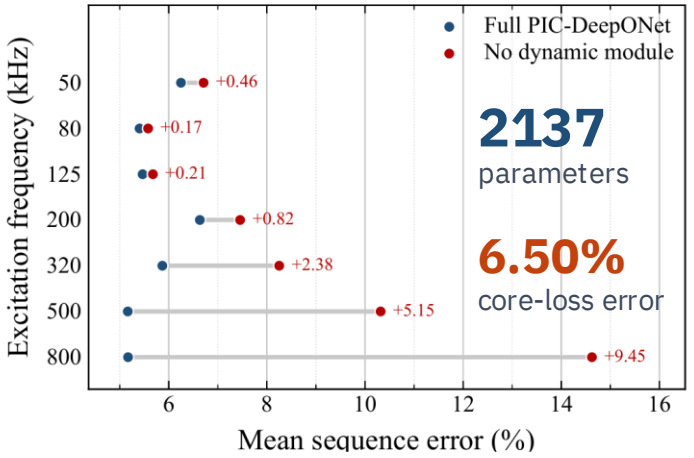
IVR: Integrated Voltage Regulato

AI assisted high frequency planar transformer design

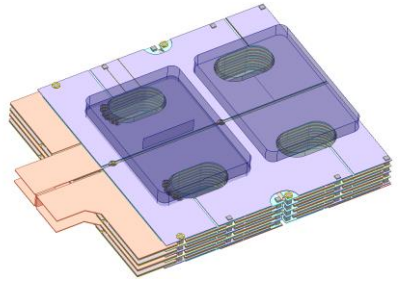
- **Non-autoregressive PIC-DeepONet for transient B–H hysteresis** ***H = baseline + history + dynamic,***

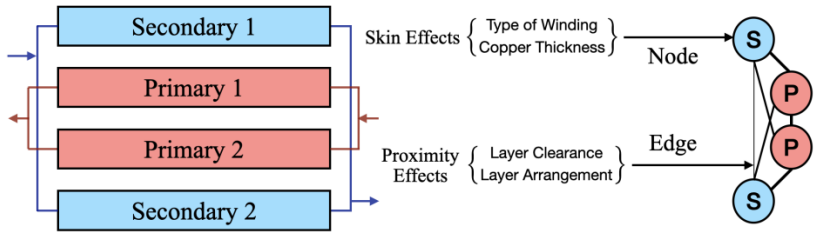


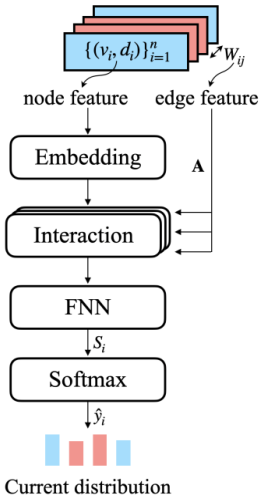


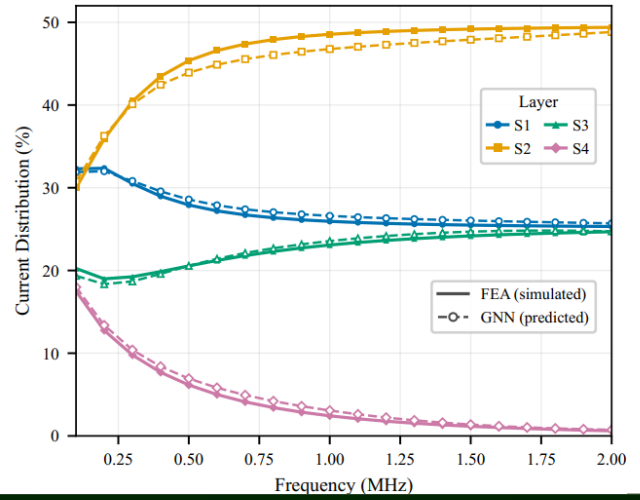


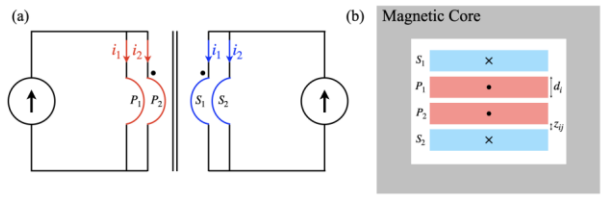
- **AI assisted planer transformer winding design: Graph Neural Network for PCB Layer Current Sharing**

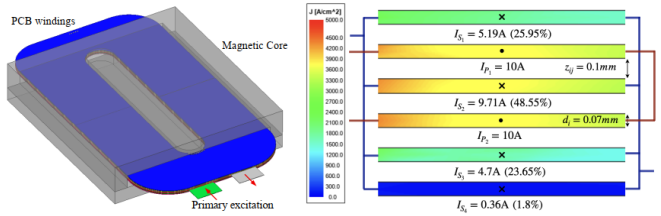




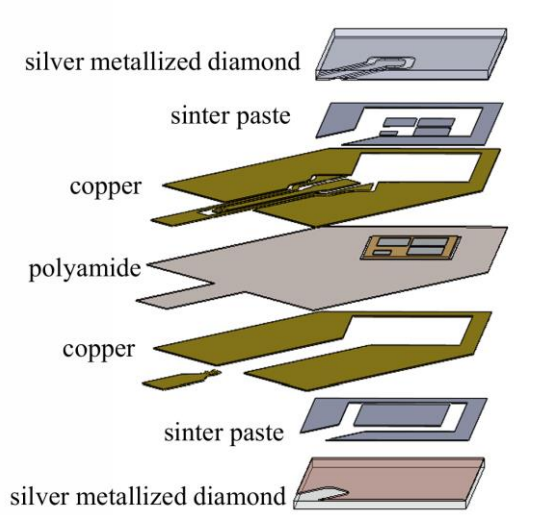


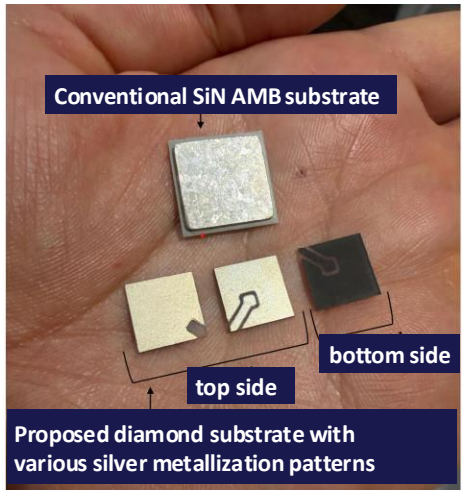


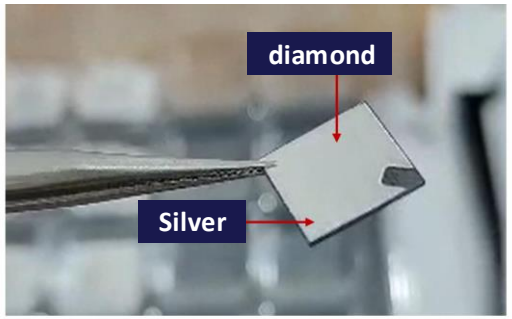




Advanced Packaging (Diamond substrate with Microchannel)



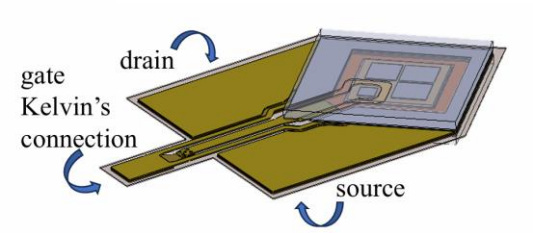


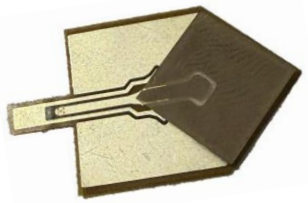


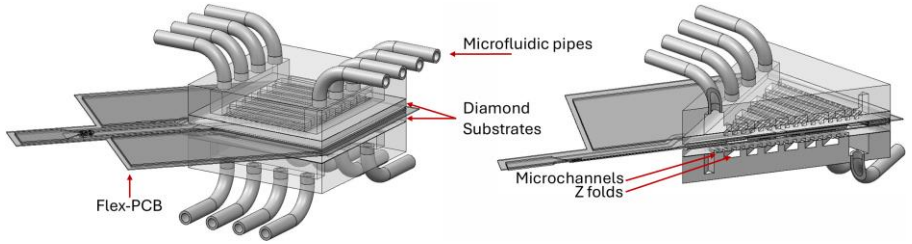
Top side

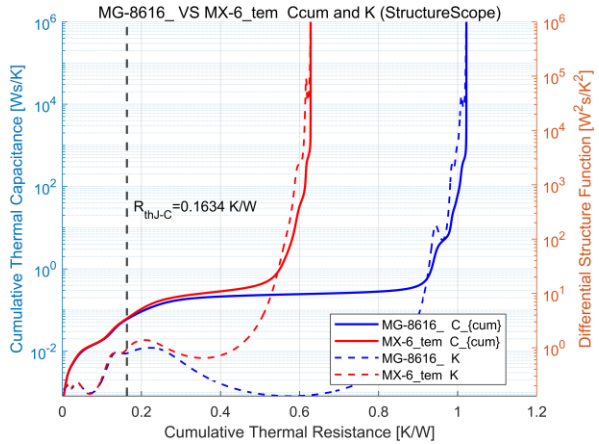


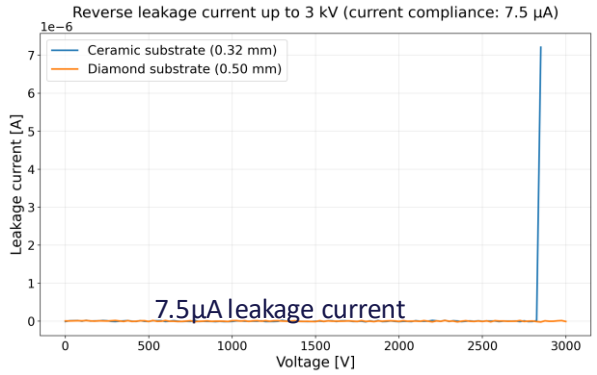
Bottom side











- Single crystalline PVD diamond
- Thin Ti (~10–50 nm) is annealed (≈500°C) to form TiC on diamond.
- Ag by PVD or plating to ~0.5–5 µm for high conductance with low stress.
- **Electrical isolation is demonstrated >3kV limit** (curve tracer limit).
- **Thermal Resistance: 0.16 C˚/W (Single side)** and **0.1 C˚/W (double side).**
- In collaboration with Cambridge Integration and Cambridge University.

OCP FUTURE TECHNOLOGIES SYMPOSIUM

October 14, 2026
San Jose, California

