

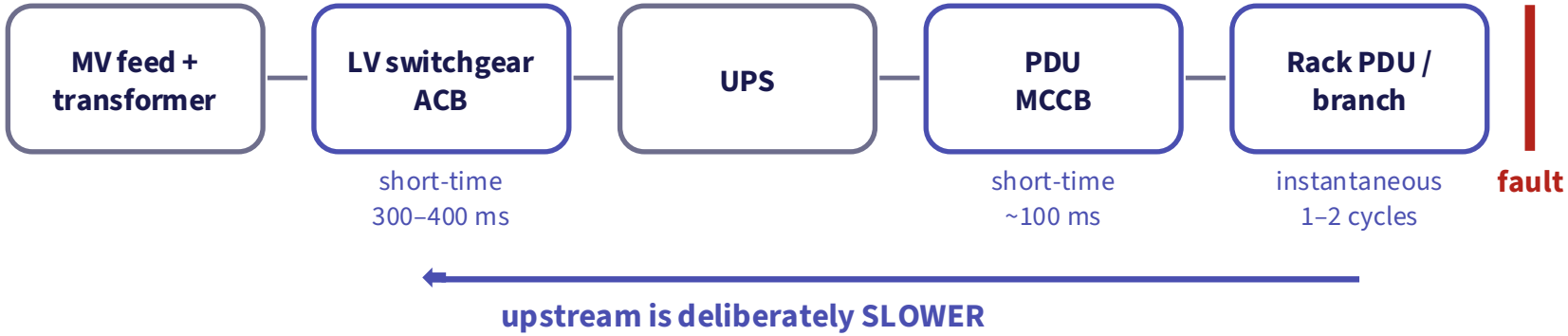
Solid-State Circuit Breaker (SSCB) and DC Fault Manager

Protection at 800 VDC is a system function, not a device function

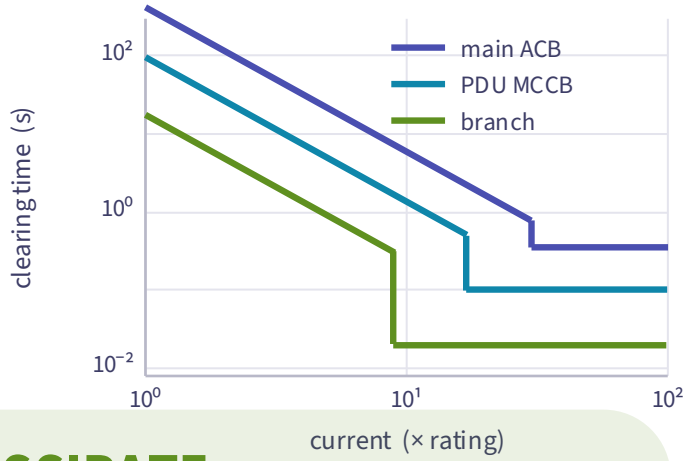
Ke Sun

VERTIV.

How the typical AC data center handles a fault today



curves must not overlap →
only the nearest device trips



WAIT

for the current zero

Every 8.3 ms the arc extinguishes itself. The breaker only has to withstand the recovery voltage.

DELAY

upstream, on purpose

Selectivity is bought with deliberate upstream delay — and ITIC lets IT load ride through a full 20 ms interruption.

DISSIPATE

in the arc

The fault energy goes into the arc. The designer's problem is arc-flash safety in cal/cm², not “where do the joules go”.

800 VDC revokes all three

~~WAIT~~

⬇

FORCE

the current to zero

~~DELAY~~

⬇

DETECT

and act inside microseconds

~~DISSIPATE~~

⬇

ABSORB

in a clamp, by design

AC spends time. 800 VDC spends joules.

OCP Diablo 400 v0.7.0 §8.1.3 specifies fuses and relays on the ±400 V output — the DC protection layer is where the specification is still being written.

SSCB Enables Advanced Fault Mgmt Strategy

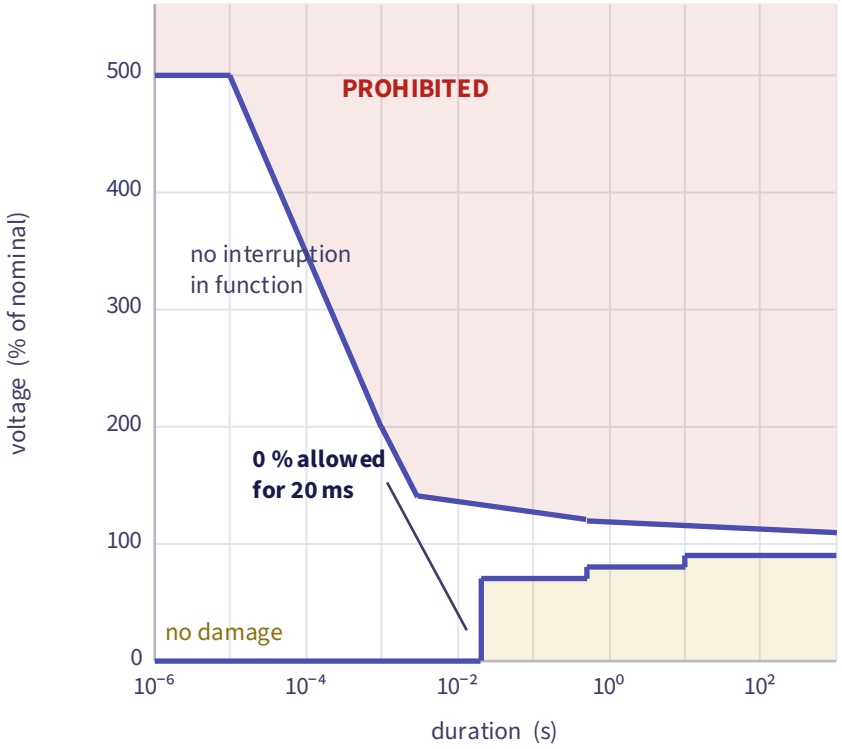
	Fuse	Mechanical DC breaker	Solid-state (SSCB)
Clearing time	ms-class, one-shot	ms-class	**tens of µs**
Limits current before the prospective peak	at extreme current	no	**yes, by design**
Switches on command, repeatedly	no — replace it	yes, wear-limited	**yes**
µs fault data + upstream interlock	none	none	**yes**
Where the fault energy goes	into the fuse arc	into the arc chute	**into a clamp, by design**

Diablo 400 §8.1.3 specifies fuses and relays today.

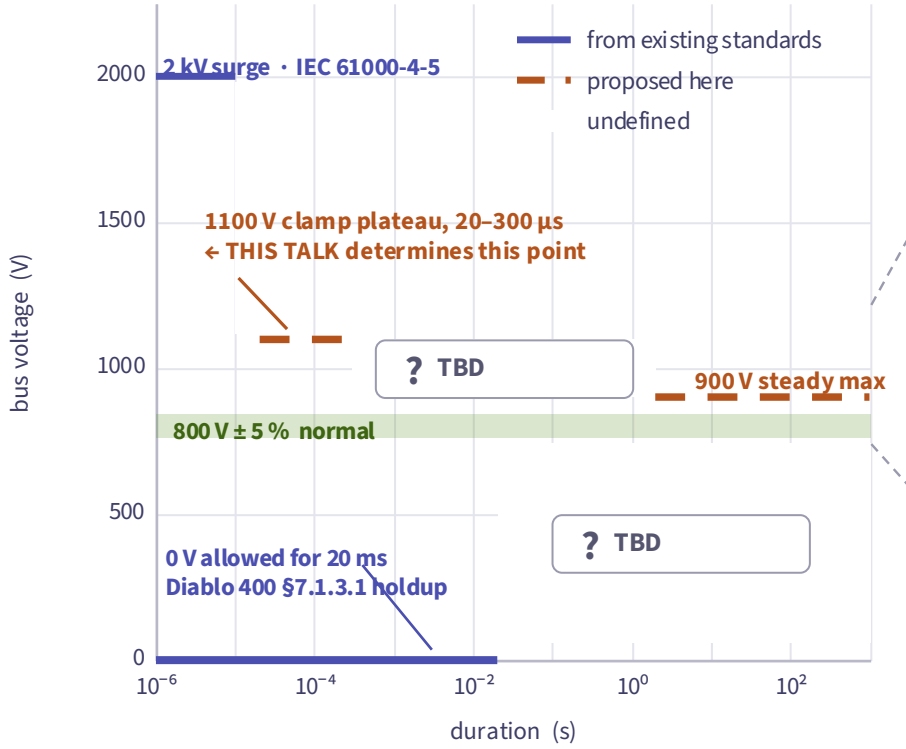
Choosing solid state is what creates the clamp-sizing problem.

DC power quality - "DC ITIC" curve

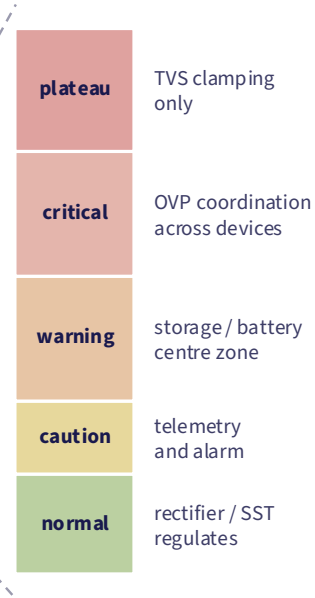
AC — ITIC / CBEMA, defined since 1996
every PSU spec is written against it



800 VDC — DC ITIC Curve

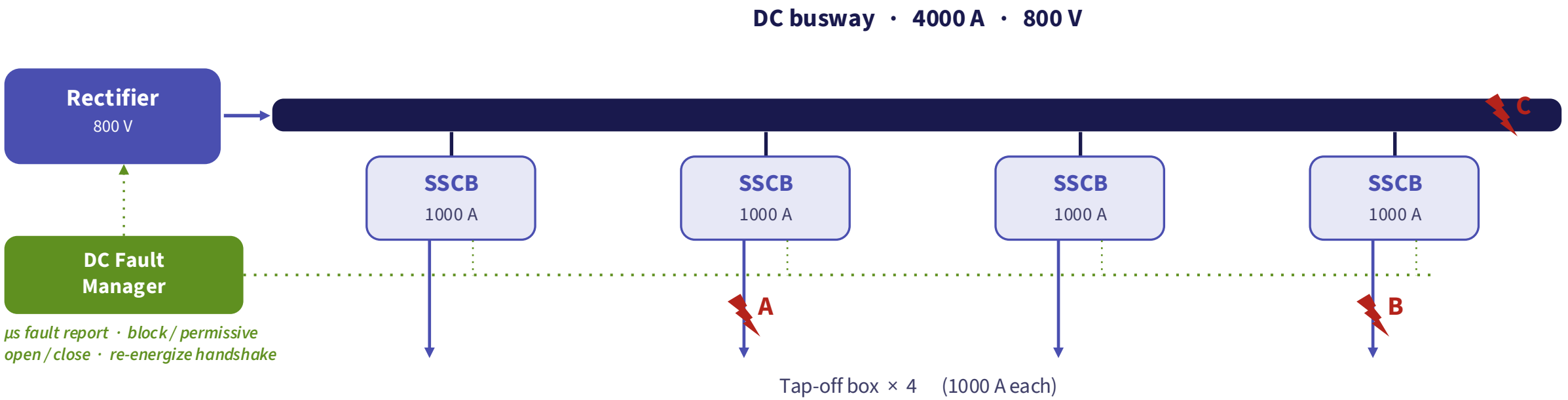


the slice, magnified
who acts in which band



Ref: OCP Data Center Facility - Low Voltage Direct Current Power Distribution V1.1.0, Power Quality

Where these breakers actually sit



A **Tap-off outlet**

B **Far tap-off outlet**

C **The busway itself**

Loop inductance scales with how much busway the fault current has to travel — of order 0.1–0.2 µH per metre for a grouped-copper sandwich busway, and several times that for cable.

Two roles in one fault

SSCB — the device
microseconds · local · no judgement

- Detect di/dt and I_peak locally — no time to ask anyone
- Force the current to zero and absorb the clamp energy
- Provide galvanic isolation, on command (UL 489I)
- Report a µs-resolution record of what it just saw

DC Fault Manager — the system
microseconds to seconds · sees the whole bus

- Decide which zone actually faulted, from several reports
- Block peers and upstream before they trip too
- Own the re-energization sequence with the rectifier
- Keep the health and wear state of every SSCB on the bus

Selectivity moves from the curve to the link

AC grades in time: 50–300 ms of deliberate upstream delay.
800 VDC at ~1 kA/µs: every SSCB on the bus sees the fault within a few µs — there is no delay left to grade with.

Fault	What the bus sees	What makes it selective
A tap-off outlet	Only that branch carries forward fault current	Local trip is already selective — the SSCB decides alone
B far tap-off	Same, but 10× the loop inductance → slower rise	Longer detection budget; same local decision
C busway itself	Every tap-off feeds the fault in reverse, within a few µs	Only the fault manager can arbitrate — a local trip drops the pod

Trip and Re-energize

Interrupting takes 40 µs.



The fast half is the breaker. Everything to the right of it is the fault manager .

A proposed minimum SSCB ↔ DC Fault Manager interface

Signal	Direction	Budget	Why it has to exist
Trip event + µs timestamp	SSCB → FM	< 10 µs	locate the faulted zone before anyone else trips
Block / permissive	FM → SSCB	< 5 µs	selectivity, now that time grading is gone
di/dt and I_peak record	SSCB → FM	post-fault	classify the fault and back out the real L_loop
Open / close command	FM → SSCB	ms	galvanic isolation and staged restart
Health · thermal · clamp wear	SSCB → FM	periodic	know the breaker's margin before the fault, not after
Ready-to-energize handshake	FM ↔ rectifier	ms	precharge and inrush control on re-energization

The latency budgets are a proposal, not a measurement. Converging on them is the ask on the next slide.

Call to action

Three things the community can do that no single company can do alone.

1 Move to model-based design

WHERE WE ARE

An SSCB is specified today by rated current and breaking capacity. Whether it actually works is set by the loop it sits in — L_loop, di/dt, detection budget, clamp energy. None of that is on a datasheet.

THE ASK

Publish the model, not just the number: an open reference model with its parameters and an energy-balance self-check, so anyone can re-run it for their own layout.

2 Define a notional DC data centre

WHERE WE ARE

Every protection study uses its own topology and its own parasitics, so no two results can be compared. Power systems solved this decades ago with the IEEE 9-, 14- and 39-bus test systems.

THE ASK

Agree one notional 800 VDC pod: source impedance, busway L and R per metre, tap-off count and rating, load and link capacitance, storage contribution, and named fault locations.

3 Design the breaker and the system together

WHERE WE ARE

The breaker's design window is set by the system — bus voltage, withstand ceiling, L_loop. The system's ride-through is set by the breaker — clearing time, clamp energy, re-energize sequence. Neither side can specify alone.

THE ASK

SSCB suppliers and LVDC system designers working jointly inside OCP DC PD, on the SSCB ↔ DC Fault Manager interface and the fault-current envelope it has to serve.

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Thank You!

