IT Equipment Workstreams Update





By Austin Hipes (UNICOM Engineering)

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Immersion-ITE Technical Committee Chair

Workstreams at a Glance

The ITE Committee concentrates on the specific needs and challenges associated with integrating IT equipment with immersion cooling technologies. This includes designing IT hardware that is optimized for advanced cooling methods, assessing the impact of cooling technologies on IT equipment performance, and developing guidelines for IT equipment installation, configuration, and maintenance in environments using immersion cooling solutions.

ITE Design Guidelines

Workstream leads: Austin Hipes (UNICOM Engineering) and **Peter Liu** (ASMC)

2nd Monday 8:00-9:00am PT / 17:00-18:00 CET / 23:00-24:00 CST

Zoom link





ITE Advanced Cooling Techniques

Workstream leads: Andy Richenderfer (Lubrizol), **Florian Hudelmaier** (Wieland)

1st Wednesday 8:00-9:00am PT / 17:00-18:00 CET / 23:00-24:00 CST

Zoom link





Signal Integrity

Workstream leads: Kai Wang (Intel) and **Tina Bao** (TE)

Each 1st Monday 8:00-9:00am PT / 10:00-11:00am CT / 17.00-18.00 CET

Zoom link

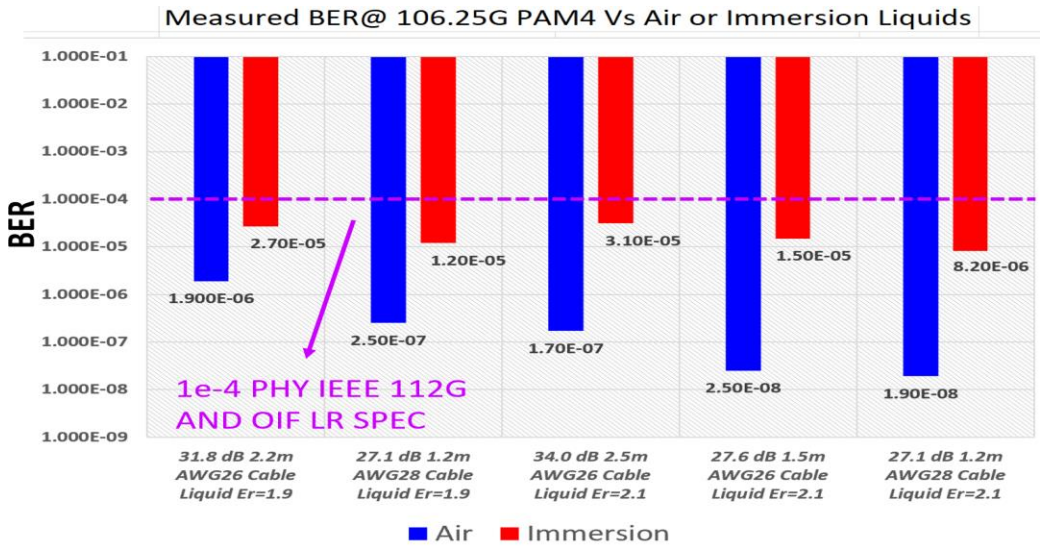


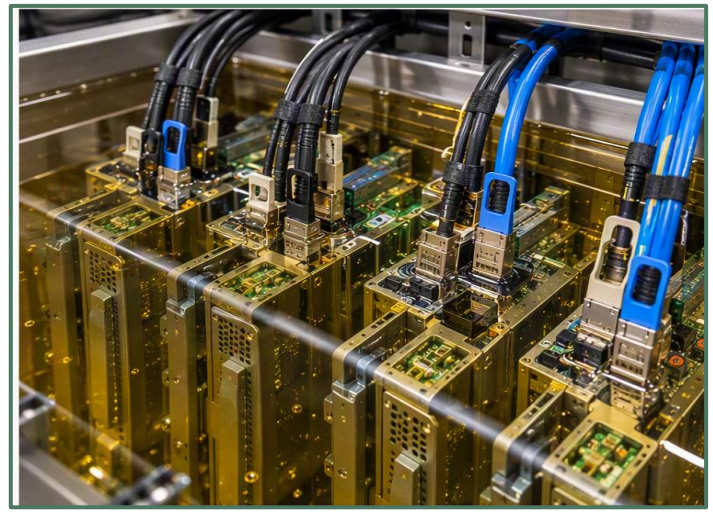


New Project: Immersion Cable & Component Validation

Immersion cable specification work is underway

- **Component validation project for immersion ITE**
- Peter Liu has offered to lead the project under ITE Design Guidelines
- Additional component classifications can follow





Data cables and connectors operating below the dielectric-fluid surface

Why the ITE Guidelines Needs a Major Refresh

- Revision 2.0x refresh is underway
  - Last update was made in December 2020
  - Numerous industry changes
  - Larger community
  - Wider adoption of immersion cooling
  - Higher power silicon available today
  - Customers are looking for a degree of standardization and interoperability
- Major refresh underway
- Participation needed across the industry
  - Server OEMs & Integrators
  - ITE Customers
  - Silicon manufacturers
  - Immersion Solutions Providers
  - Regulatory organizations
  - Fluid providers
  - Etc.



OPEN
Compute Project

Design Guidelines for Immersion-Cooled IT Equipment

Revision 1.0

Authors:

Lesya Dymyd, Leonard Ciubotaru, Michael Helezen (2CRSI), Jimil M. Shah (3M), Lentis Pai (Wiwynn), Rolf Brink (Asperitas), Rick Payne (Flex), Jessica Gullbrand (Intel), Nigel Gore (Vertiv)

Reviewers:

Rob Curtis (Dell), Alex McManis, Larry Kosch (GRC), Herb Zien (LiquidCool Solutions), John Bean

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ITE Design Guidelines: Revision 2.0x Progress

- Last update was made in December 2020
  - Numerous industry changes
  - Larger community
  - Wider adoption of immersion cooling
  - Higher power silicon available today
  - Customers are looking for a degree of standardization and interoperability

- Refresh underway
  - Sections 1, 2, 3 & 4 wrapping up (under review)
  - Section 5 under development (Best Practices & Principals)
  - Working document:

- Participation needed across the industry
  - Server OEMs & Integrators
  - ITE Customers
  - Silicon manufacturers
  - Immersion Solutions Providers
  - Regulatory organizations
  - Fluid providers
  - Etc.

Guidelines 2.0x

Open Compute Project Design Guidelines for Immersion-Cooled IT Equipment

Test ID	Cooling mode	Fluid and ITE configuration	Thermal boundary conditions	Power and workload	Required evidence
TC-01 Baseline	Intended natural, direct, targeted, forced, mixed, two-phase, or hybrid mode	Named fluid and lot or approved property range; production-representative BOM, firmware, orientation, power, cable, and fluid interfaces	Nominal fluid inlet or bath temperature; nominal secondary-loop condition; nominal flow or circulation	Defined baseline performance configuration and representative sustained workload	Component temperatures and margins; inlet/outlet or bath temperatures; flow; pressure drop if applicable; system/component power; performance; alarms or throttling
TC-02 Maximum performance	Same mode as baseline unless modes are compared	Same fluid and comparable production-intent configuration; maximum supported performance settings	Nominal boundary conditions maintained within reported tolerances	Maximum supported sustained performance using subsystem and system workloads appropriate to the platform	Sustained performance; maximum component temperatures; thermal margin; total power; throttling; errors; link state; protective actions
TC-03 High inlet temperature	Intended cooling mode	Same fluid and ITE configuration as baseline	Maximum specified normal inlet or bath temperature; secondary-loop inlet and heat-exchanger approach reported	Representative sustained workload at defined baseline or maximum performance	Thermal margin; power; performance; flow; pressure drop; alarms; throttling; pass/fail against product limits
TC-04 Minimum circulation	Applicable active or directed-flow mode	Same fluid and ITE configuration as baseline	Minimum specified normal flow or circulation; inlet temperature held at a defined value	Representative sustained high-power workload	Component response; distribution indicators; pressure drop; thermal margin; performance; flow or pump status
TC-05 Maximum design power	Intended cooling mode	Highest supported CPU, GPU, accelerator, memory, storage, network, and power-conversion configuration	Nominal and high-inlet conditions as applicable	Workload combination producing maximum sustained system heat load or defined design power	Total and subsystem power; critical temperatures and margins; performance state; throttling; stability; cooling-capacity margin
TC-06 Transient condition	Intended cooling mode	Same configuration as maximum-power test	Defined steady boundary conditions before and during transition	Transition from idle or low load to high power and return to lower load	Temperature and power response; overshoot; time to steady state; controls; pump/flow response; throttling; alarms

Evidence checklist

The following evidence package should accompany the completed matrix so results can support design qualification, customer deployment decisions, regulatory review, and warranty-envelope definition.

☐ Test plan with objectives, scope, applicable requirements, acceptance criteria, deviations, and responsible laboratory or organization.

☐ Test-article identification with manufacturer, model, serial or asset identifier, hardware revision, prototype or production status, and tested configuration.

☐ Controlled BOM identifying immersion-critical components, materials, cables, connectors, labels, adhesives, heat sinks, TIMs, seals, coatings, and approved alternates.

☐ Firmware and software record including BIOS/BMC, accelerator and device firmware, operating system, drivers, management tools, workload versions, and settings.

☐ Cooling-system description identifying tank or enclosed chassis, cooling mode, pumping or circulation method, heat exchanger, secondary loop, manifolds, filters, hoses, and connection layout.

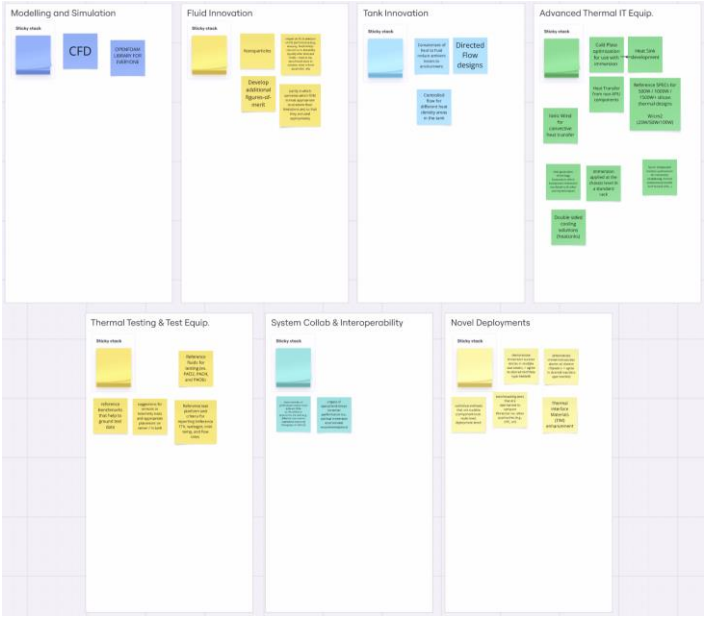
☐ Fluid record identifying manufacturer, product, batch or lot when available, condition, sampling date, exposure history, and physical, thermal, and dielectric properties used for interpretation.

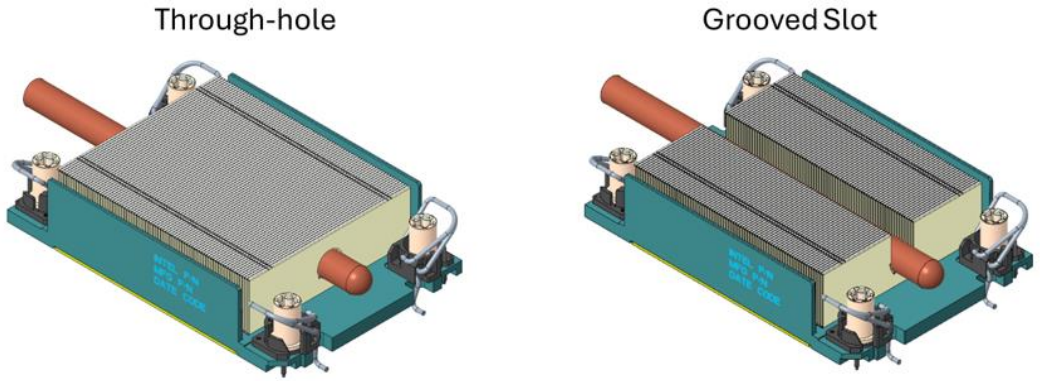
Advanced Cooling Techniques: Current Focus

Focused on thermal optimization techniques and design optimizations for high TDP silicon (>500W). For fluid, thermal solution, and ITE designers.

First Reference Design for Targeted Flow Heatsink published

https://www.opencompute.org/documents/ocp-spec-targeted-flow-efficiency-heat-sink-v1-0-pdf





ACT Miroboard

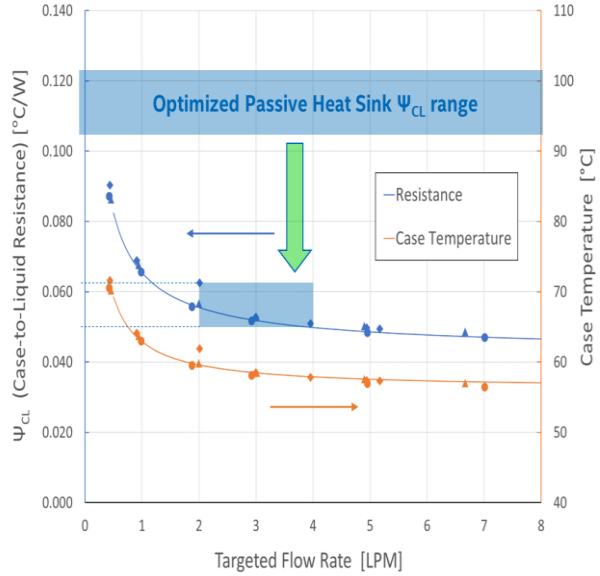
ACT Project: Thermal Performance Test Specification

First project under development

Thermal Performance Test Specification

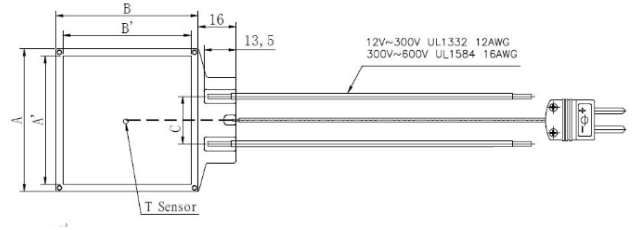
Developing reference test platform and methods for fluids, heatsinks, and TIMs for industry use and comparison

Thermal Performance Test Specification Outline.docx



Specification authoring has begun (sections covered)

- Hardware
- Instrumentation
- Componentry
- Controls, Protocols, and Test Matrix
- Benchmarking



- Opportunities for OCP members to submit SPECs for thermal solutions for publication
  - Eg. Targeted Flow Heatsinks, hybrid immersion cold-plates, etc

Signal Integrity Update

Continued testing of SI Margin Testing of DDR / PCIe / Ethernet / Optical

- Good results overall, but margins are shrinking in same cases
- Crosstalk can be reduced in other cases, such as DDR5
- Focus beginning on frequencies >32GHz (e.g. 224G PAM4 @ 56 GHz)
- Focus on higher frequency test results for next whitepaper revision

Research Into Acceptable Test Methods

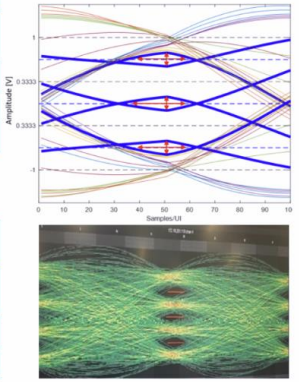
- Frequences Required
- Test Methodologies and Equipment
  - Resonator Cavitary Types
  - Temperatures
  - Frequency Test Points

High Speed IO	Immersion Eye compared to Air	Eye Immersion Aging
DDR 5600,6400MT/s, 8800MT/s	➢ 95 % Small data samples	After 24 months; no change
PCIe 5.0 / 4.0	Similar Eyes	After 24 months and 4 month
Ethernet 56G PAM4 per Lane	Pass	After 24 months; no change
Sealed Optical Ethernet	Pass	WIP

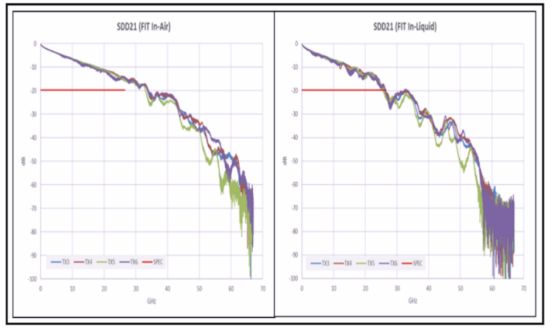
Test focus

High Speed IO	Compared Air BER with Immersion Eye BER	Worse BER impact to work lord Performance
AI/Ethernet 112 Gbps PAM4	* 1e-8 → 1e-6 to 1e-5	* Need Study BER drop impact to AI workload
AI/Ethernet 224 Gbps PAM4		
PCIe 6.0 64 Gbps PAM4	WIP	

PAM4 and BER

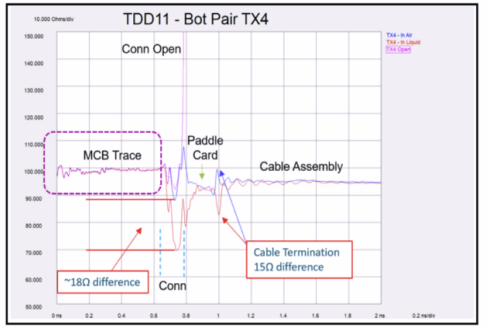


OSFP 800 Connector and Cable Insertion Loss



Insertion Loss is higher when submersed in fluid. Marginal for 112G.

OSFP 800 Connector and Cable Impedance



"Isolation" Fixtures allow us to pin-point specific areas affected by the fluid. Note the MCB Traces are smooth as they are not submersed in fluid.

Signal Integrity Whitepaper: New EMI Evidence

New System Emissions (EMI) comparisons, measured in air and immersion environments contributed.

https://drive.google.com/file/d/1gihfAcUGMkmk9S_QJm75hCDz_VDQ0jhM/view?usp=sharing



Get Involved: Join the ITE Workstreams

Advanced Cooling Techniques

Volunteers needed with experience and interest in the design, testing, and validation of thermal solutions and techniques fo n cooling of silicon >500W.

Design Guidelines for ITE

Volunteers needed with experience in immersion ITE design, testing, and validation. Help establish industry guidelines and standards for the development, integration, deployment, and servicing of immersion ITE.

Signal Integrity

Volunteers needed with experience and interest in SI testing, SI simulation, PCB/cable/connector design in immersion environments. Explore and understand how immersion affects SI and how to mitigate possible negative impacts.