NETWORKING

224G AECs for AI Data Centers

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OCP PLATINUM Member

Copper Solutions at 224G per lane

112G AECs → 224G per lane

1–7 m

Common deployment range

How do we keep copper-based solutions moving forward?

Higher data rates and compute needs bring recurring challenges



Heat | Operational cost | Reliability | Network margin

Solving the problem of power

72 ports per rack

4 GPU trays

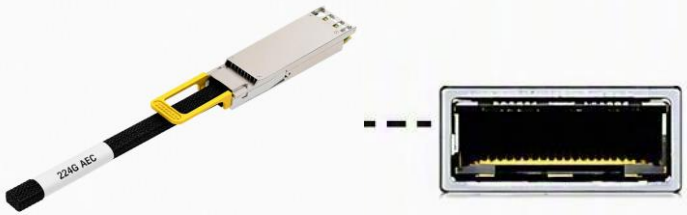
18 ports per tray

$4 \times 18 = 72$ ports

Port mix at 224G

18 passive ports 25%

54 active ports 75%



1 module per active port

5,000 racks

270,000 active modules

AOC 25 W/module	6.75 MW
AEC 18 W/module	4.86 MW

28% lower power

1.89 MW saved with AEC

Assumptions: 4 trays/rack, 18 ports/tray, 25% passive connections. Module power only; excludes other IT and cooling loads.

Optimizing the solution

Optimize

PCB, Twinax, SI at the PCBA

Known Good Die

vs Packaged Design



Copper connectivity options at 224G per lane



AEC maintains an Excellent BER across the known use cases of 1–6 m.

1.6T AEC growth outlook

Global annual units (millions)

2026–2031 forecast



1.74M

800G AEC units in 2025

6.5×

1.6T growth, 2027–2030
1.37M to 8.85M units

2030

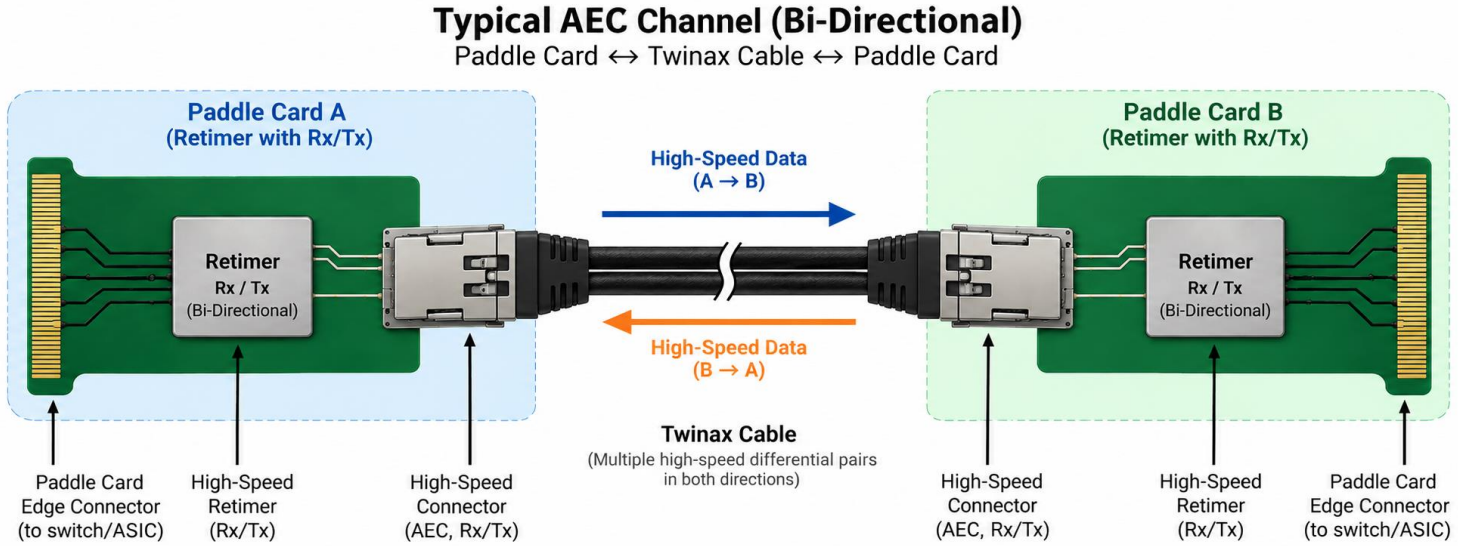
First forecast year with
1.6T ahead of 800G

Source: LightCounting Cloud Data Center Optics Database, July 30, 2026

6m+ at 224G Is Nuanced

Every segment of the channel has to be optimized together

Insertion Loss	Crosstalk	Intra-Pair Skew	Reflections	Power Supply Noise



Optimize every segment: Retimer ↔ Package ↔ Paddle Card ↔ TwinAx

Where it starts: AEC Retimer Silicon-level specs and simulation for <u>every</u> segment

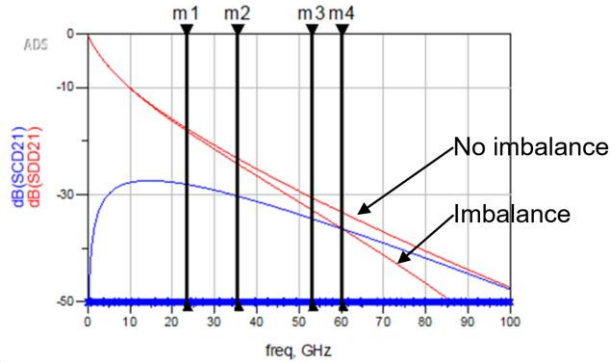
Skew: Legacy Metrics Fail at 200G+

Intra-pair skew

- Degrades signal quality
- Raises insertion loss, crosstalk and EMI

Legacy metrics break down at 200G+

- Time-domain (TDR/TDT): poor correlation to system performance
- Raw frequency-domain (VNA): skew varies widely across frequency bands

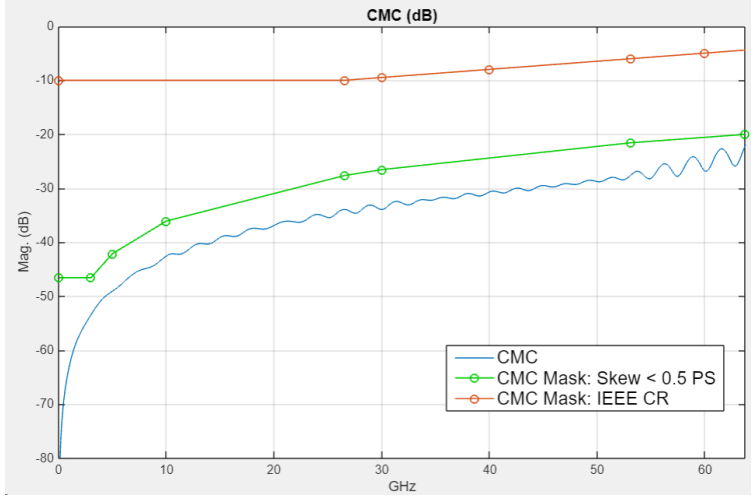


IL roll-off caused by P/N imbalance

EIPS – weighted integration, time- + frequency-domain

$$\mathrm{EIPS} = \int_{f_{min}}^{f_{max}} W(f) \cdot |\,\mathrm{skew}(f)\,|\, df$$

Absolute frequency-domain skew integrated against a normalized weighting function W(f)[1]



IEEE CR mask
Long, tightly coupled pairs like 3m+ twinax cables

Skew < 0.5 ps mask
Short, loosely coupled lines: packages, paddle cards, DVT and OSFP boards

[1] S.-J. Moon et al., "Intra-Pair Skew Metric, EIPS (Effective Intra-Pair Skew)," IEEE 25th SPI Workshop, Siegen, Germany, 2021

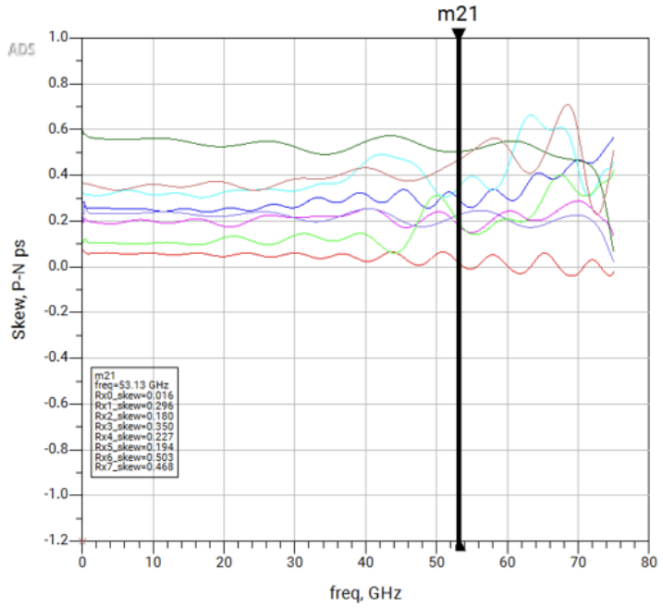
Retimer Silicon & Package Optimization

Same SerDes as used in
Broadcom Tomahawk switches

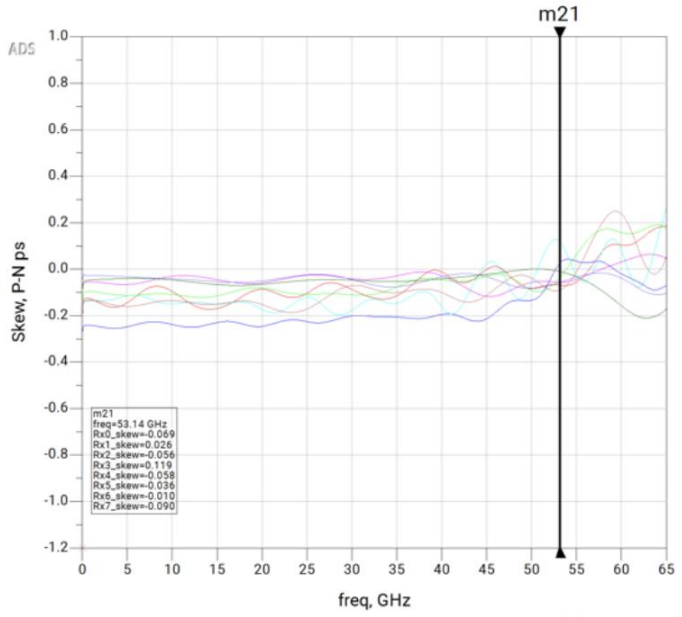
Signal integrity leadership (Superior DSP Equalization Architecture)
>45 dB Insertion Loss Profile

Industry's broadest DSP / retimer portfolio
25+ years of customer collaboration

Non-Optimized



Optimized

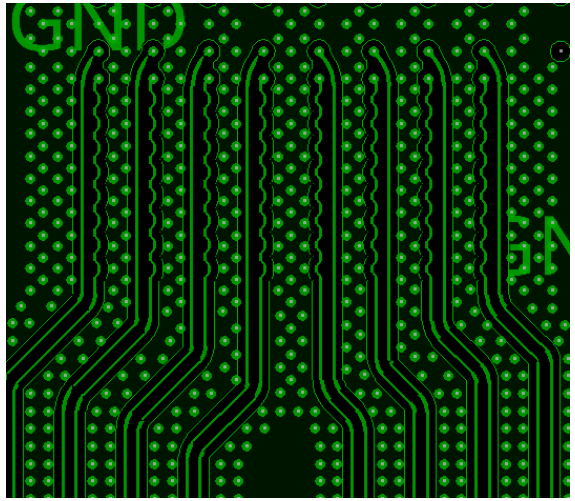


Optimize Package For

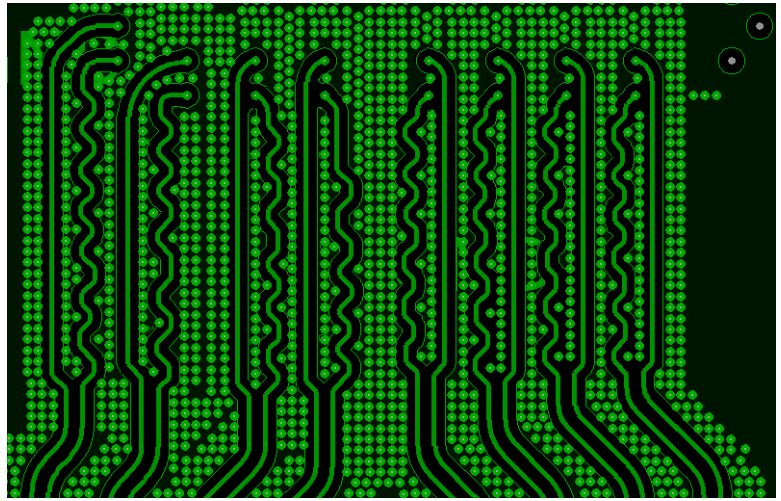
P/N Skew	Lower, tighter P–N skew across all lanes
Reflections	Improved impedance profile
Crosstalk	Special GND shielding techniques

Paddle Card Optimization & Co-Simulation

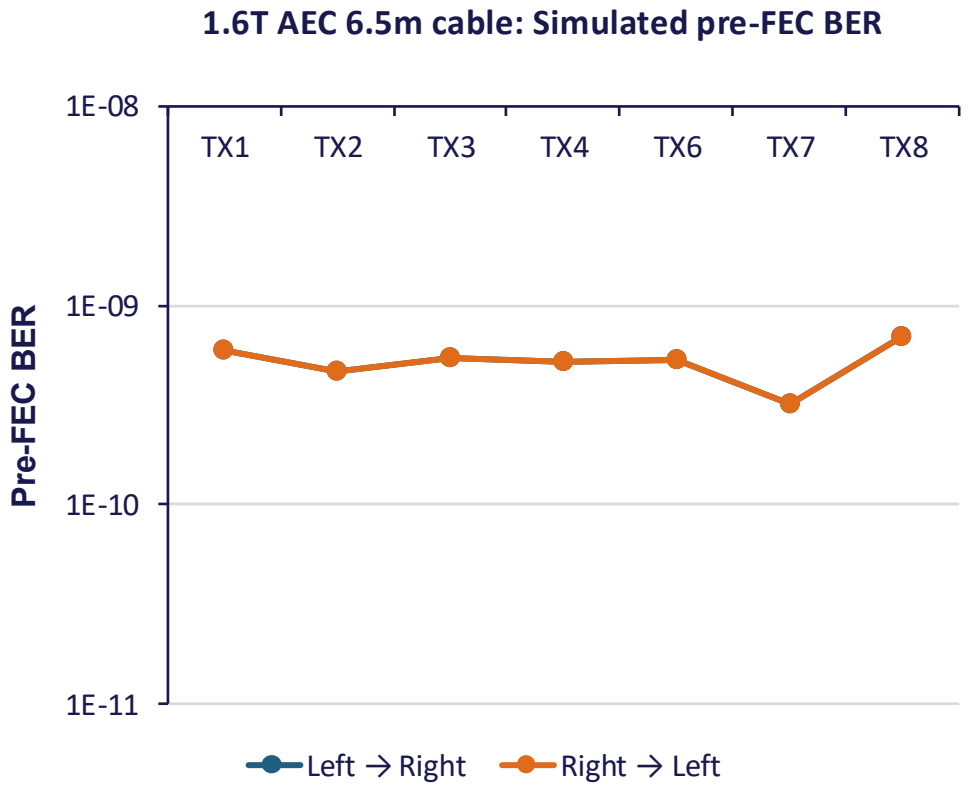
Non-Optimized



Optimized (For EIPS/CMC spec)



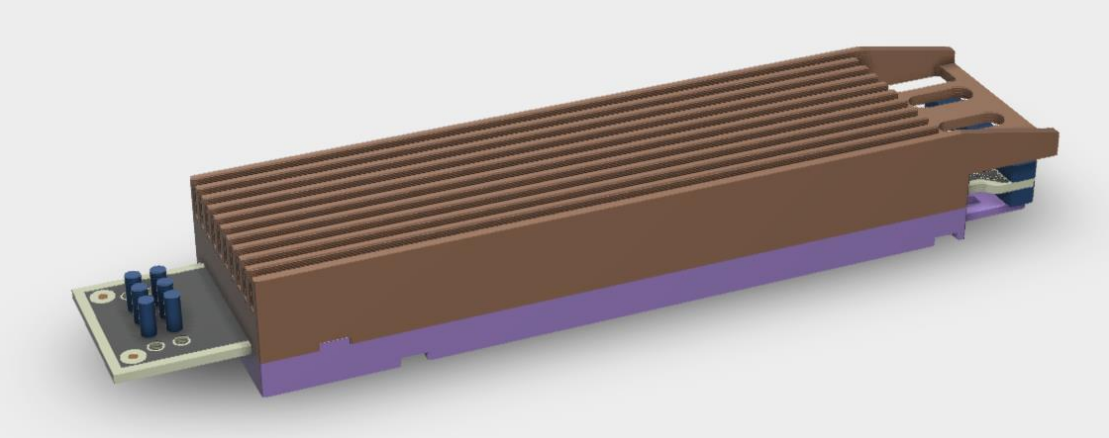
P/N Skew



Co-simulate the full channel: retimer + package + paddle card + twinax → every lane lands in a tight BER band at 6.5m

Consistent 6m+ Performance, Faster TTM

A shared paddle card baseline helps cable partners and hyperscalers



What each side gets

- **Cable partners:** A proven baseline for faster TTM, with room to differentiate (TwinAx, connectors etc)
- **Hyperscalers:** Consistent performance
- **Behind it:** Silicon-level insight, optimized end to end

How we get to 6m+

Drive specs	Retimer & Package	Paddle card & TwinAx	Co-simulate	Shared baseline	Cable partners & hyperscalers
EIPS & CMC masks per segment	DSP architecture, SI expertise	Skew-matched	Full channel, 6.5 m	Paddle card design	Build, qualify, deploy

Real-Time Diagnostics

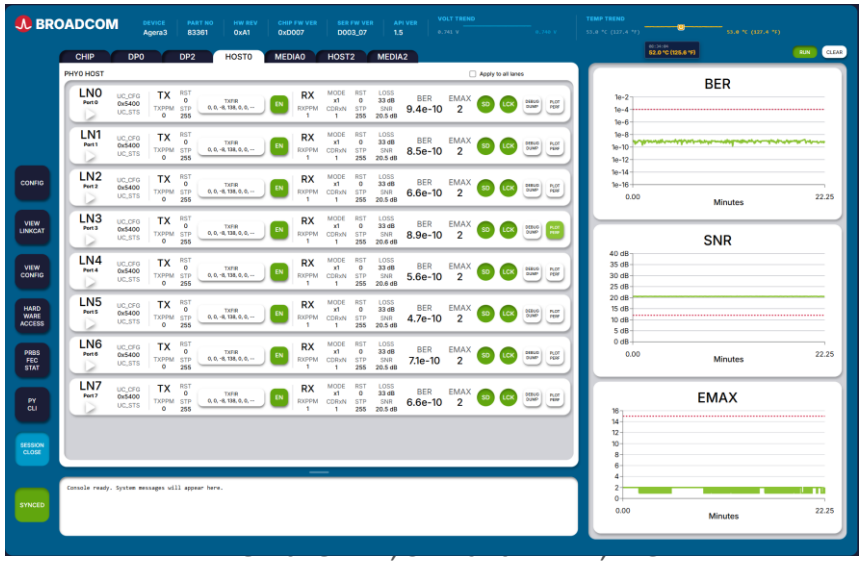
Find cable issues fast – for cable partners and hyperscalers

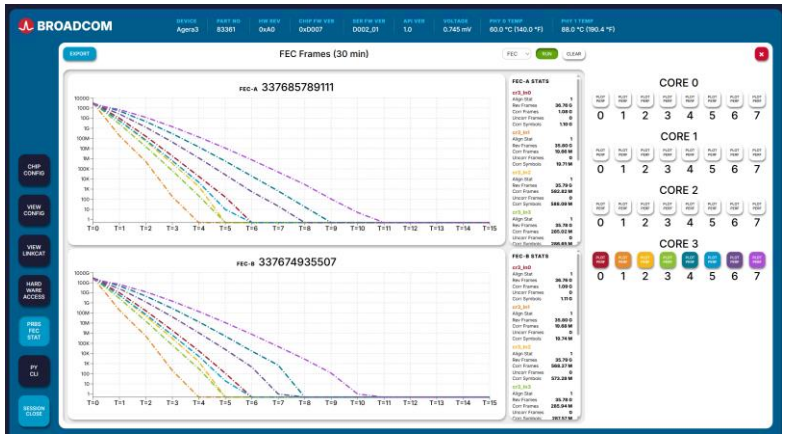
Cable partners

Faster bring-up, production test and failure debug

Hyperscalers

Operational efficiency: find a bad cable before it hurts the fabric





FEC tail: frame-error statistics

Pre-FEC BER | SNR | FEC tail monitoring | Power & temperature | Near-end + far-end

Robust, real-time telemetry measured on the retimer itself – at both ends of the cable

Real-Time Channel Modeling– At Hyperscalers

Characterize the entire AEC channel – and manage it from one common interface



Entire channel, in real time

- Frequency response (raw and smoothed)
- Step and pulse response
- Per lane, host and media side
- Whole channel, not just one segment

One common interface

The GUI integrates into CMIS software – one interface for diagnostics and channel modeling

Diagnose the cable (real-time), model the channel, all through CMIS

AGERA Ethernet AEC Family

400G



- **Same SerDes as Tomahawk5**
- **>45dB Reach,** 8m+
- In production

800G



- **Same SerDes as Tomahawk5**
- **>45dB Reach,** 8m+
- In production

1.6T



- **Same SerDes as Tomahawk6**
- **>45dB Reach,** 6m+
- In production

3.2T



- **400G SerDes**
- **>40dB Reach**
- Coming soon!

Industry's 1st AEC Retimer supporting lowest pJ/b, while extending 1.6T cable reach to 6m+

Key Takeaways

What it takes to deliver 6m+ at 224G

1 6m+ is nuanced

- Optimize: Insertion Loss, crosstalk, skew, reflections and supply noise across the channel
- Every segment matters: retimer, package, paddle card and twinax

2 Cable + Silicon-led, ecosystem-wide

- Specs and co-simulation across every segment
- A shared paddle card baseline: faster TTM for cable partners, consistent performance for hyperscalers

3 Reduce Hyperscalers TTM & Opex Cost

- Real-time diagnostics through CMIS
- Real-time channel modeling through CMIS

AEC eco-system for longer reach is ready for 224G, next-phase is to help the industry deploy & ramp 224G AEC’s

Thank You!

