Cooling Environments





Immersion Project

Rack Scale Reliability Demonstration Testing of an Intel Datacenter Certified Immersion Solution

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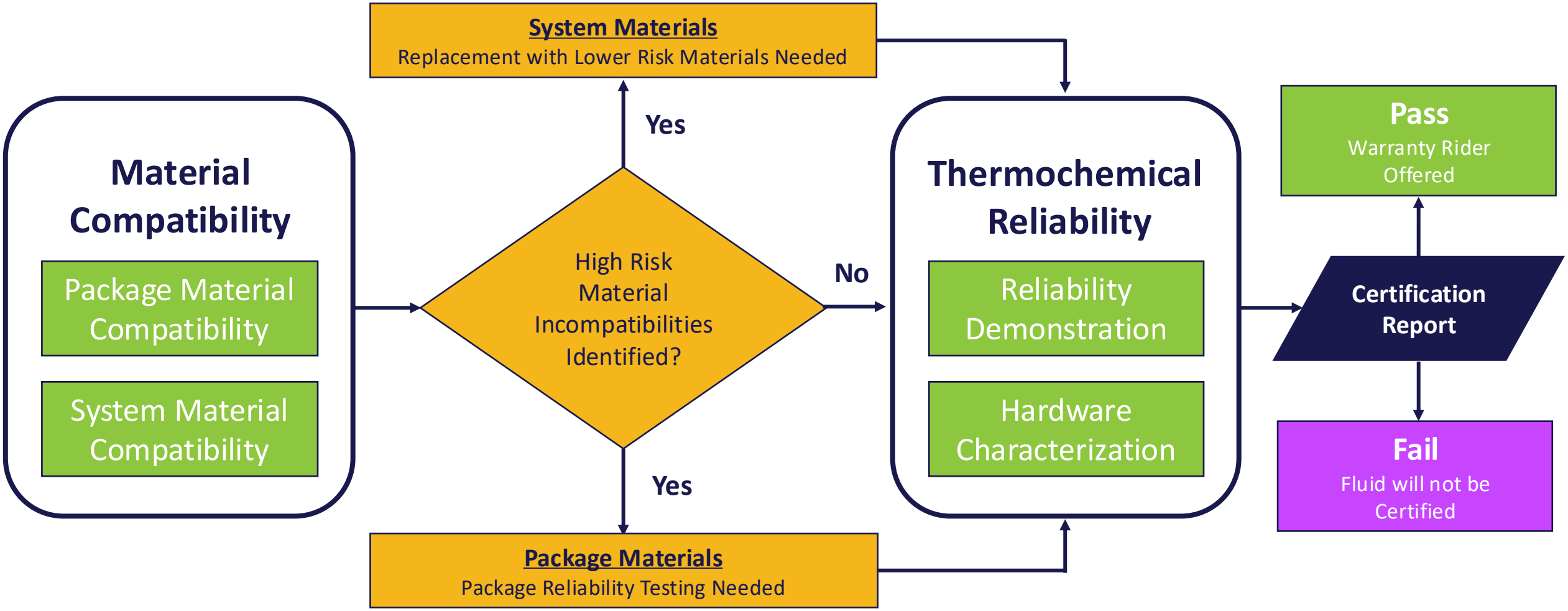
Betsy Cossette *Immersion Cooling Market Development Manager - ExxonMobil*

OCP PLATINUM Member

Intel Datacenter Certified Immersion Solution

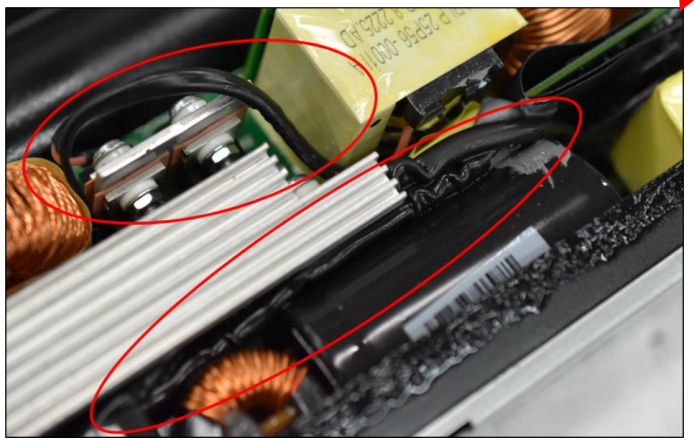
	Tested	Enveloped
Intel	5th Gen Intel® Xeon® Platinum 8592+ Processor	5th Gen Intel® Xeon®
BAC	DUG Cool 26RU – 30kW: 2 CDU Configuration	Rev 1.5: 16RU, 32RU, 48RU
Hypertec	Ciara Trident IC610DR-G6	—
Micron	64GB DDR5 4800MT/s RDIMM x 16	16GB, 32GB
ExxonMobil	EM DC 3235 Super	EM DC 3220, EM DC 3250

Intel Datacenter Immersion Certification



Material Compatibility Results

Package Reliability	Result
Assembly Test Vehicle	PASS
Substrate High Speed IO	PASS



Component	Result	Resolution
Intel® XEON®	HIGH RISK	PASSED: Package Reliability Testing
Motherboard	PASS	
Power Supply	FAIL	REPLACED: Wire Insulation Material
CPU1 Heatsink	PASS	
CPU2 Heatsink	PASS	
Power Cable v1	PASS	
Power Cable v2	PASS	
Coin Cell	PASS	
Chassis Screws	PASS	
PCIe + Riser	PASS	
Power Delivery Board	PASS	
Chassis Mylar	PASS	
PCH Heatsink	PASS	
Network Heatsink	PASS	
SSD	PASS	
NIC Card	PASS	
Micron RDIMM	PASS	

IRDT: Thermochemical FMEA

Thermochemical Reliability

Fluid + Materials
=
Contamination

↓

Potential Thermochemical Reactions

↓

Potential Performance
and
Reliability Degradation

Rack-Scale Thermochemical FMEA

- Component performance degradation due to secondary reactions with contamination
- Film, deposit, or particle formation that results in hardware performance degradation
- Fluid property changes that impact hardware performance

Risk-Based Certification Plan

- Thermal Performance Degradation Assessment
- Signal Integrity Degradation Assessment
- Memory Degradation
- Performance Benchmark Degradation Assessment
- Fluid Analysis
- Contamination Baseline

Data-Driven Certification

- Demonstrated Reliability
- Statistical Analysis of Performance Degradation
- Fluid Stability
- Contamination Quantification

Fluid Service Use Case: Ideal Batch Reactor Model

Ideal Batch Reactor Assumptions:

- System is closed so mass/volume is conserved and constant
- System is well mixed and homogeneous

1st order reaction for a batch reactor:

$$[P] = [R]\, e^{-kt}$$

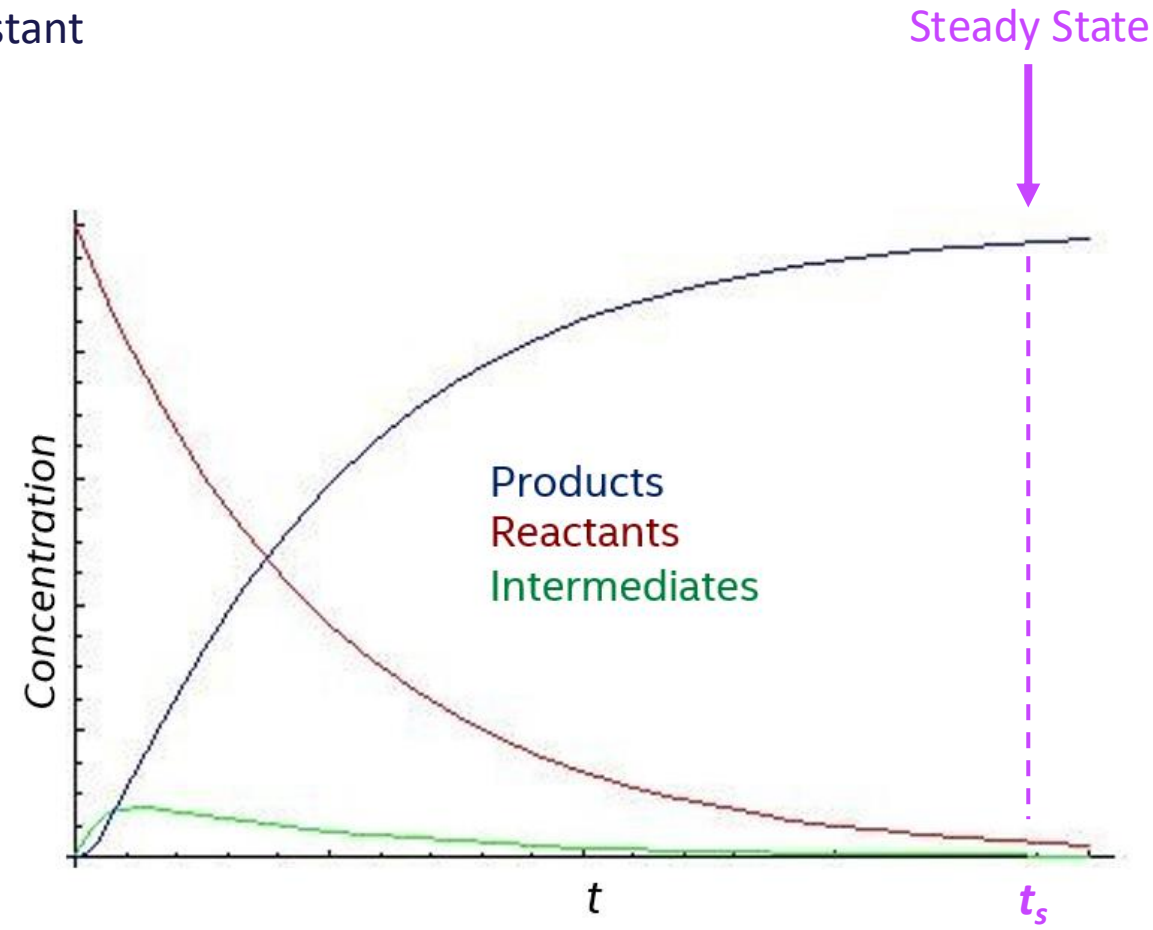
where *k* is the reaction rate and *t* is time.

Intermediate Reactions:

$$[R] \xrightarrow{k_c} [I] \xrightarrow{k_i} [P]$$

Steady state approximation for intermediate reactions:

$$[P] = \left(1 - e^{-k_c t}\right)[S]$$



IRDT: Accelerating to Steady State

Most reactions can be described with the Arrhenius relationship:

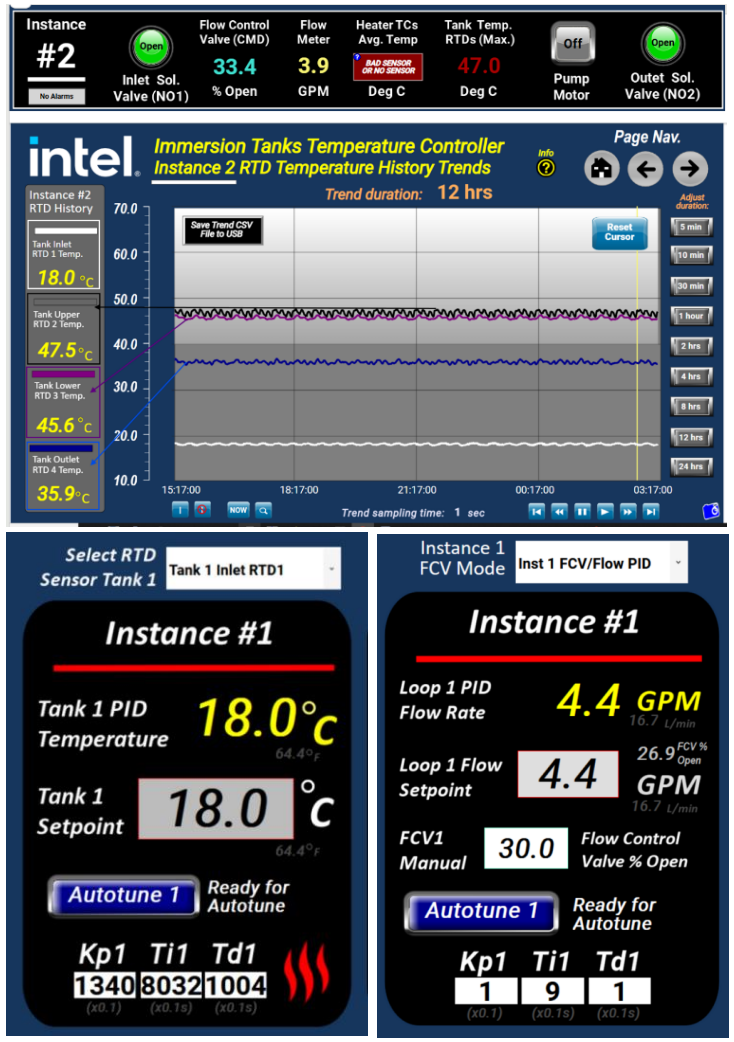
$$\ln k = \ln A - \frac{E_a}{RT}$$

Process Water Temperature Control Cabinet:

- Precise control (± 1°C) of process water to ensure consistent boundary conditions at t_0 and t_s
- Preheats process water to target a higher fluid operating temperature to accelerate achieving steady state



U.S Patent No. 12,672,256

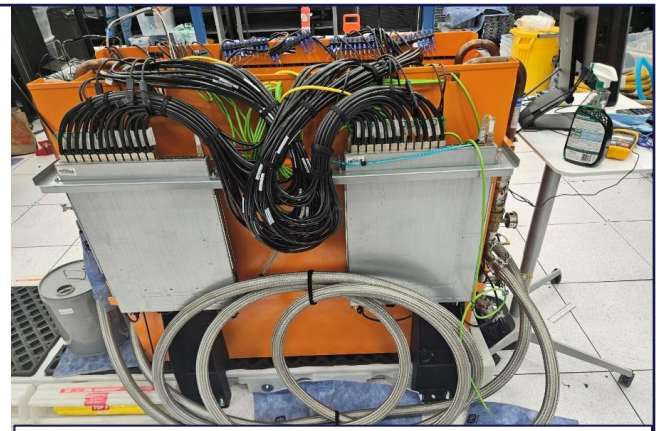


IRDT: Data Collection Infrastructure

Augmented Networking



Custom Brackets

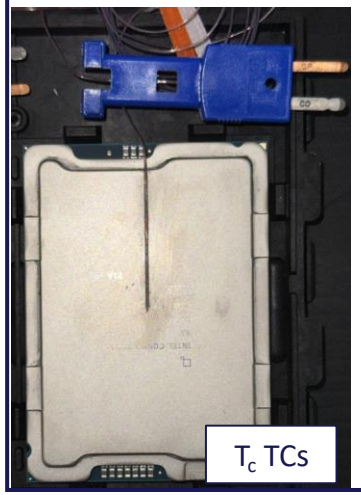


3 Switches: Network Traffic and BMC Access

Augmented Temperature Telemetry



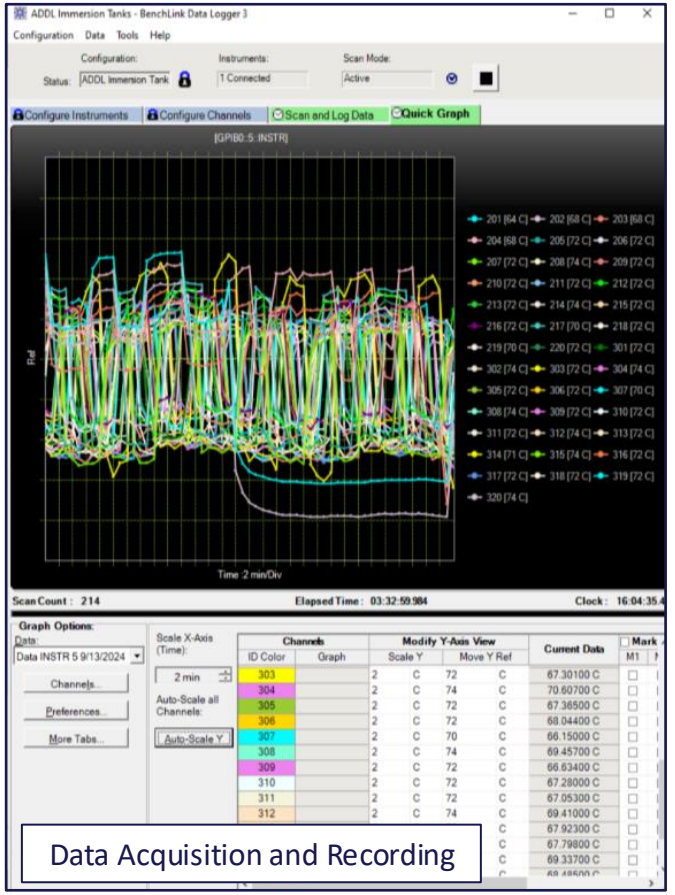
RDTs at Tank Top/Bottom



T_c TCs



RDTs on Tank In/Out



Data Acquisition and Recording

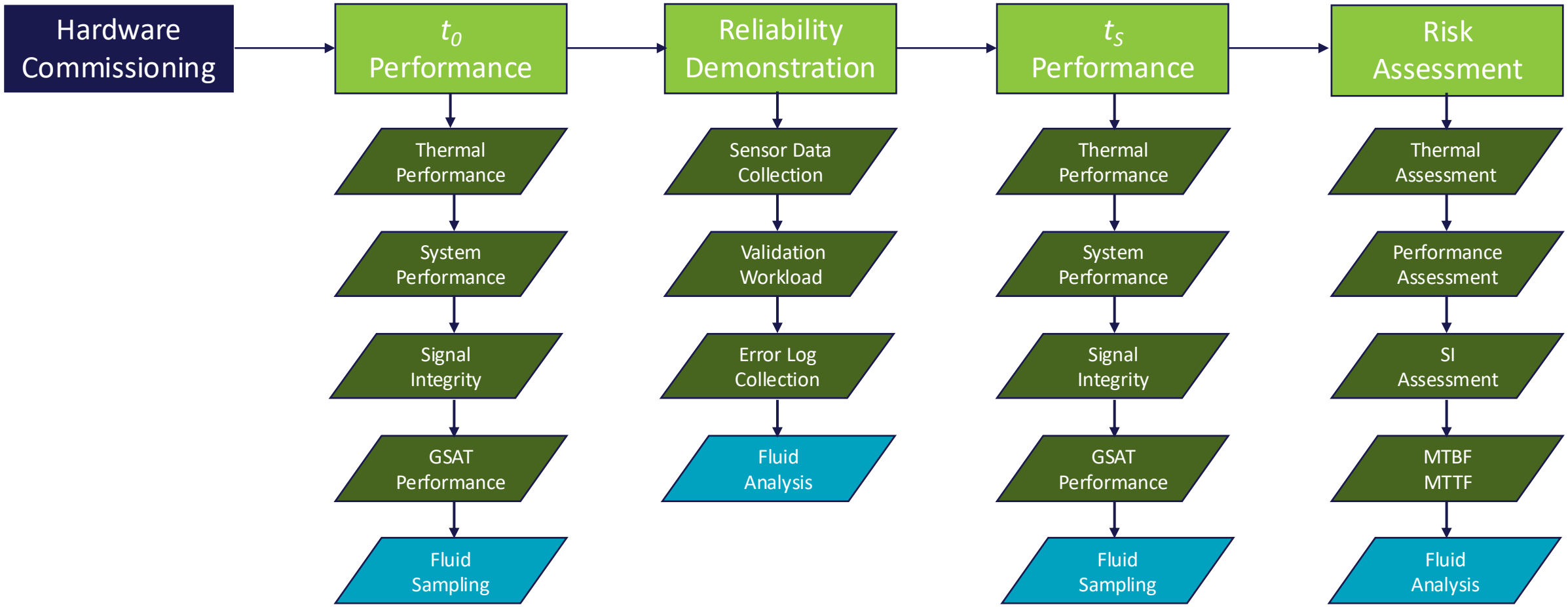
IRDT: Validation Data

Thermal Sensors	Power Sensors	Logs
CPU1_DIMMA1_Temp CPU1_DIMMB1_Temp CPU1_DIMMC1_Temp CPU1_DIMMD1_Temp CPU1_DIMME1_Temp CPU1_DIMMF1_Temp CPU1_DIMMG1_Temp CPU1_DIMMH1_Temp CPU1 Temperature CPU2_DIMMA1_Temp CPU2_DIMMB1_Temp CPU2_DIMMC1_Temp CPU2_DIMMD1_Temp CPU2_DIMME1_Temp CPU2_DIMMF1_Temp CPU2_DIMMG1_Temp CPU2_DIMMH1_Temp CPU2 Temperature PCH Temperature	+12V +3.3V +3.3VSB +5V +5VSB Power Supply 1 PSU1 Power In PSU1 Power Out +VCCD_HV1 +VCCD_HV2 +VCCFAEHV_FIVRA1 +VCCFAEHV_FIVRA2 +VCCINFAON1 +VCCINFAON2 +VCORE1 +VCORE2	Sensor_Data (CSV) iLVSS (LOG) MUERRCHK (XML)

Validation Stress	Purpose
Memory	NUMA aware memory stress test that utilizes all CPU threads at 100%.
I/O	Auto-configured Storage and Network stress test.
Server Management	BMC Sensor test and monitoring SEL and logging events.
Configuration and Event Monitoring	System configuration saved pre-test and verified post-test.
PCIe Configuration Check	PCIe device information saved for post-test evaluation.

	Log Files	Sensor Data
Log Files	8681	3041
Lines of Data	1,090,163,098	419,004,192
Unique Sensors	-	35

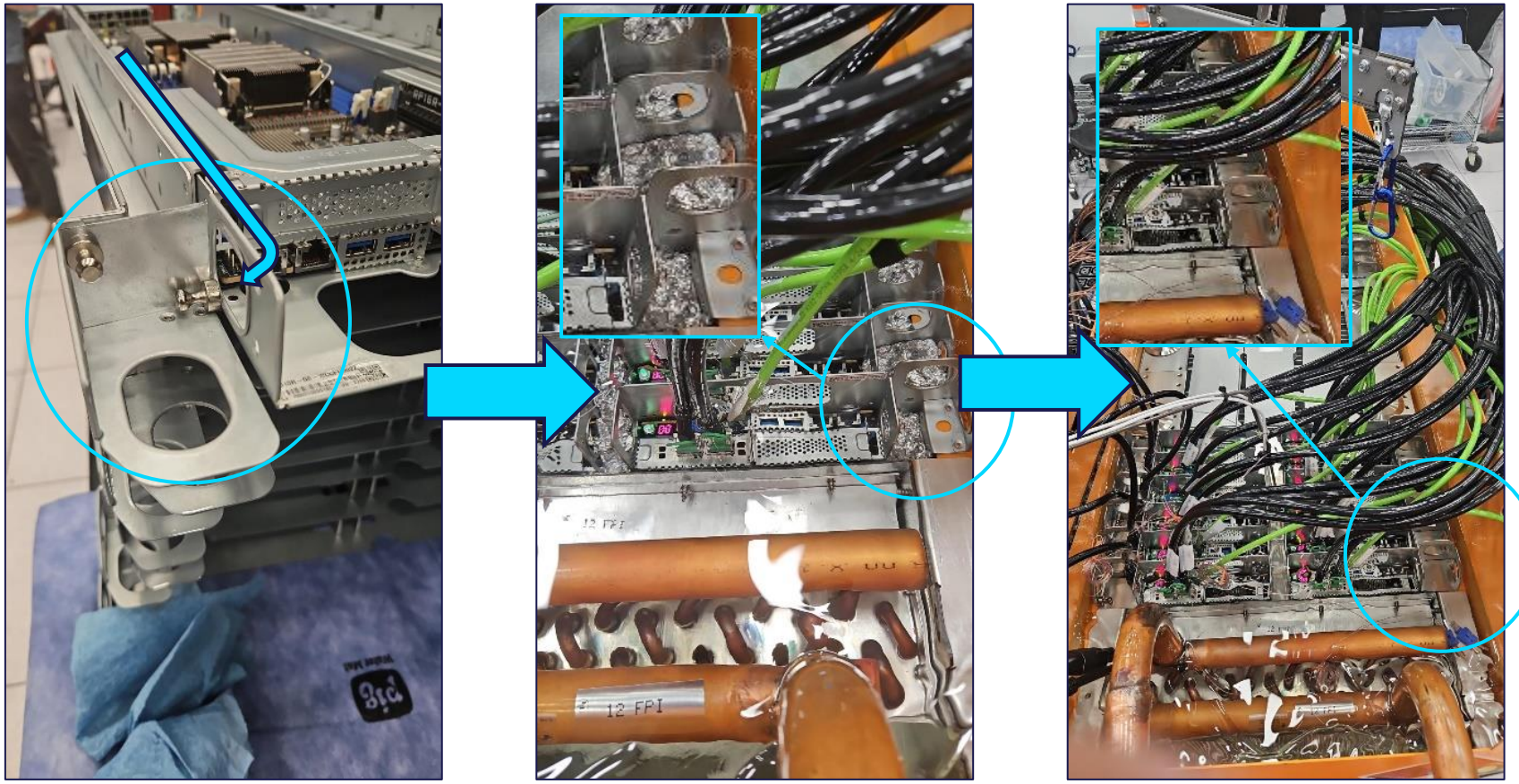
IRDT: Test Flow



IRDT: Hardware Commissioning

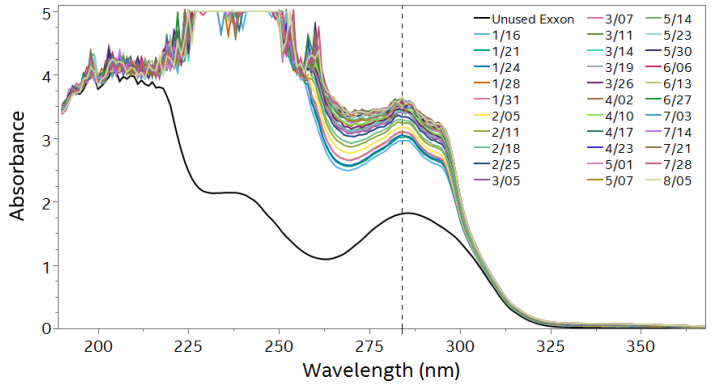
Fluid follows through the path of lease resistance. The open tank and chassis let too much fluid flow bypass the server components instead of cooling them.

- A custom chassis hanger designed for the certified configuration to prevent fluid bypass.

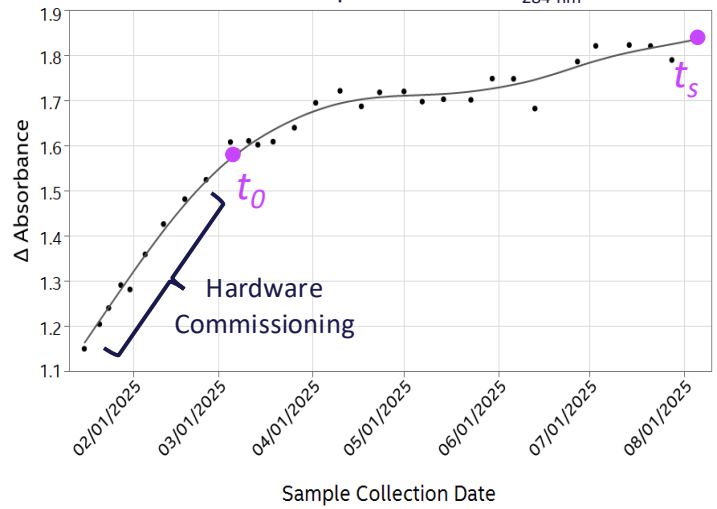


IRDT: Fluid Analysis

UV-VIS

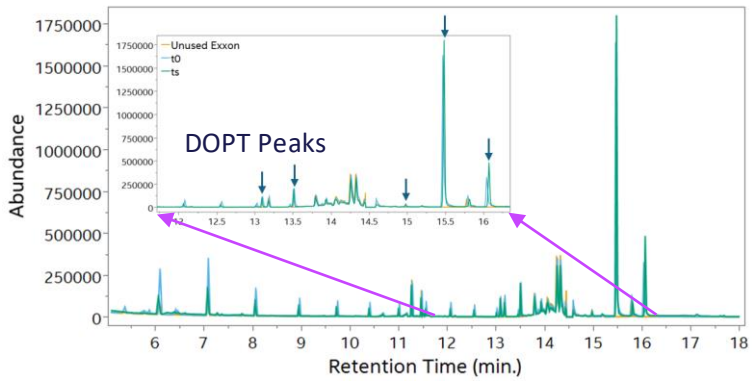


Δ Absorbance = Sample Absorbance$_{284\ nm}$ – 1.8097

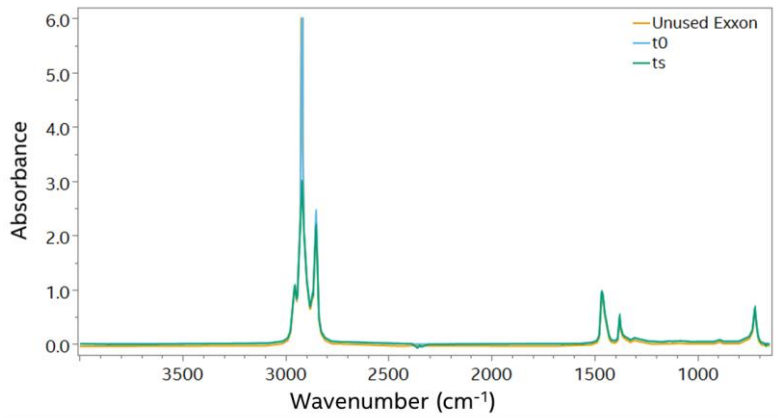


Fluid Analysis Test	t_0	t_s
GC-MS	Plasticizers	Plasticizers
ICP-MS: Bromine	11.20 ± 0.03 ppb	25.09 ± 0.12 ppb
Dielectric Constant	Er = 2.11 Loss tangent = 0.0004	Er = 2.11 Loss tangent = 0.0004
FT-IR Spectroscopy	Matched to Unused	Matched to Unused
UV-Vis Spectroscopy (Absorbance @ 284 nm)	3.394	3.654
Visual Color/Appearance	Matched to unused	Matched to unused

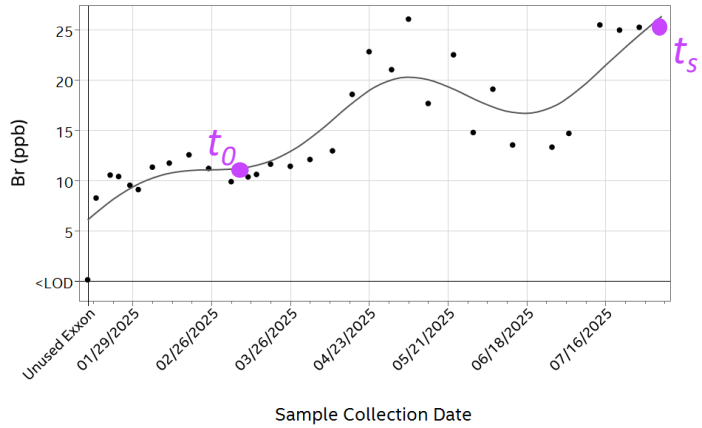
GC-MS



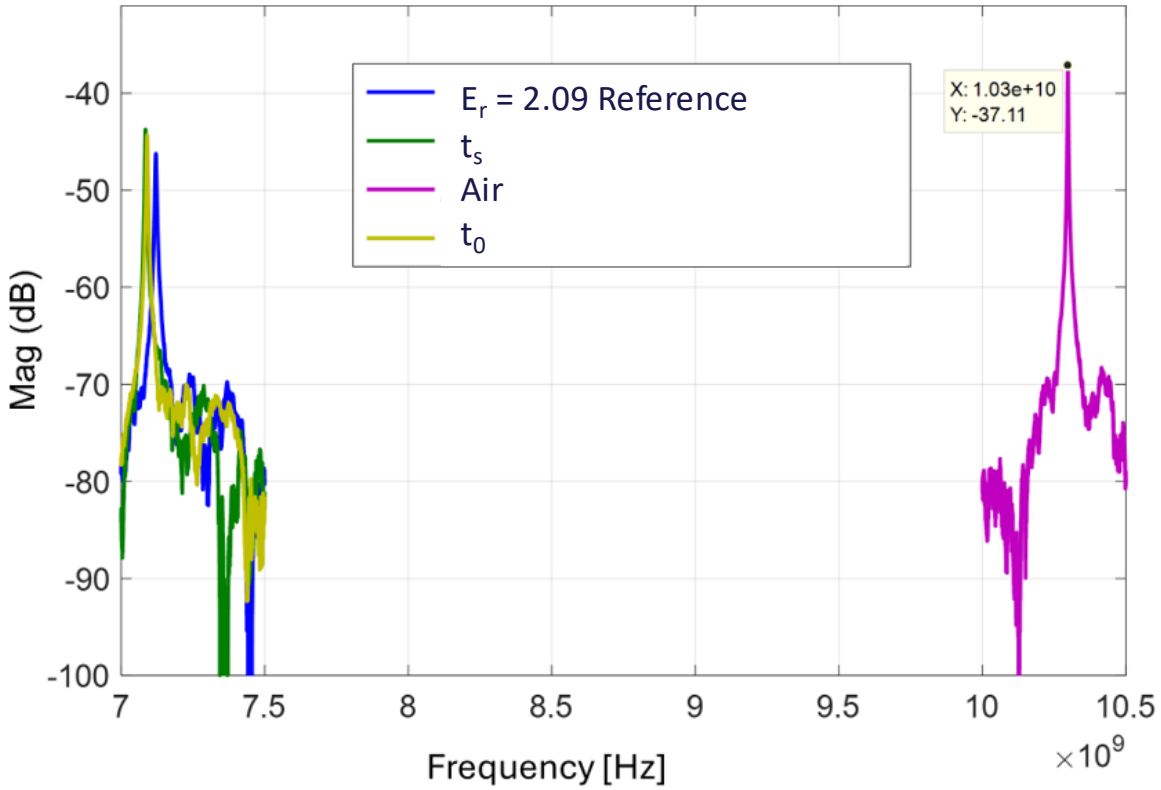
FTIR

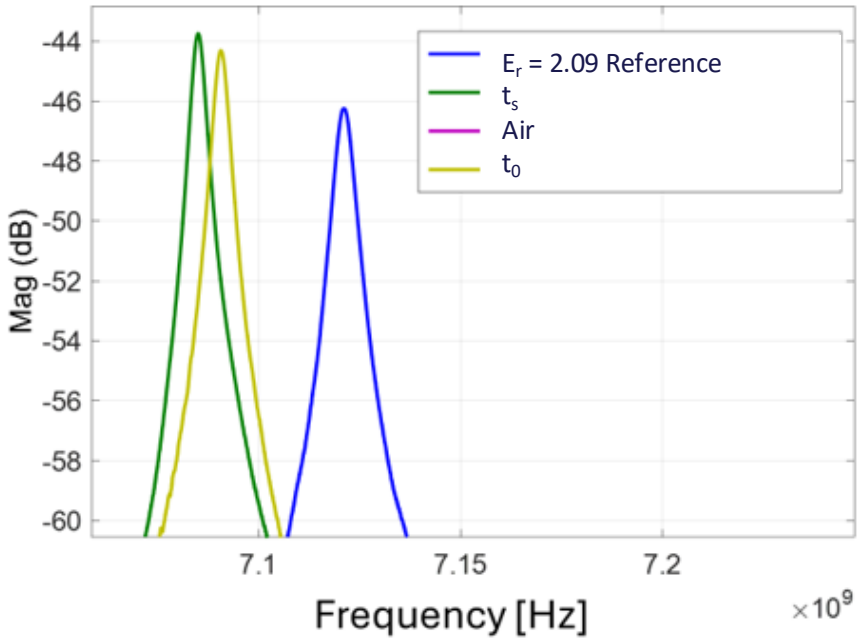


ICP-MS



IRDT: Dielectric Fluid Comparison

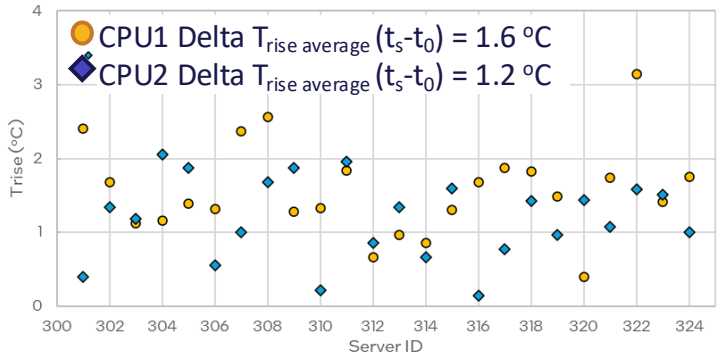




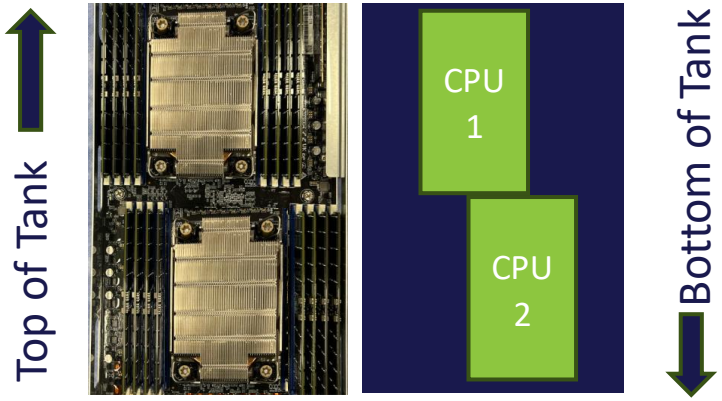
Measurement	Er	Loss Tangent	Frequency
Air	1	0	10.3 GHz
t_0	2.11	0.0004	7.1 GHz
t_s	2.11	0.0004	7.1 GHz

IRDT: Hardware Performance Analysis

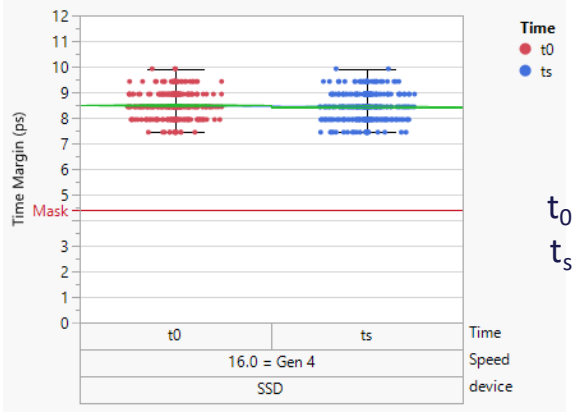
CPU Thermal Performance



CPU Configuration



PCIe SSD Timing



Mask = 4.4ps
t_0 Mean = 8.5ps
t_s Mean = 8.4ps

DDR UPM

UPM = **0** = Low Risk

System Information

Platform:	Eagle Stream
Processor:	SPR
Stepping:	*Warning
Mem Speed:	DDR5-4800
Mem Vdd:	1.145V
Topology:	1 DPC
RC Version:	*Warning
Part Number:	MTC40F2046S1RC48BA1MHCC
Margin Sample N >= 120	
DIMM Shift:	Shift >= 3

Check Status

Mem Vdd	Consistent
Topology	Supported
RC Version	Not Found
Part Number	Found one module
Margin Sample Size	Sufficient
DIMM Shift	Sufficient

DIMM S/N found in each slot:

N0.C0.D0: 24	N0.C1.D0: 24	N0.C2.D0: 24	N0.C3.D0: 24	N0.C4.D0: 24	N0.C5.D0: 24	N0.C6.D0: 24	
N1.C0.D0: 24	N1.C1.D0: 24	N1.C2.D0: 24	N1.C3.D0: 24	N1.C4.D0: 24	N1.C5.D0: 24	N1.C6.D0: 24	

*Warning: User has responsibility to confirm the validity of the data

UPM Assessment

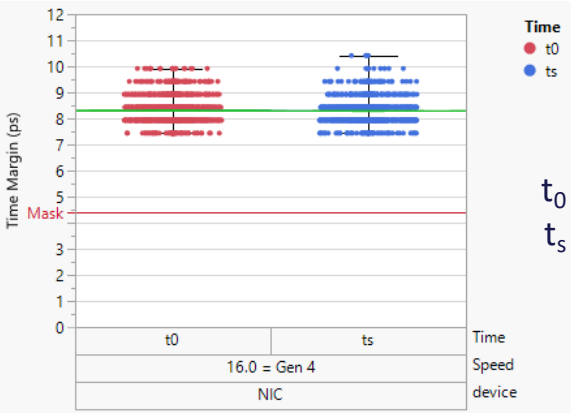
Rank	Test	Mean	Std Dev	N	MIN Margin	Bootstrap UPM
N0.C0.D0.SC0.R0	RxDqs-	20.275	0.80921686	120	18	0
N0.C0.D0.SC0.R0	RxDqs+	19.66666667	0.84349546	120	17	0
N0.C0.D0.SC0.R0	RxV-	26.26666667	1.05107655	120	23	0
N0.C0.D0.SC0.R0	RxV+	23.21666667	1.31688028	120	20	0
N0.C0.D0.SC0.R0	TxDq-	19.50833333	0.76691933	120	18	0

Benchmarks

Difference between t_0 and t_s to assess degradation

Test	Deviation	Result
Linpack	-1.0%	PASS
SPECrate	-0.8%	PASS
GSAT	+2.0%	PASS

PCIe NIC Timing



Mask = 4.4ps
t_0 Mean = 8.3ps
t_s Mean = 8.3ps

Reliability Demonstration Statistics

Mean time between failures (*mtbf*) during a continuous test can be calculated as the total test time *t* from all tested units divided by the number of failures *k*.

$$mtbf = \frac{t}{k}$$

If the unit failure rate is assumed to be constant the X^2 distribution can be used to calculate confidence intervals around a MTBF, and therefore demonstrated reliability can be extracted.

The MTBF LCL for a time truncated test, such as IRDT, is described by

$$MTBF \leq \frac{2t}{X^2_{(\alpha,2k+2)}}$$

In the case of a nonrepairable error, MTBF becomes mean time to failure MTTF.

If the assumption that the failure rate is constant is maintained, the survival probability $R(t)$ for a given service lifetime t can be estimated by the exponential distribution function

$$R(t) = e^{\left(\frac{-t}{MTBF}\right)}$$

where the reliability confidence limit is defined by the MTBF lower confidence limit.

Demonstrated Reliability of Hardware in EM DC3235

	Unit Count	Unit Hours	MTBF (80% LCL, hours)	MTBF (90% LCL, hours)	MTBF (95% LCL, hours)
Server	24	63,548	39,471	25,570	21,218
CPU	48	127,096	78,942	55,139	42,436
DIMM	384	1,016,832	631,533	441,114	339,488

Unit	Service Lifetime	Survival Probability (80% LCL)	Survival Probability (90% LCL)	Survival Probability (95% LCL)
Server	1 yr	80%	71%	66%
CPU	1 yr	89%	85%	81%
DIMM	1 yr	99%	98%	97%

IRDT Reliability Risk Assessment



Test Area	Tests Performed	Result
Package Material Compatibility	Viscoelastic Properties: Storage Modulus	HIGH RISK
	Viscoelastic Properties: Tan Delta	HIGH RISK
	Coefficient of Thermal Expansion	PASS
	Shear Adhesion	PASS
Package Reliability	Assembly Test Vehicle Reliability	PASS
	Substrate High Speed IO Reliability	PASS
System Material Compatibility	Component Visual Inspection	PASS
	Fluid Integrity: FT-IR	PASS
	Fluid Integrity: GC-MS	PASS
	Fluid Integrity: ICP-MS	PASS
iRDT: **Immersion Reliability Demonstration Testing**	Benchmark Performance Degradation	PASS
	Thermal Performance Degradation	PASS
	Signal Integrity: Rank Margin (DDR)	PASS
	Signal Integrity: Lane Margin (PCIe)	PASS
	iLVSS	PASS
	System Errors	Info Only
	Fluid Analysis: Contamination Steady State	PASS
	Fluid Analysis: Contamination Analysis	PASS
	Fluid Analysis: Degradation Analysis	PASS
Characterization	Xeon®	N/A
	System Components	PASS
Demonstrated Reliability	MTBF	Info Only
ADDL Immersion Certification		**PASS**

Call To Action

- All board components need to be compatible with the fluid — and the immersion solution needs to be tested to ensure the materials are compatible with each other.
- The industry needs to standardize methodologies to measure the reliability of hardware in an immersion solution with statistical confidence limits — and align on how to share the data.
- Contact any partner for additional information on the Intel Datacenter Certified Immersion solution

Thank You!

