Toward quantum supercomputing with IQM quantum processors

Khadijeh Sona Najafi, Ph.D.

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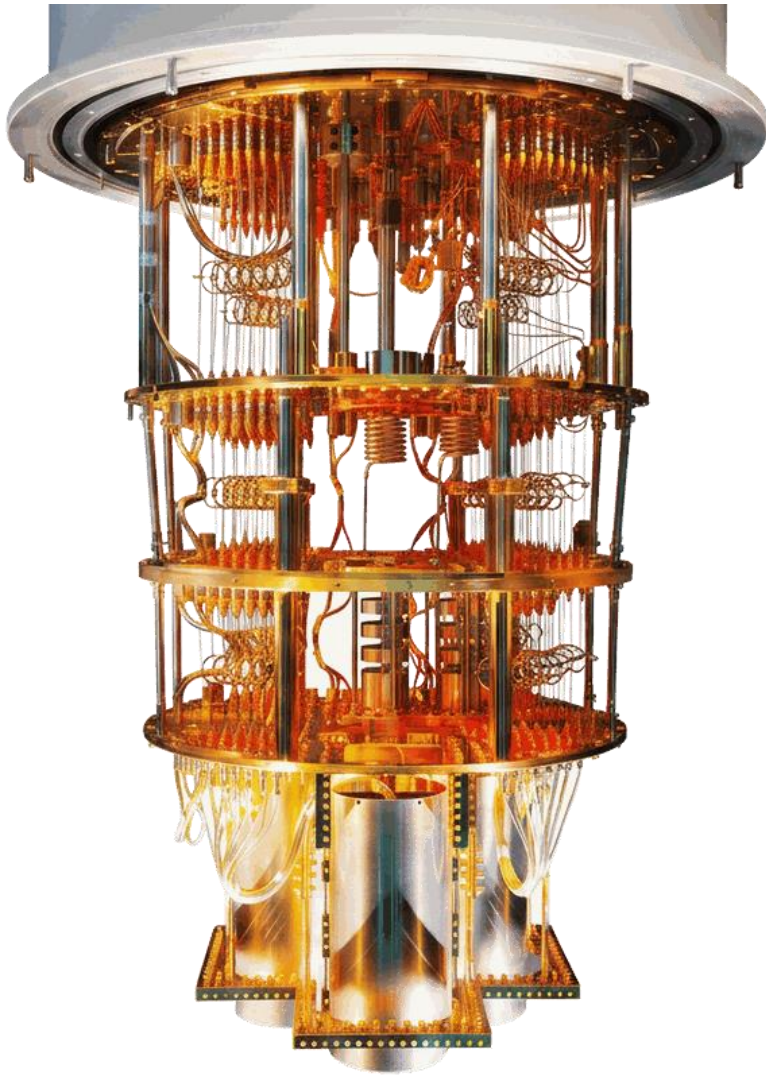


OCP FUTURE TECHNOLOGIES SYMPOSIUM

October 14, 2026
San Jose, California

IQM: Full stack quantum computers integrated with HPC

- → Algorithm and Application Development
- → Software & Workflow
- → Scalable Hardware + Error Correction + HPC Integration



Deployments drive learning and architectural progress

Q-Q fidelities 97-98%

Crystal-5
2Q fidelity
Median
99.65%
Best
99.74 ± 0.02%

Crystal-20
2Q fidelity
Median
99.76%
Best
99.85 ± 0.02%

Star-6
Retired

Crystal-54
2Q fidelity
Median
99.47%
Best
99.85%

Star-24
Q-R fidelity
CZ median
99.26%
Best
99.45%
MOVE median
99.66%
Best 99.75%

Crystal-150
Coming in 2026

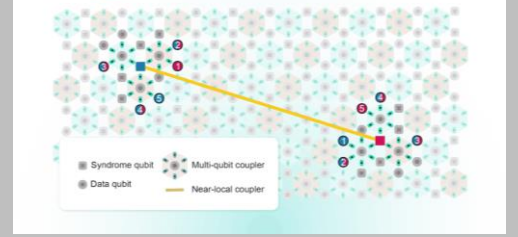
2022 2023 2024 2025 2026

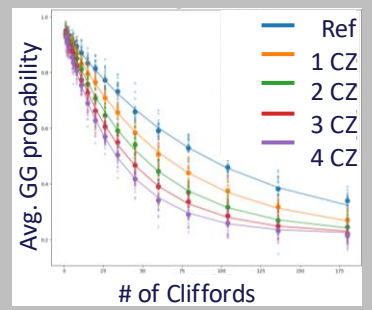
IQM Star
High connectivity
+
IQM Crystal
Parallel gates
=
IQM Constellation
Coming soon

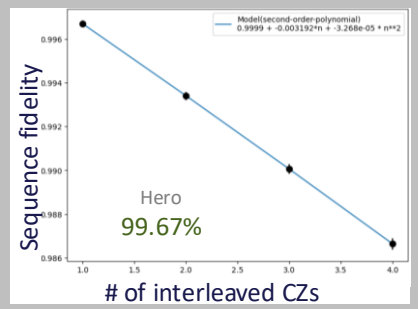
Constellation Q-Q fidelities now well beyond 99%

Theory: arXiv:2603.10699

Barbell codes. build on IQM Constellation





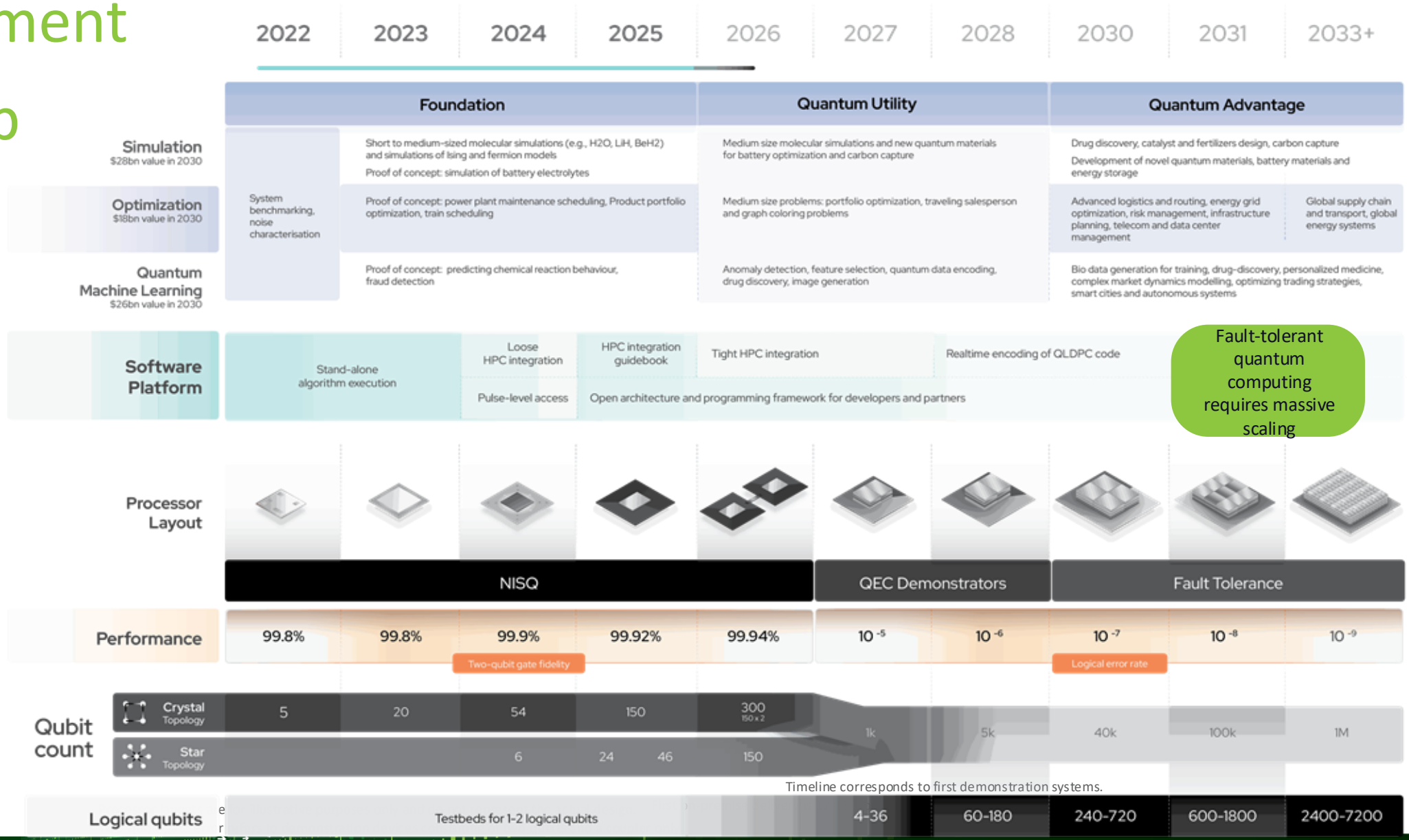


	QB1	QB2	QB3	QB4	QB5	QB6
QB1	-	99.41	99.40	99.41	99.30	99.52
QB2	99.38	-	99.44	99.35	99.10	99.49
QB3	99.41	99.49	-	99.49	99.06	99.31
QB4	98.81	99.19	99.47	-	98.53	99.32
QB5	99.13	99.13	98.59	99.07	-	99.22
QB6	99.41	99.48	99.51	99.48	99.08	-

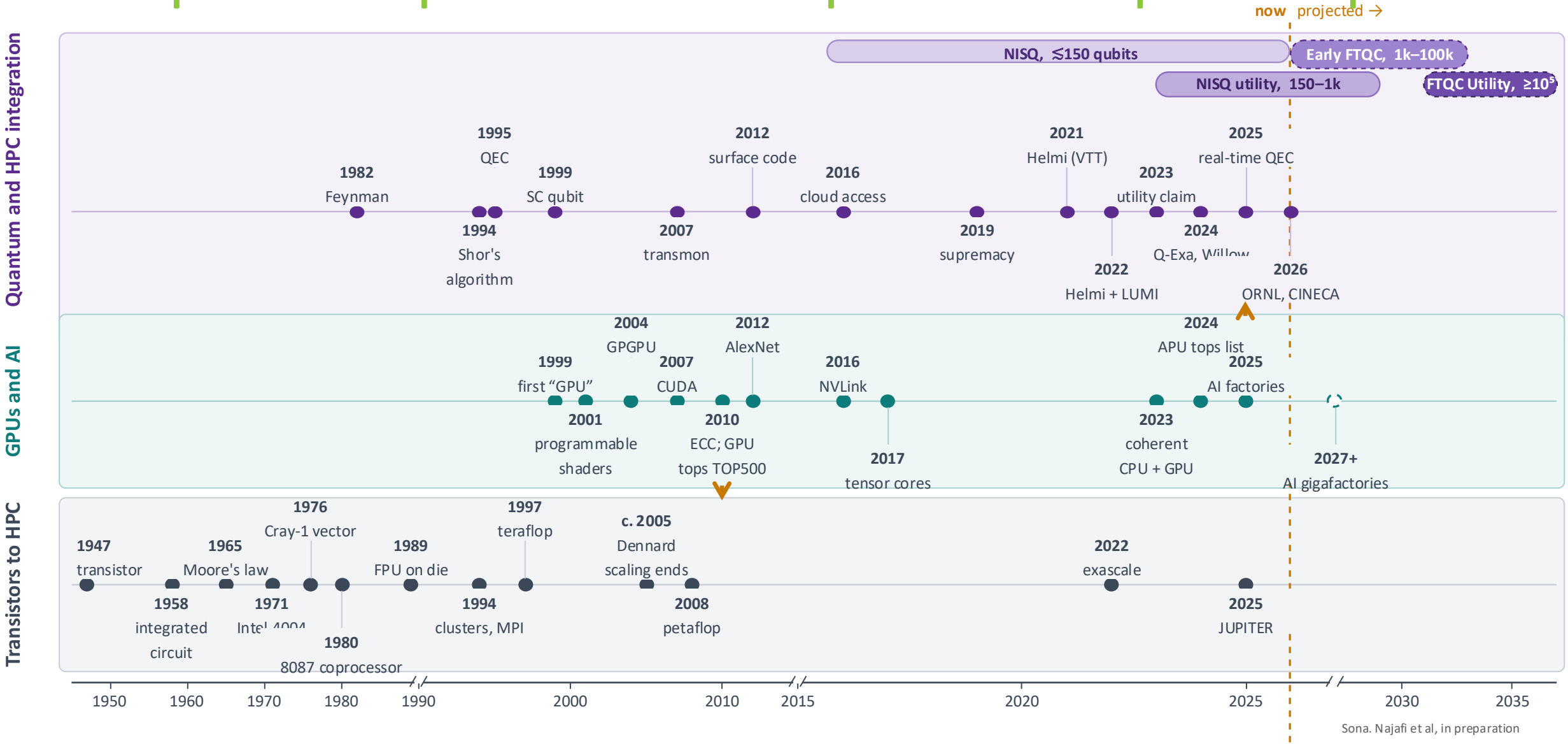
CZ median
99.37%
Best
99.52%
Hero
99.67%

Note: The timeline shows when the first-version of the QPU was developed, and the fidelities are based on the latest available data

Development Roadmap

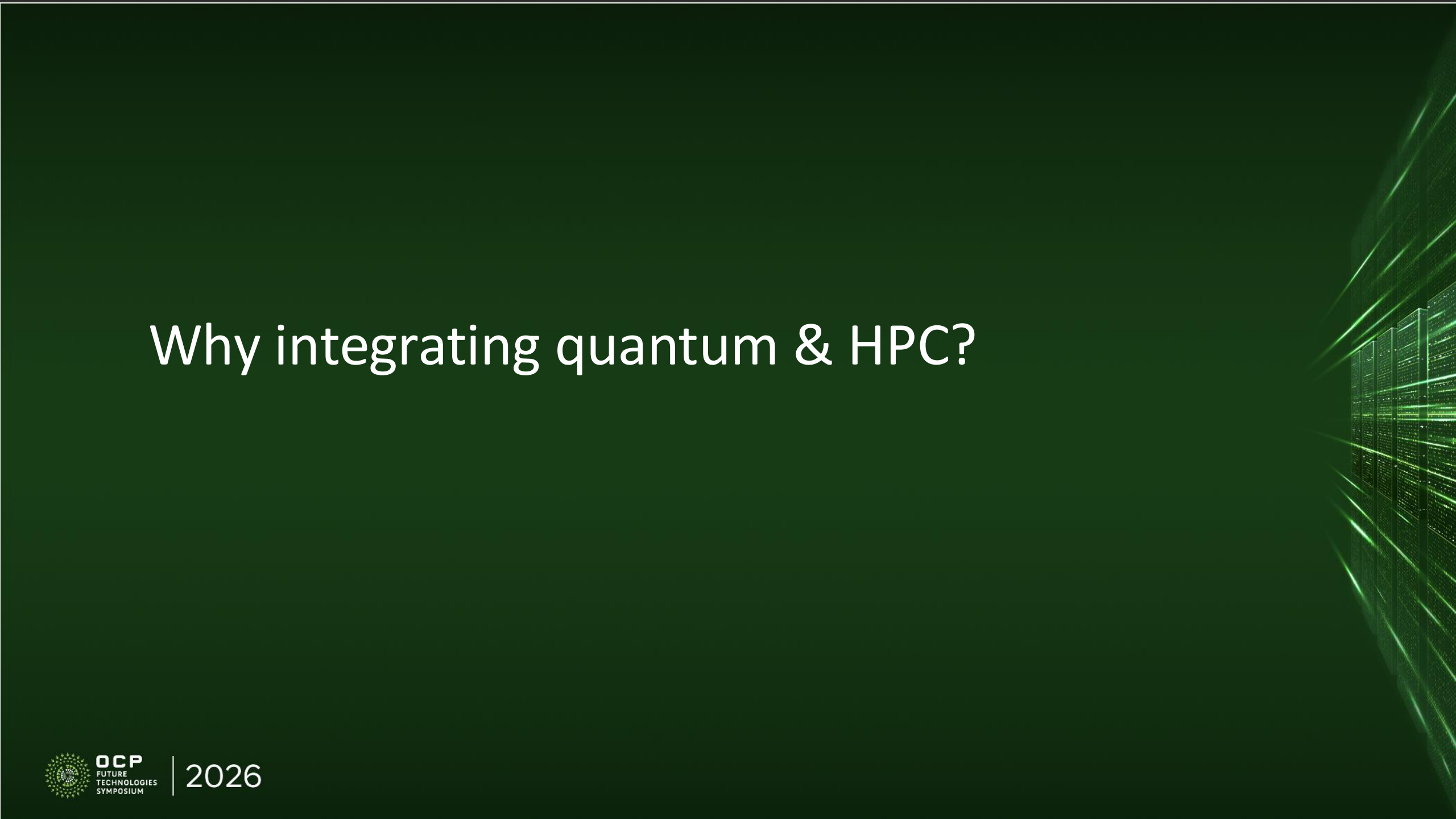


From quantum processors to quantum supercomputer



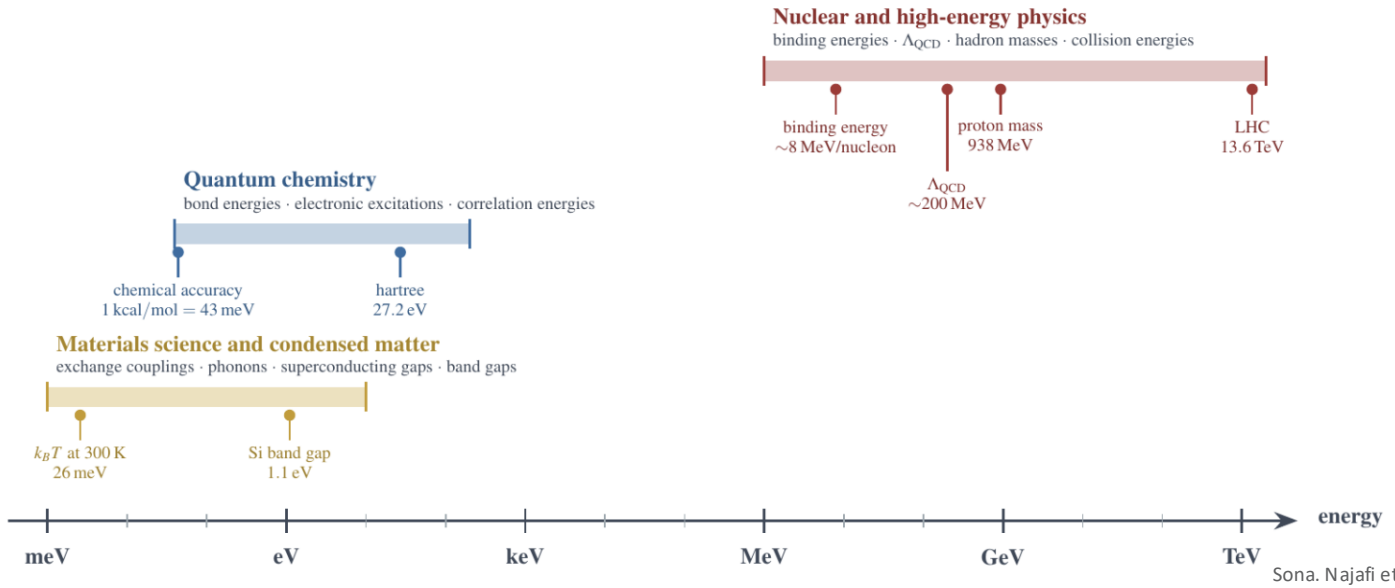
Sona. Najafi et al, in preparation

Why integrating quantum & HPC?



Demand of computing has reached beyond classical resources

- Exact solutions of many particle physical systems is computationally is challenging
- Different classical and quantum approximations such as MD,DFT, DMFT, DMRG, Quantum Monte Carlo require HPC resource
- In some regime such as strong correlation or nonlinear regimes, the approximation methods fail or do not have required accuracy



Sona. Najafi et al, in preparation

Demand of computing has reached beyond classical resources

TIER 1 · TOP OF STACK

Applications

Every target workload is a hybrid workflow, not a circuit. The classical stages set the time to solution.

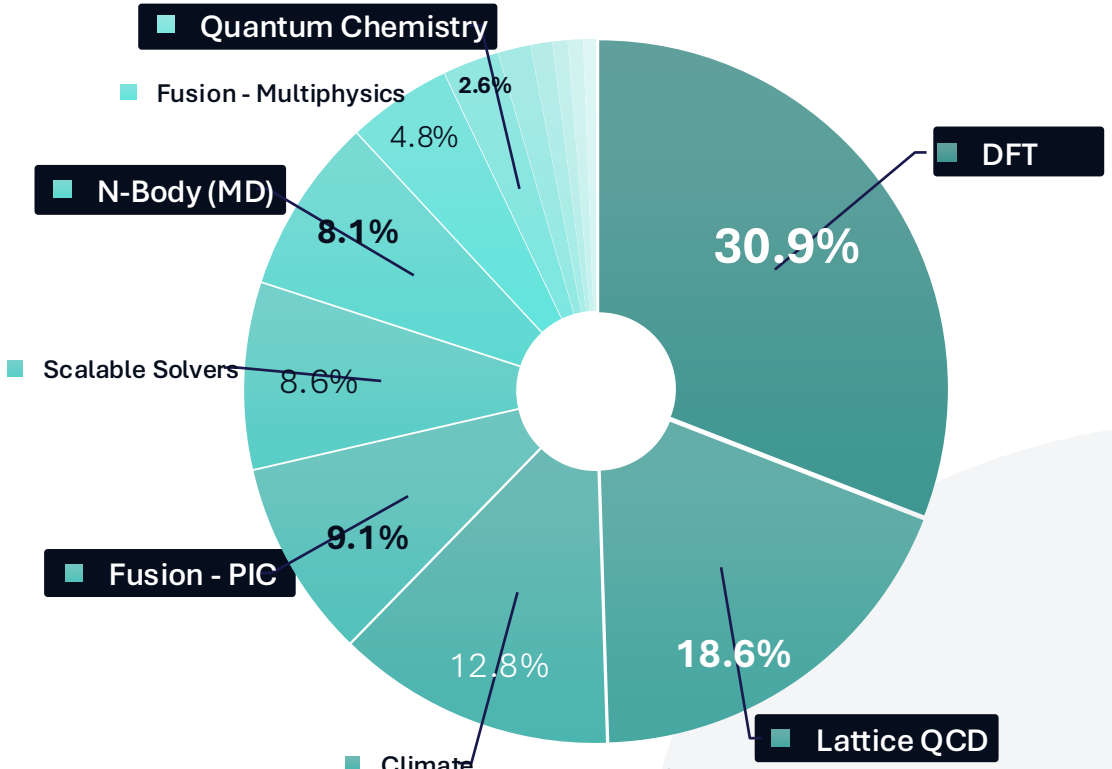
Materials science | Quantum chemistry | High-energy physics | QML | Differential equations

The first three make up over 50% of NERSC's production workload today. The same analysis proposes execution time of large-scale quantum workflows, rather than qubit count, as the parameter to optimise.

CLASSICAL DEMAND

Bulk

Large partitions, hours to days. Batch scheduling is adequate.



Tier 1: Camps et al., arXiv:2509.09882 (NERSC/LBNL, 2025) · Tiers 2–3: Seelam et al., arXiv:2603.10970 (2026)

Why integrate Quantum with HPC?

Three tiers of the stack, three independent reasons. Each generates classical work on its own, and the **character of that work changes** as you descend.

TIER 1 · TOP OF STACK

Applications

Every target workload is a hybrid workflow, not a circuit. The classical stages set the time to solution.

Materials science | **Quantum chemistry** | **High-energy physics** | QML | Differential equations

The first three make up over 50% of NERSC's production workload today. The same analysis proposes execution time of large-scale quantum workflows, rather than qubit count, as the parameter to optimise.

CLASSICAL DEMAND

Bulk

Large partitions, hours to days. Batch scheduling is adequate.

TIER 2 · MIDDLE

Mitigation and compilation

The layer that turns an unreliable device into a usable one, and the layer whose cost scales worst.

Zero-noise extrapolation | **Probabilistic error cancellation** | Noise-aware transpilation

Sampling overhead grows exponentially in the circuit error rate, so the classical burden rises faster than the qubit count. Compilation consults live calibration data, which makes it a runtime service rather than a build step.

CLASSICAL DEMAND

Burst

Many circuits per observable, seconds to minutes. Needs co-allocation and sessions.

TIER 3 · BASE

Error correction

Not a post-processing step. A classical computation running continuously, under a deadline set by physics.

Syndrome decoding | **Feed-forward** | Logical scheduling

Decoder throughput must at least match the syndrome rate or backlog grows without bound, forcing the processor to idle while further errors accumulate. Worst-case latency, not average, is the figure of merit.

CLASSICAL DEMAND

Real-time

Microseconds, inside the coherence window. Deterministic interconnect required.

Tier 1: Camps et al., arXiv:2509.09882 (NERSC/LBNL, 2025) · Tiers 2–3: Seelam et al., arXiv:2603.10970 (2026)

Integration is inevitable

	NISQ ≲150	**NISQ Scaling** 150–1k	**Early FTQC** 1k–100k	**FTQC Utility** ≥ 10^5
Applications and Algorithms	hybrid algorithms compensate for few qubits	hybrid workflows at larger scale	early fault-tolerant algorithms	algorithms expressed in logical qubits
Compilation, Error Mitigation and Pulse Control	vendor stack, local control	AI-assisted compilation; mitigation overhead	compilation to logical operations	compilation to a quantum ISA
Quantum Error Correction	demonstrators only	demonstrators only	real-time decoding on HPC and AI	decoding at scale; may migrate in-device
Physical Layer	CPU, GPU, QPU, cryogenics, wiring and control electronics: internal to the quantum + HPC system in every era			

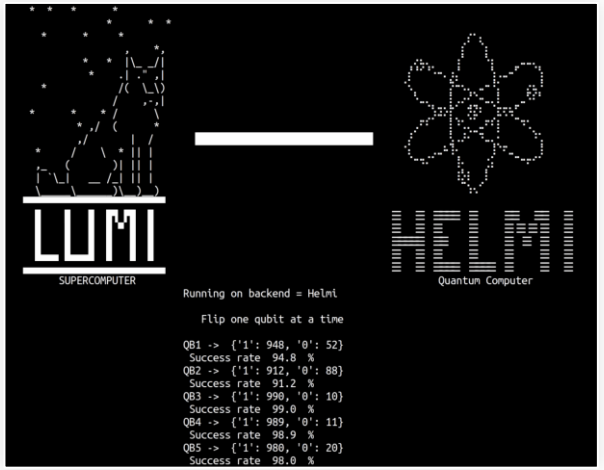
Stand-alone — Deeply integrated HPC + Quantum

Sona. Najafi et al, in preparation

How can we integrate quantum & HPC?

HPC-QC integration since 2022

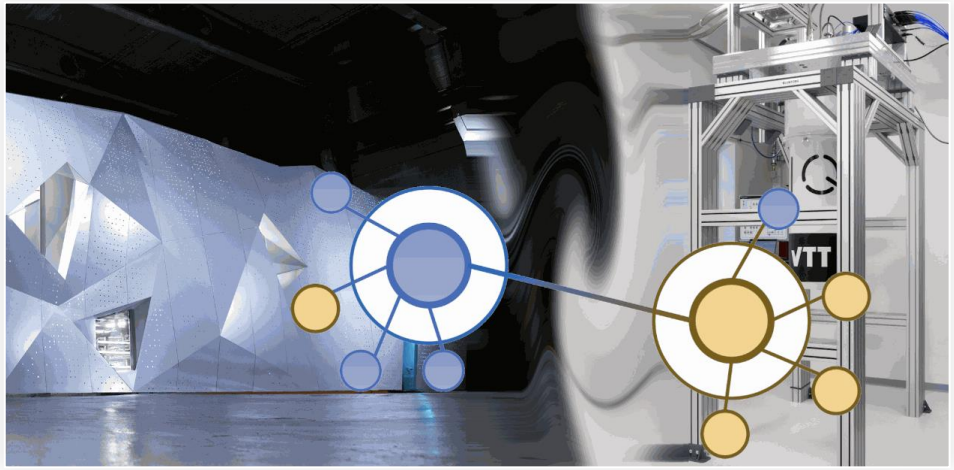
Demonstration in Slush 18.11.2022



Finland opens quantum computer for research purposes – the fusion of quantum computing and supercomputing enables completely new science

News, Press release 01.11.2022 09:00 EET

VTT's quantum computer HELMI ("Pearl") has been connected with the pan-European supercomputer LUMI ("Snow"), hosted by CSC - IT Center for Science. The connection to Europe's most powerful classical supercomputer enables the best possible use of the quantum computer's computing power. This is the first time in Europe that this kind of hybrid service connecting a supercomputer and a general-purpose quantum computer is opened for researchers.



Our HPC Guidebook

Detailed learnings from one of the first HPC+QC systems

- **Superconducting qubits** have stricter facility requirements than **HPC**, but these **can be managed by careful site selection**

- IQM Radiance 20 operated for **>150 days without any human touch** except for the weekly 5-minute liquid nitrogen refill.

Download the article to learn more!
https://arxiv.org/abs/2509.12949



First Practical Experiences Integrating Quantum Computers with HPC Resources: A Case Study With a 20-qubit Superconducting Quantum Computer

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arXiv:2509.12949v1 [quant-ph] 16 Sep 2025

Abstract

Incorporating Quantum Computers into High Performance Computing (HPC) environments (commonly referred to as HPC+QC integration) marks a pivotal step in advancing computational capabilities for scientific research. Here we report the integration of a superconducting 20-qubit quantum computer into the HPC infrastructure at Leibniz Supercomputing Centre (LRZ), one of the first practical implementations of its kind. This yielded four key lessons: (1) quantum computers have stricter facility requirements than classical systems, yet their deployment in HPC environments is feasible when preceded by a rigorous site survey to ensure compliance; (2) quantum computers are inherently dynamic systems that require regular recalibration that is automatic and controllable by the HPC scheduler; (3) redundant power and cooling infrastructure is essential; and (4) effective hands-on onboarding should be provided for both quantum experts and new users. The identified conclusions provide a roadmap to guide future HPC center integrations.

CCS Concepts

• Hardware → Quantum computation; • Applied computing → Data centers; • Social and professional topics → Computer manufacturing; Hardware selection; Management of computing and information systems.

Keywords

Quantum computing, high-performance computing, hybrid workflows, superconducting qubits, HPC+QC Integration, HPCQC, site selection

ACM Reference Format:

Eric Mansfield, Stefan Seegerer, Panu Vesanen, Jorge Echavarria, Burak Mete, Muhammad Nufail Farooqi, and Laura Schulz. 2025. First Practical Experiences Integrating Quantum Computers with HPC Resources: A Case Study With a 20-qubit Superconducting Quantum Computer. In Proceedings of International Workshop on Software Frameworks and Workload Management for Quantum and HPC Ecosystems (SFWM). ACM, New York, NY, USA, 9 pages. https://doi.org/10.1145/3731599.3767551

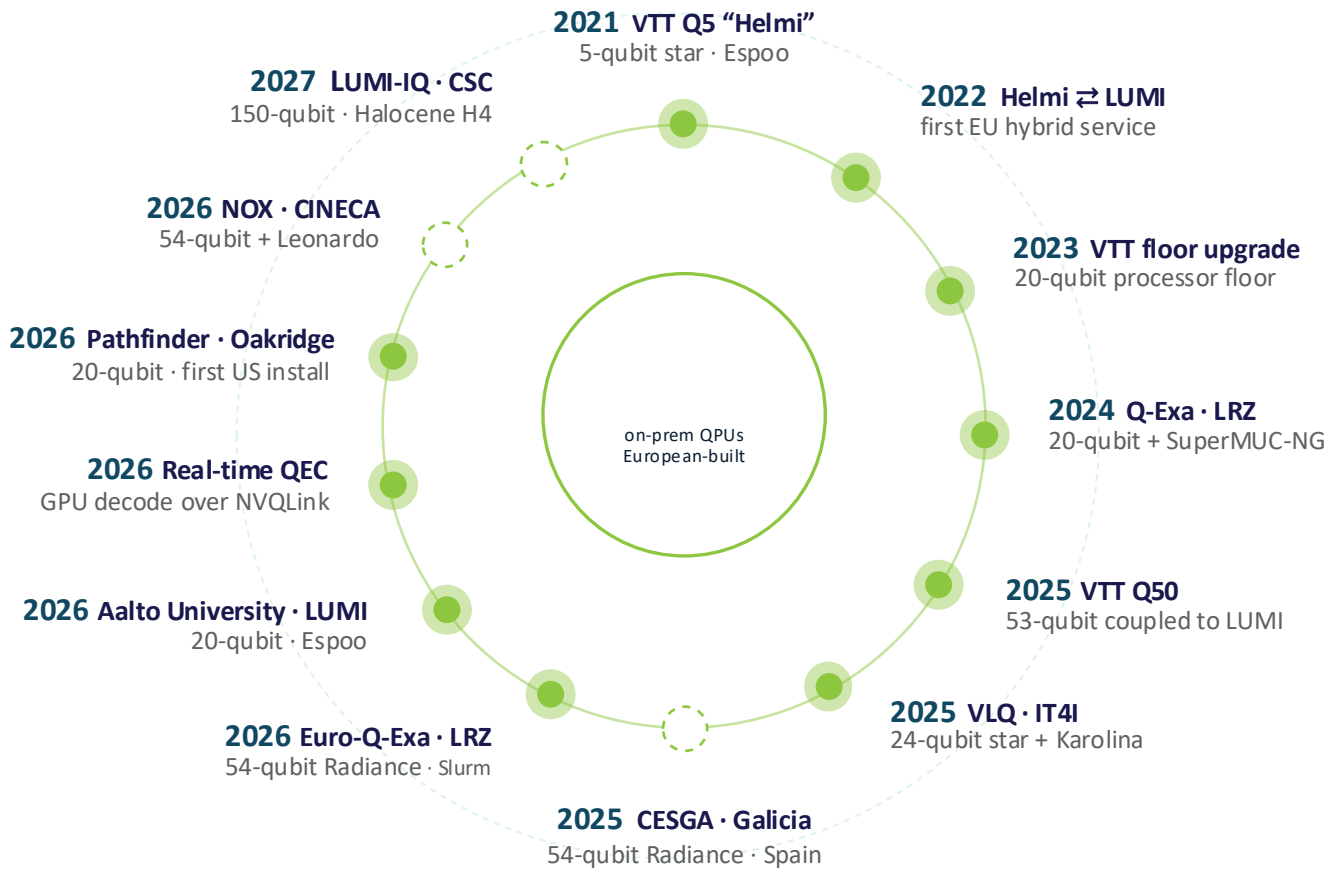
1 Introduction

Quantum computers, leveraging the principles of quantum mechanics, offer unique capabilities for solving specific problems that are intractable for classical systems. These include chemistry simulation, combinatorial optimization, and machine learning, where quantum systems could provide exponential speedups or energy efficient solutions. Classical computing, particularly High Performance Computing (HPC), is well-suited for parallelized problems with large datasets ("big data"). Quantum Computing can complement the capabilities of HPC by enabling specific High Performance Computing+Quantum Computing (HPC+QC) workflows, a series of steps, that combine the unique strengths of both classical and quantum computing to create new methods for scientific computing

Appeared in: 1st International Workshop for Software Frameworks and Workload Management on Quantum and HPC Ecosystems. ACM: Workshop at SuperComputing 2025, St. Louis, MO, USA.

Already integrated with 11 quantum supercomputer

IQM leads quantum–HPC integration



Deployment status:

- Integrated
- Contracted, not yet delivered

Sona. Najafi et al, in preparation

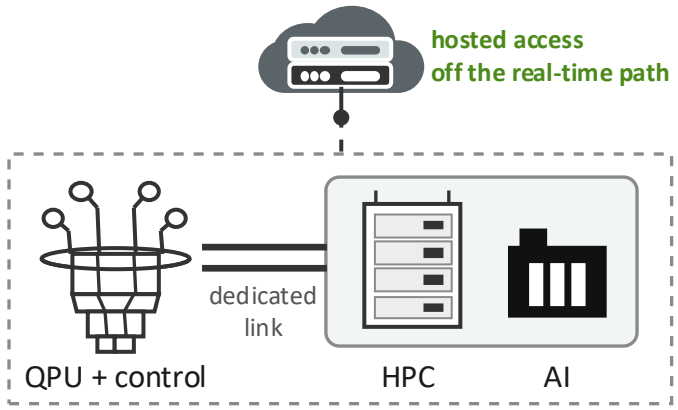
Three regime of integration

TIER T

Tight

real-time, ≲100 µs

ONE TIMING DOMAIN



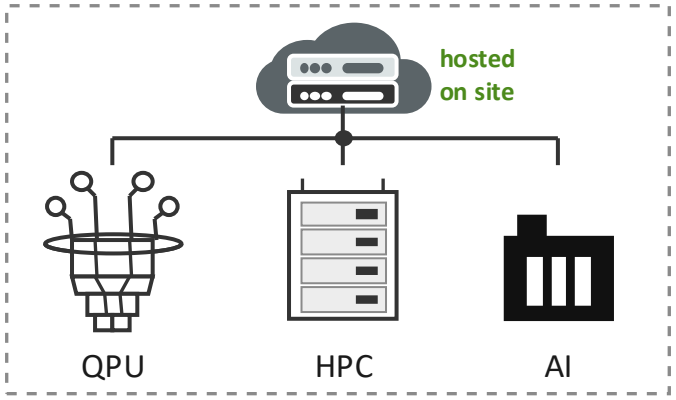
The decoder sits inside the coherence budget. No scheduler, no shared network and no general-purpose operating system may appear on this path.

TIER M

Intermediate

co-scheduled, 0.1 ms – 1 s

ONE ALLOCATION, ONE SCHEDULER



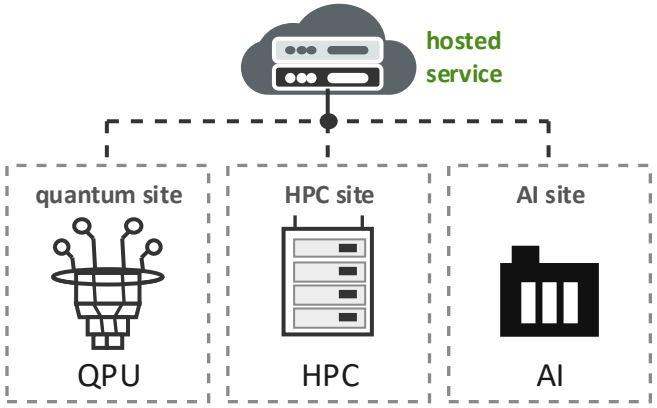
Quantum and classical resources are held in a single job. The scheduler must see device availability and calibration state as first-class attributes.

TIER L

Loose

federated, ≳1 s

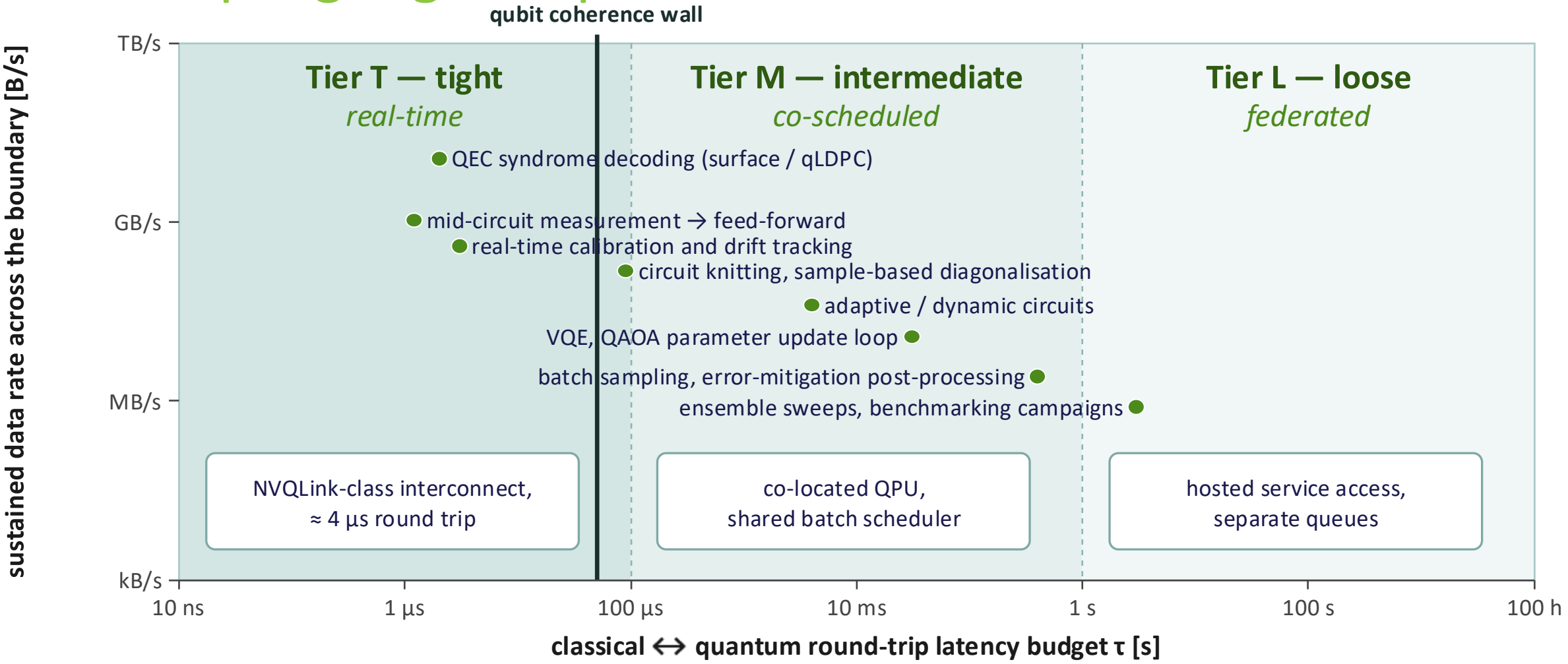
SEPARATE SITES, HOSTED ACCESS



Access is a service across an institutional boundary. What remains hard is identity, accounting, data movement and the reconciliation of two queues.

Sona. Najafi et al, in preparation

The coupling regime space



Each regime is a different engineering problem: Tier T an interconnect problem, Tier M a scheduler problem, Tier L a federation and identity problem. Solving one does not solve the others.

Sona. Najafi et al, in preparation

A reference architect for quantum supercomputer

1 Applications — Quantum simulation · Quantum AI · Optimisation · PDEs

I1 workflow definition

2 Algorithms & kernels *quantum and classical methods*

QUANTUM: NISQ: VQE, QAOA, QNN · FTQC: QPE, Grover, Shor — Qrisp . Qiskit · Cirq · PennyLane · CUDA-Q

CLASSICAL: DFT · DMFT · DMRG · QMC — BLAS · ITensor · Quantum ESPRESSO

I2 job submission

3 Orchestration — Scheduler · Workflow manager · Gateway / API · Accounting & identity

I3 resource allocation

4 Hybrid compilation & runtime *what each device executes*

NISQ toolchain: transpilation · mitigation · post-processing

FTQC toolchain: FT compiler · emulator · assembler

Classical toolchain: LLVM · CUDA / HIP · MPI

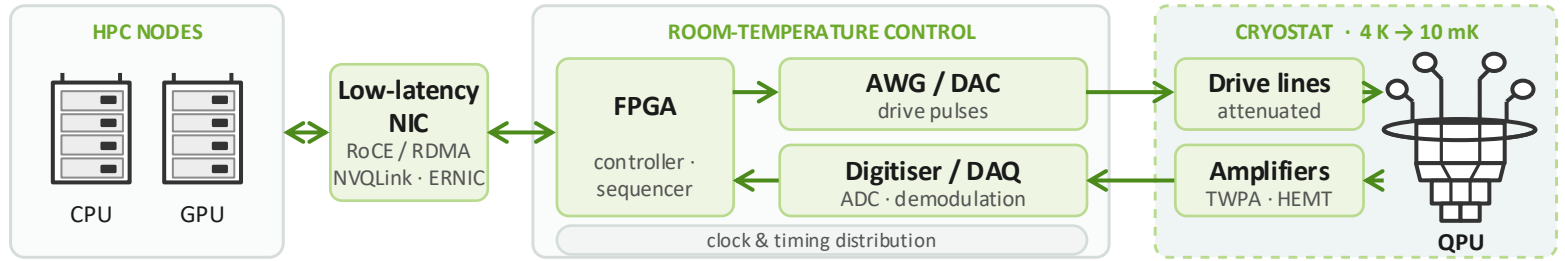
shared IR (MLIR) · hybrid runtime: CUDA-Q, Catalyst + Backline

I4 device interface (QDMI)

5 Device interface & control *firmware on the control path* — Quantum device interface · Pulse sequencing · Primary decoder · NVQLink · Backline link

I5 control, readout & deterministic link

6 Hardware resources *connected in signal order*



CROSS-CUTTING

Calibration, telemetry & feedback

- calibration state
- device telemetry
- monitoring & logging
- AI-assisted tuning and decoding
- provenance for results

state flows up, corrections flow down

Sona. Najafi et al, in preparation

Applications of quantum supercomputer

Applications of quantum supercomputer

In every one of these flows the QC is accelerator and the HPC/AI cluster carries the load

01 · QUANTUM CHEMISTRY

Next-generation batteries

Volkswagen Group × IQM

- Hybrid AFQMC models Li-ion electrolyte breakdown
- Chemical accuracy using 13 of 32 qubits

02 · BIOLOGY & HEALTH CARE

Cancer drug research

Algorithmiq × IQM

- Energy gaps of BODIPY photosensitizers on IQM Emerald (54 qubits)
- ~100× better precision than another superconducting QPU



Quantum + HPC + AI

03 · AI FOR QUANTUM

Error-correction decoders

AI cluster beside the QPU

- GPU-trained neural decoders turn syndromes into corrections
- Low-latency inference beside the cryostat

04 · QUANTUM FOR AI

Quantum machine learning

Global insurance company

- Quantum kernels flag anomalous behaviour for fraud detection
- Quantum transformers: comparable accuracy, fewer parameters

05 · PDE

Physical simulation

- Navier–Stokes, plasma, heat and ion transport
- Black–Scholes pricing and seismic waves

Sona. Najafi et al, in preparation

Towards simulation of next generation batteries



- Battery materials are strongly-correlated

Approximations cannot capture the behavior of strongly-correlated systems, such as battery materials

Need to understand the reaction pathways



- Computational cost too high for practical use

QC-AFQMC is a hybrid method that is a quantization of a promising classical method. While efficient, it is still too slow for any practical chemical system



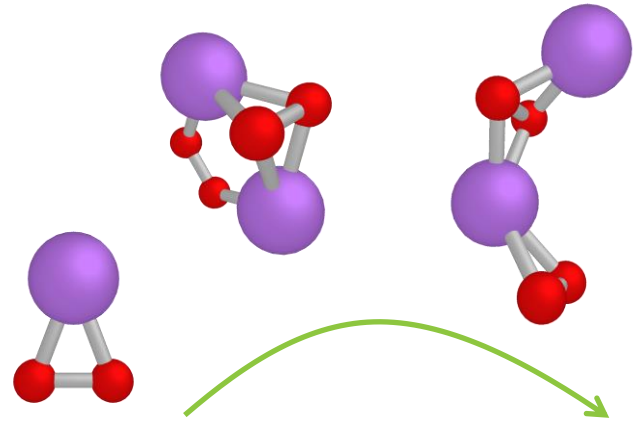
- Improved SOTA runtime estimates by 248x using LUMI supercomputer

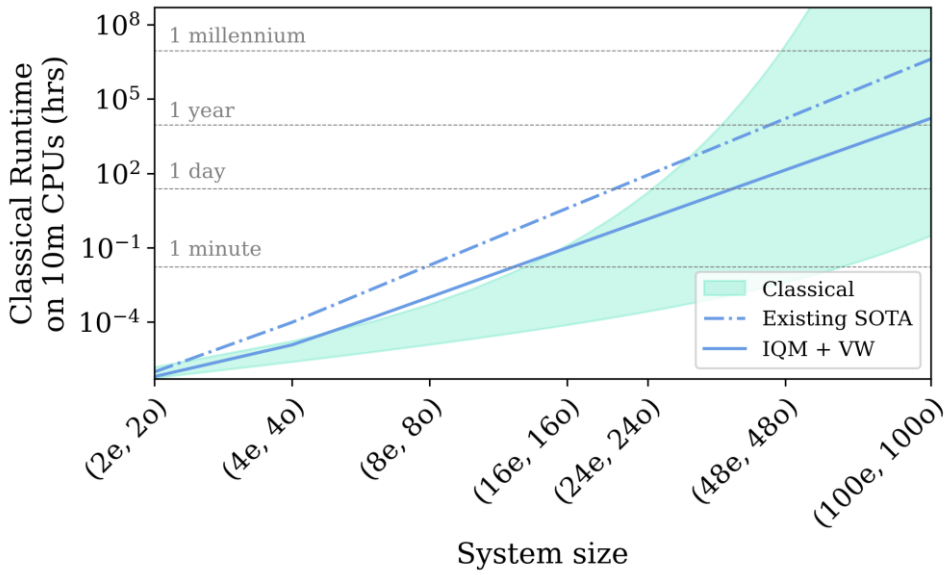
Combining algorithmic and implementation improvements, we bring the projected runtime for a 100-orbital system down to a couple years from half a millennium



- Largest demonstration of this hybrid method

Contextualize the work with a reaction pathway for lithium-air batteries that fitted to 40 qubits



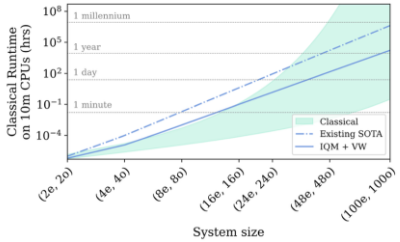


arXiv:2606.19239

Examples of hybrid workflows on IQM machines

BATTERY CHEMISTRY · VW × IQM

Towards simulating next-generation batteries



THE PROBLEM

Battery materials are strongly correlated, so approximations miss their reaction pathways. Hybrid QC-AFQMC captures them, but its classical post-processing was too slow for practical systems.

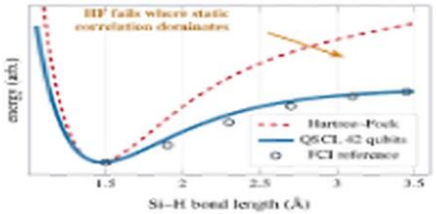
THE RESULT

Algorithmic and implementation gains cut projected runtime **up to 248×**: a 100-orbital system drops from ~500 years to ~1.8 years on 10M CPU cores. Largest run: a **lithium-air (Li_2O_4) pathway on 40 qubits** (simulated data, LUMI).

Nappi et al., arXiv:2606.19239

INDUSTRIAL CHEMISTRY

Compact wavefunctions from quantum-selected CI



THE PROBLEM

Selected CI needs a configuration subspace that is both small and well chosen. Sampling it is classically hard exactly where static correlation matters, at bond dissociation.

THE RESULT

Potential energy curve of silane, SiH_4, on **42 qubits**. At large separation the subspace is **over 200× smaller** than conventional SCI with comparable energies. Final energies are solved on HPC, so hardware noise never enters.

Weaving et al., arXiv:2509.02525

SOLUTION CHEMISTRY

Subspace, embedding and classical MD combined



THE PROBLEM

A reaction in solution can span ~10^5 atoms. Almost none need quantum treatment, but deciding which do, and handing them over cleanly, is the hard part.

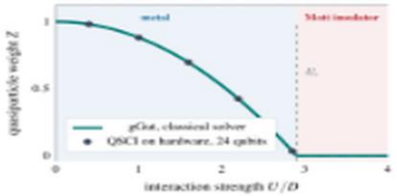
THE RESULT

Proton transfer (solvated Zundel cation) through a multiscale workflow: classical MD, projection-based embedding and qubit-subspace reduction feeding **QSCI on a QPU**. Run on IQM's 20-qubit Q-Exa with LRZ compute.

Bickley et al., arXiv:2505.16796

MATERIALS SCIENCE

Quantum-assisted ghost Gutzwiller ansatz



THE PROBLEM

Ghost Gutzwiller matches dynamical mean-field theory at lower cost, but is bottlenecked by the embedding density matrix, which must converge in a self-consistent loop.

THE RESULT

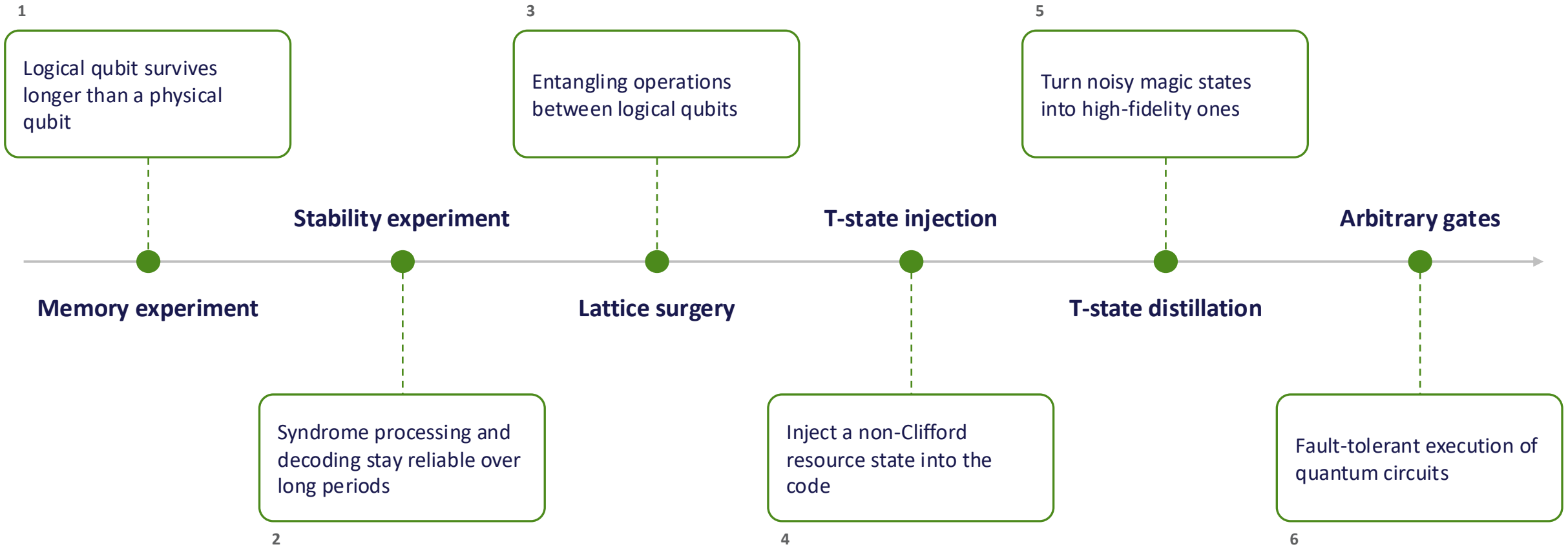
The metal-to-insulator transition of the Fermi-Hubbard model on a Bethe lattice, captured with **24 qubits** and 11 ghost orbitals on IQM Garnet, using an SCI basis of as little as **1% of the CI states**.

Sriluckshmy et al., arXiv:2506.21431

The path toward FTQC

The path toward fault-tolerance

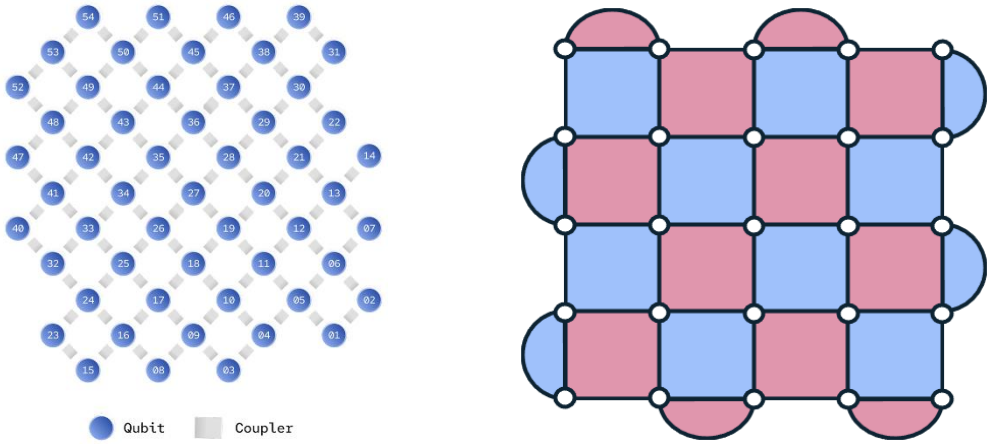
The first institutions to demonstrate lattice surgery at scale, publish decoder benchmarks and build production-grade QEC tooling will define the standards the field builds on.



Beyond the surface code

WELL-KNOWN OPTION

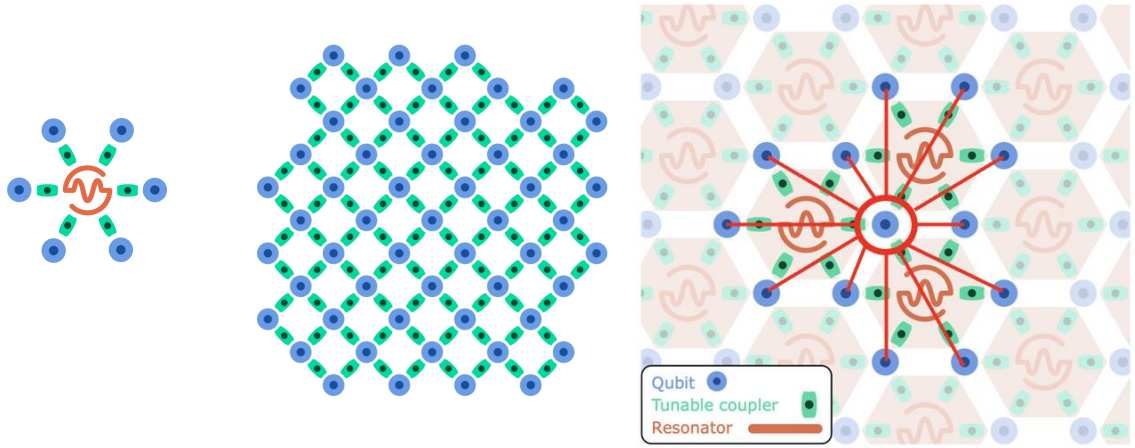
Square grid + surface code



- 4 neighbours per qubit: ideal for the surface code, inefficient for colour codes or qLDPC
- Needs a vast number of physical qubits to protect a few logical qubits

NEW HARDWARE COMPONENTS

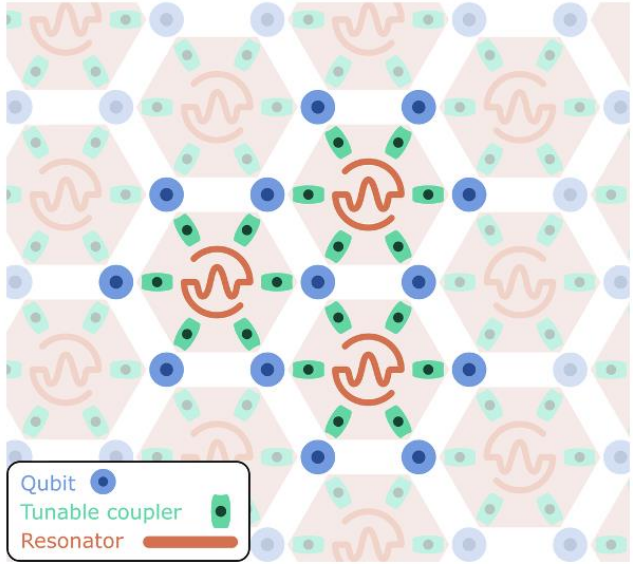
Connectivity beyond the square grid



- **IQM Star**: high connectivity through a central resonator, but limited parallelism slows QEC cycles at scale
- Tunable couplers + resonators give each qubit many native partners

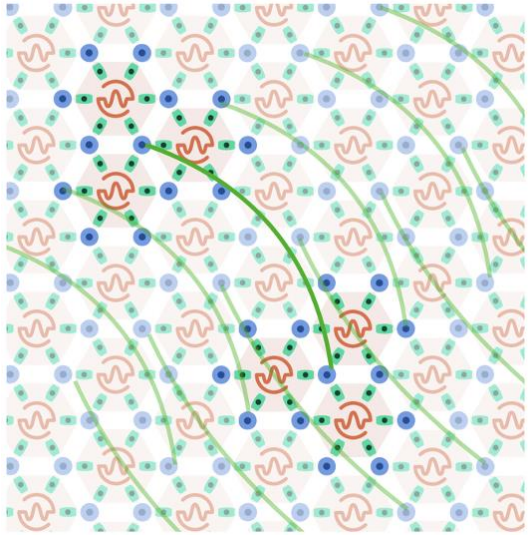
IQM constellation and barbell code

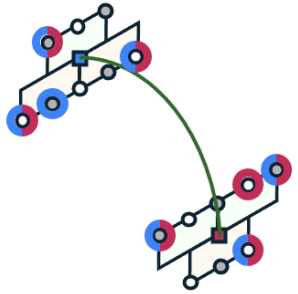
HARDWARE · CONSTELLATION TOPOLOGY



- **12 native neighbours** per qubit, instead of 4 on a square grid
- High parallelism with high-fidelity two-qubit gates
- A platform to research **new QEC codes** such as quantum LDPC (qLDPC)

CODE · BARBELL qLDPC





A "barbell"

Few near-local long couplers (one per every other qubit) join planar Constellation sites

- Limited number of **near local couplers**
- Hardware complexity stays constant as code distance grows
- 8x lower cost in resources, high efficiency compared to rotated surface code
- 30 physical qubit to 1 logical qubit

Choe et al., Barbell Codes: qLDPC Codes for Superconducting Quantum Hardware, arXiv:2606.06062 (2026). Circuit-level noise simulations; surface-code comparisons per IQM announcement, 9 June 2026.

Introducing IQM Halocene

The next-generation product line for quantum error correction research

QEC RESEARCH: UNTIL NOW A CLOSED FIELD

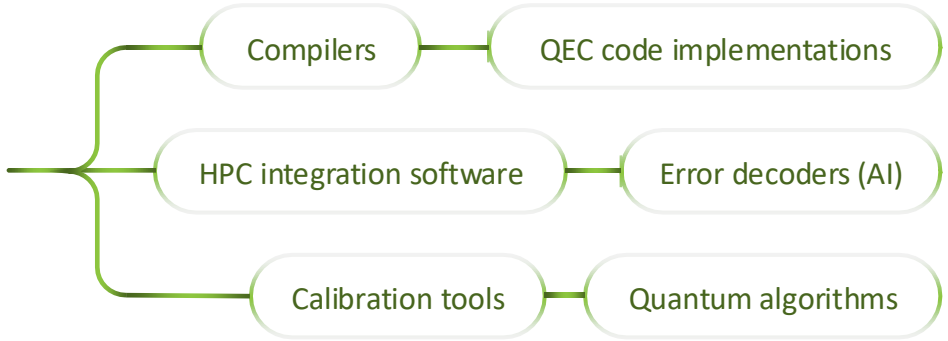
- Meaningful QEC experiments have run only on proprietary systems, out of reach of the HPC community
- Halocene puts this research **in the hands of HPC centres**: learn, educate, research and create IP on the path to fault tolerance

150
qubits in the first system; installs from end of 2026

5
logical qubits for research, with Clifford gates

Open
QEC stack, modular decoders

Build **commercial applications** across key domains





What is next for quantum supercomputer?



TIER 1 · APPLICATIONS

New algorithms, not ported ones

The algorithms that will use a 1000-qubit machine coupled to an HPC centre have not been written. Existing ones were designed for a device in isolation, and must be rediscovered for the hybrid setting.

algorithm discovery | workflow adoption

TIER 2 · MITIGATION AND COMPILATION

Tools that survive the next decade of scale

Mitigation overhead grows faster than the device. Above 100 qubits, compilation and characterisation need **AI-assisted methods** to stay tractable, plus workflow integration that makes the QPU a scheduled resource.

AI-assisted compilation | workflow integration

TIER 3 · HARDWARE AND FACILITY

QPU scaling and the AI factory

Scaling 150 to 1000 physical qubits needs new technology, not more of the same. In parallel, the QPU has to be integrated into facilities being built around **quantum, HPC and AI together**.

QPU scaling | HPC + AI factory integration

Join the Future Of Supercomputing



Sona Najafi, Quantum Solution Manager
sona.najafi@iqm.tech

OCP FUTURE TECHNOLOGIES SYMPOSIUM

October 14, 2026
San Jose, California

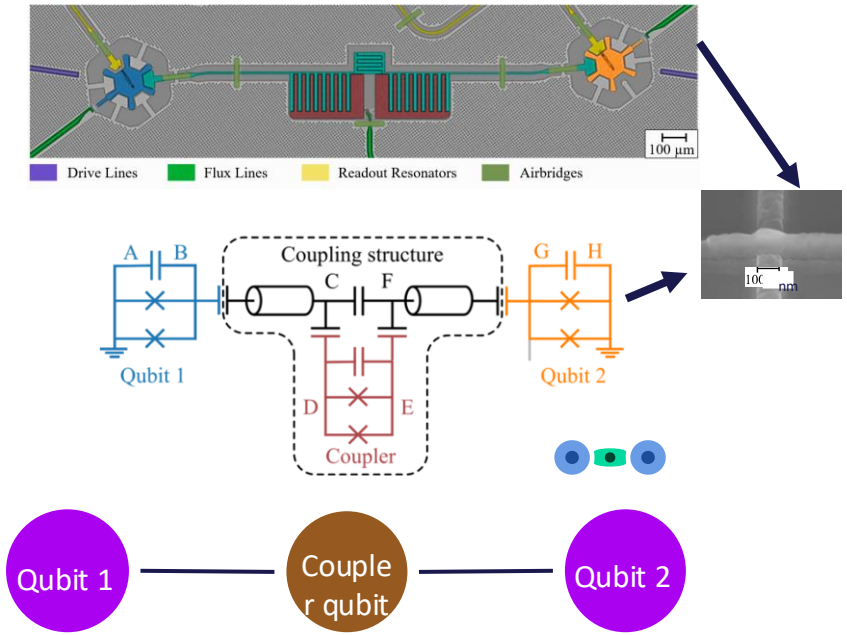




OCP FUTURE TECHNOLOGIES SYMPOSIUM | 2026

Superconducting qubits and processors

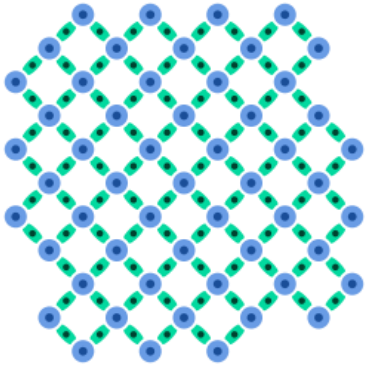
Superconducting qubits as building blocks for quantum information processing

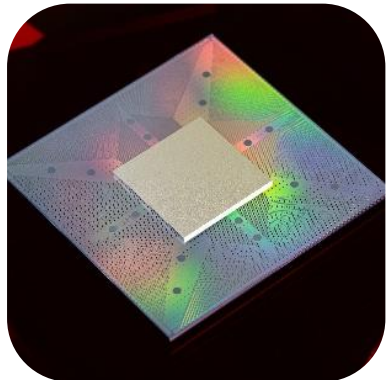


Coupled structure with two qubit; schematics and microphotographs.

Superconducting quantum processor structure

- Superconducting QPUs are high-end microwave ICs (4 – 8 GHz)
- Superconducting ultra-low-loss thin-film structures (CD ≥ 1 µm) as on-chip microwave building blocks
- Josephson junctions as core qubit elements
- Infrastructure for high-performance microwave connectivity





Quantum processing unit (QPU) as “artificial atom” lattice. Example topology of IQM Crystal-54 with 54 qubits and 90 couplers.

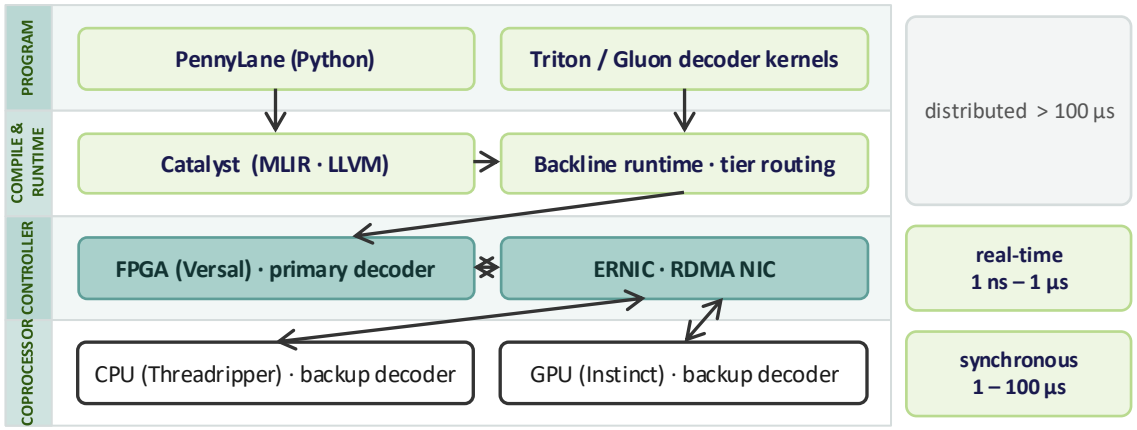
F. Marxer et al., PRX 4, 010314, 2023

Real time couplings

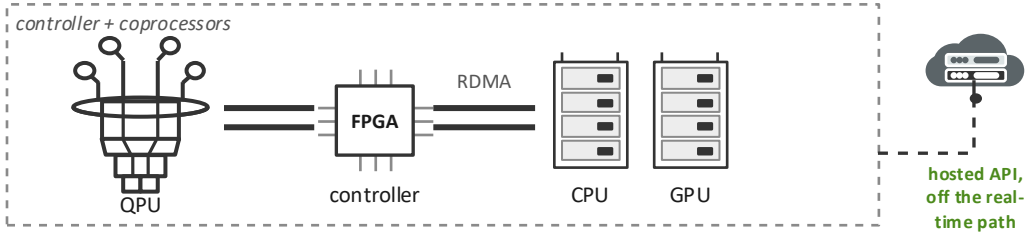
(a) Backline

Xanadu · AMD

TIER T · HETEROGENEOUS COPROCESSING



RESOURCES

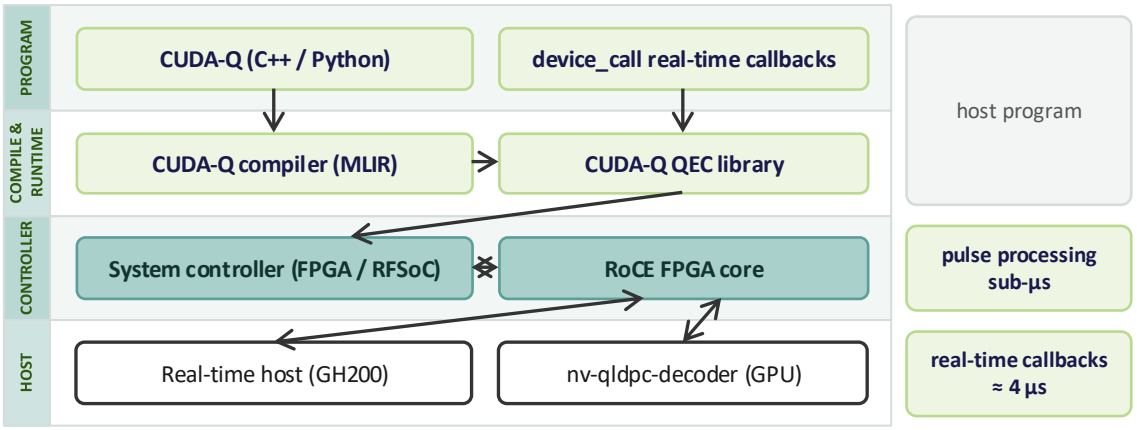


mean round trip, FPGA → coprocessor → FPGA: 2.3 µs (CPU) · 4.4 µs (GPU)

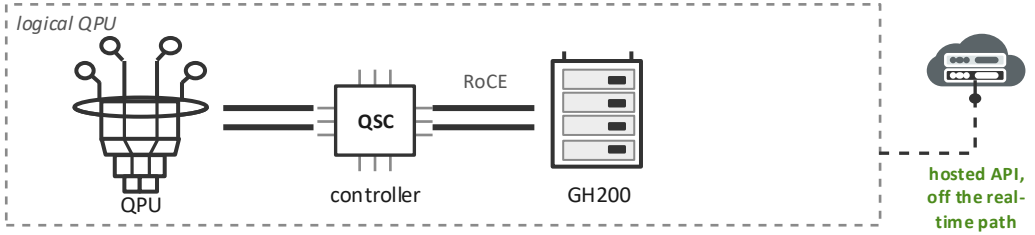
(b) NVQLink

NVIDIA · Quantinuum · IQM with Zurich Instruments

TIER T · LOGICAL QPU



RESOURCES



mean round trip over RoCE: 3.84 µs (σ = 0.035 µs, n = 1000)

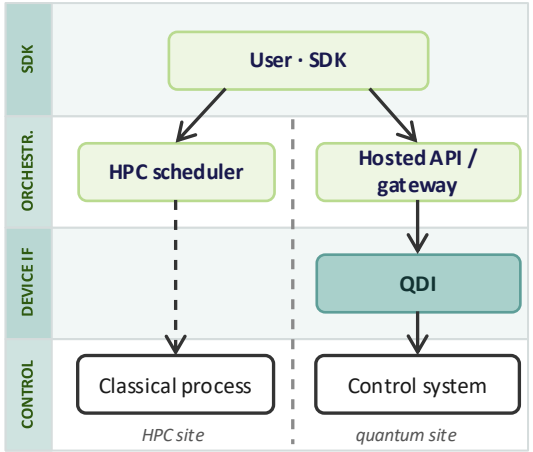
Both place classical decoding inside the timing domain of the processor; they differ in the coprocessor and in the programming path from the host language to the controller.

Sona. Najafi et al, in preparation

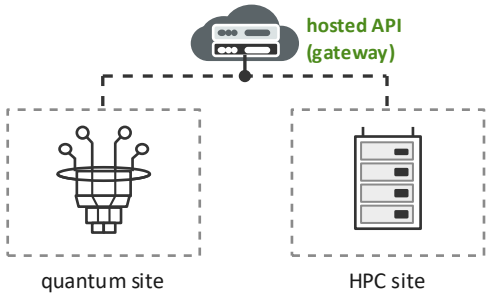
Deployment variant of quantum supercomputer

(a) Gateway access

TIER L · SEPARATE SITES

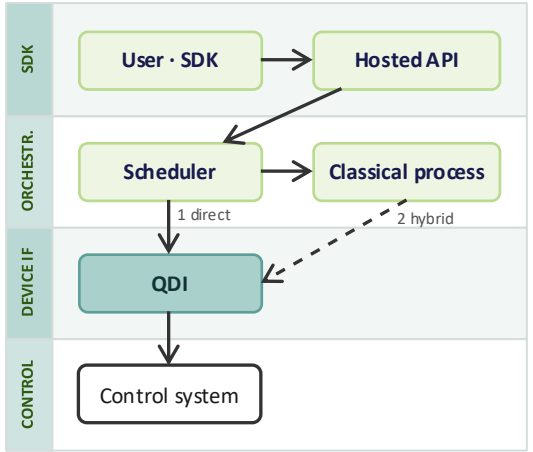


RESOURCES

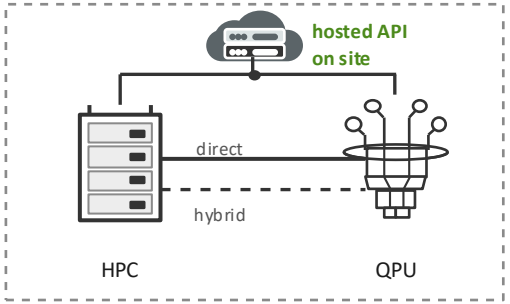


(b) Scheduler-integrated

TIER M · 1:1

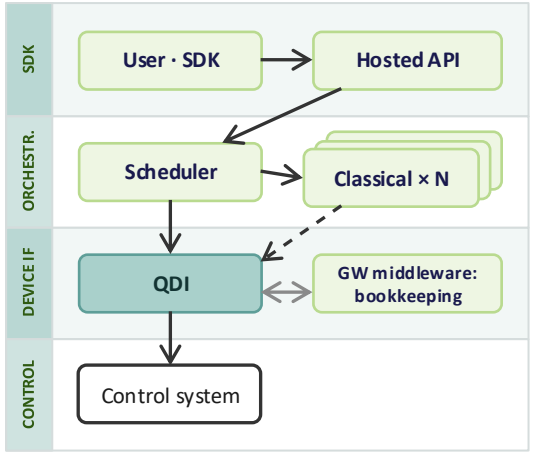


RESOURCES

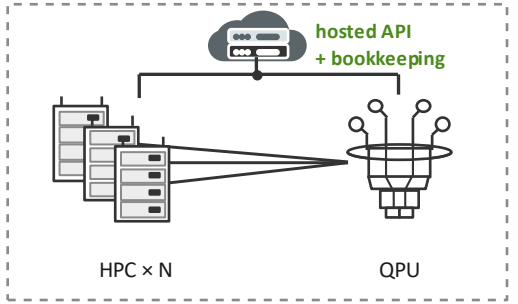


(c) Shared QPU

TIER M · MANY:1

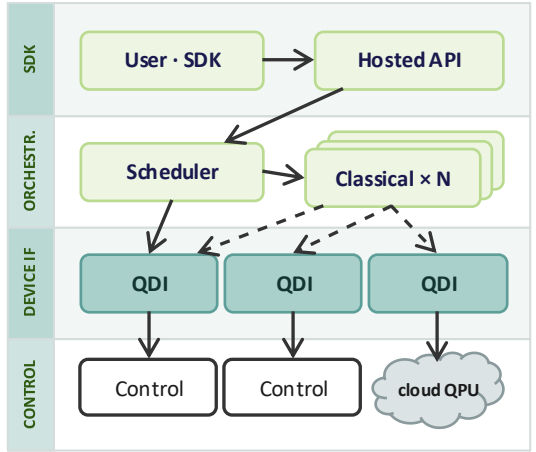


RESOURCES

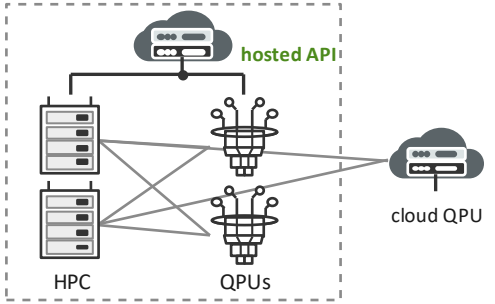


(d) Multi-QPU

TIER M/L · MANY:MANY



RESOURCES



Component paths follow the IQM deployment diagrams: (1) direct offload from the scheduler, (2) hybrid offload from a running classical process. Dashed boxes mark site boundaries.

Sona. Najafi et al, in preparation

Lithium-air batteries have 5.0x theoretical energy density of Li-ion batteries

Towards simulation of next generation batteries



Battery materials are strongly-correlated

Approximations cannot capture the behavior of strongly-correlated systems, such as battery materials

Need to understand the reaction pathways



Computational cost too high for practical use

QC-AFQMC is a hybrid method that is a quantization of a promising classical method. While efficient, it is still too slow for any practical chemical system



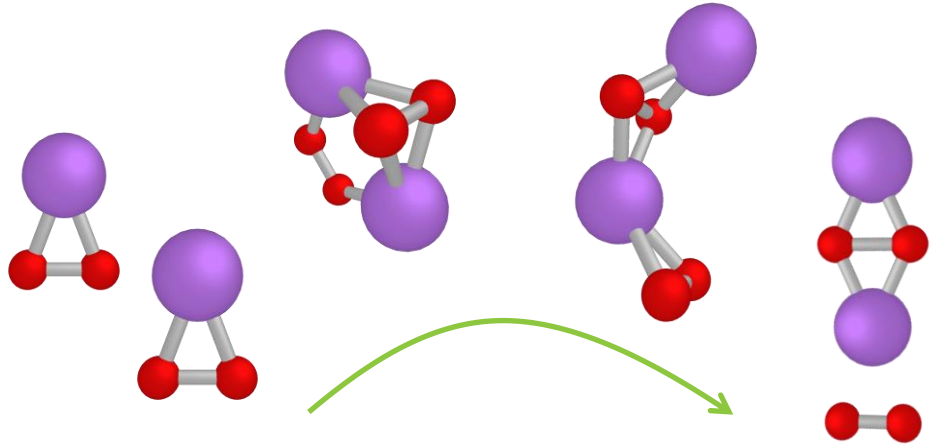
Improved SOTA runtime estimates by 248x using LUMI supercomputer

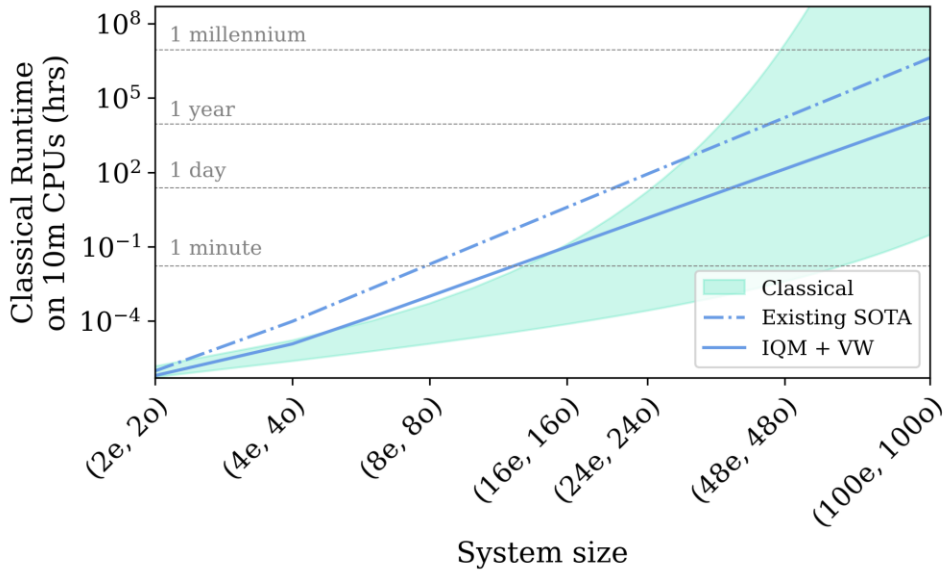
Combining algorithmic and implementation improvements, we bring the projected runtime for a 100-orbital system down to a couple years from half a millennium



Largest demonstration of this hybrid method

Contextualize the work with a reaction pathway for lithium-air batteries that fitted to 40 qubits



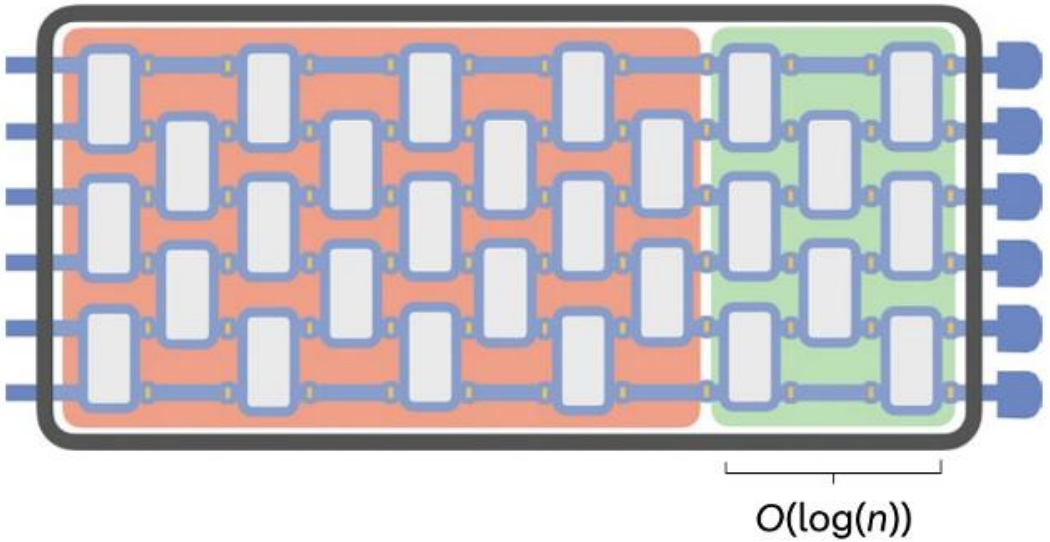


arXiv:2606.19239

Why we need error corrections?

Noise sets a hard ceiling on what a quantum computer can do without error correction.

- Noise makes deep circuits **effectively shallow**: only the last O(log n) layers still influence the output.
- Adding qubits and depth without QEC **stops adding computational power**.
- QEC encodes each **logical qubit** in many physical qubits and corrects errors faster than they accumulate.
- How efficient QEC is depends on the **hardware connectivity** and on fast classical decoding on HPC/AI.



Effective depth of noisy circuits. For most circuits with (possibly non-unital) noise, only the last O(log n) layers significantly influence expectation values; n is the number of qubits.

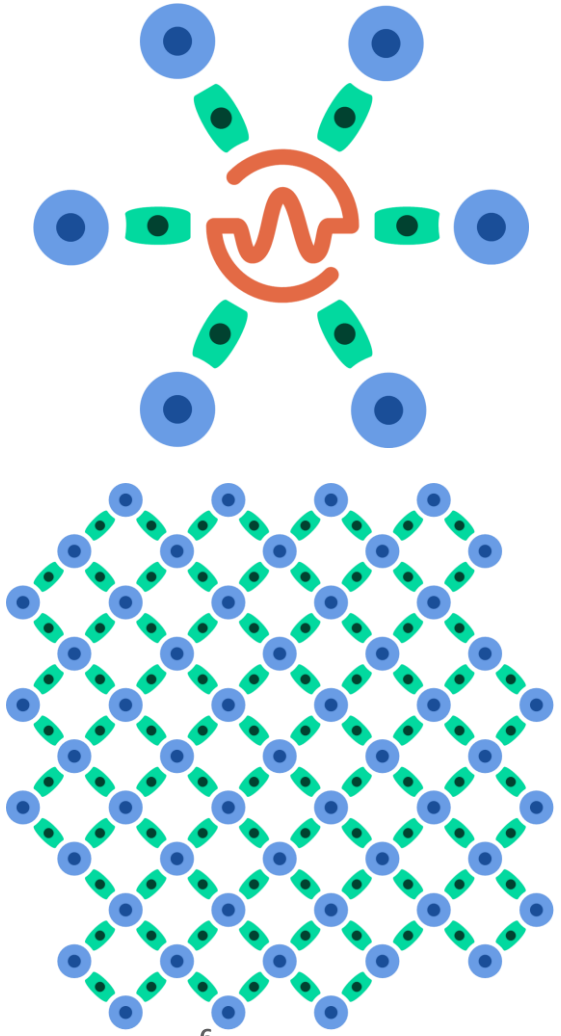
Mele, A.A., Angrisani, A., Ghosh, S. et al. Noise-induced shallow circuits and absence of barren plateaus. Nature Physics (2026). doi:10.1038/s41567-026-03245-z

Beyond surface code

Quantum error correction (QEC) is crucial in reaching fault-tolerant quantum computing, and its efficiency depends on hardware connectivity.

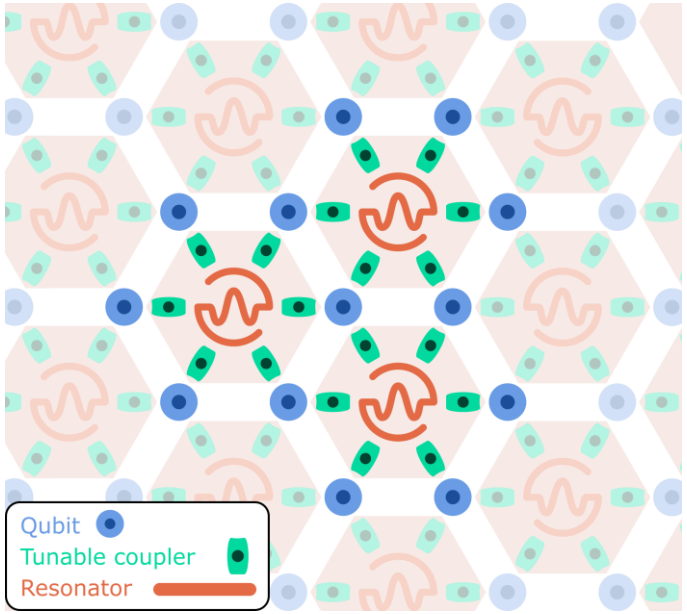
Previous approaches fall short:

- Most processors use square lattice connectivity, ideal for surface code QEC but inefficient for newer codes like color codes or qLDPC.
- Surface code needs a vast number of physical qubits to protect few logical qubits.
- **IQM Star** provides high connectivity but limited parallelism, slowing QEC cycles at scale.

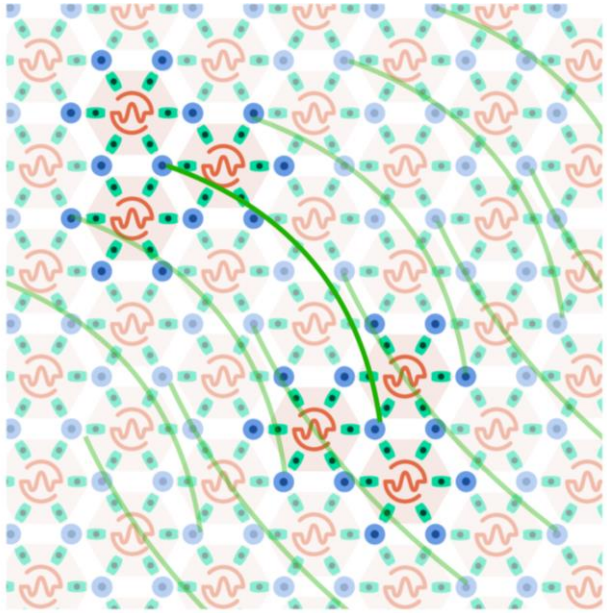


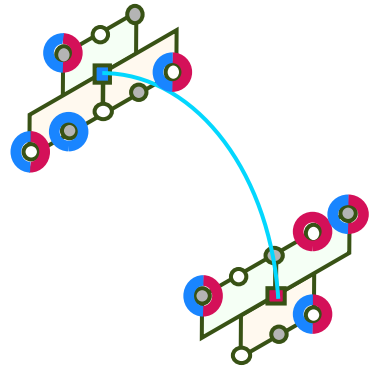
2 4 6

IQM Constellation & Barbell code



- Effective **12-to-1 connectivity** instead of 4-to-1
- High parallelism, high connectivity, high fidelity 2 qubit gate
- Ability to research **NEW QEC codes** such as quantum low density parity check (qLDPC) codes





A “barbell”

- Limited number of **near local couplers**
- Utilize IQM new quantum error correction code, the **Barbell Code**
- 8x lower cost in resources, high efficiency compared to rotated surface code
- 30 physical qubit to 1 logical qubit

Introducing IQM Halocene

The next gen product line for quantum error correction research

Learn, educate, research, and **create IP** on the critical path to **quantum error correction.**

Join cutting-edge researchers to reach fault-tolerant quantum computing

From **IP creation** to **commercialization**

Build **commercial applications** across key domains

- Compilers
- QEC code implementations
- HPC integration software
- Error decoders (AI)
- Calibration tools
- Quantum algorithms

