AI OPEN
DATA CENTER

Pushing the Single-Phase Cold Plate Limit:

Design Practice, Field Learnings, and the Runway Before Two-Phase Scales

Moderator:

Joel Chakkalakal *Director of Business Development, Shield by Guardian*

Panelists:

Remco van Erp *Co-Founder & CEO, Corintis*

Yin Hang *Technical Lead Thermal Engineer, Meta*

Oscar Farias Moguel *Principal Thermal Engineer, Microsoft*

Weihua Tang *Technical Lead Manager, Google Cloud*

OCP BRONZE Member

Panel Discussion

OCP INNOVATION VILLAGE



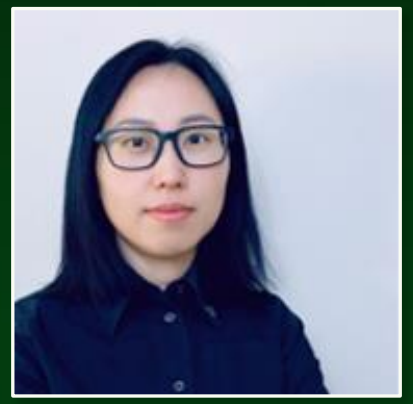
Joel Chakkalakal

Director of Business Development Guardian- Moderator



Remco van Erp

Co-Founder & CEO, Corintis-Panelist



Yin Hang

Technical Lead Thermal Engineer, Meta Platforms-Panelist



Oscar Farias Moguel

Principal Thermal Engineer, Microsoft-Panelist



WeiHua Tang

Technical Lead Manager, Google Cloud

Moderator



Joel Chakkalakal

Director of Business Development, Shield by Guardian — Moderator

As a Lean Six Sigma Master Black Belt, Joel builds end-to-end solutions that help data center operators take operational risk out of their critical infrastructure. At Shield by Guardian — the data center services division of Guardian — he works with hyperscale and enterprise clients on the testing, maintenance, and fluid management programs behind high-density liquid-cooled deployments.

Joel earned his Master's in Supply Chain Management from the University of Houston after completing his Bachelor's in Marketing at the University of Texas. His experience spans prestigious brands including AWS, Meta, Formula 1 Racing, and Coca-Cola, where he led cross-functional teams and spearheaded initiatives to overhaul complex operating systems — 180 process optimization projects that saved his clients over $1.8B.

Panelists



Remco van Erp

Co-Founder & CEO,
Corintis

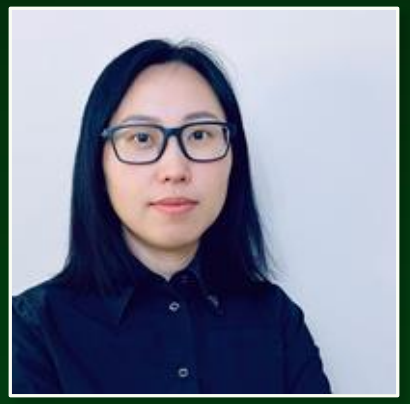
Remco van Erp is co-founder and CEO of Corintis, a provider of liquid cooling solutions for data center applications.

Remco received B.S. and M.S. degrees in mechanical engineering from the Eindhoven University of Technology, Eindhoven, The Netherlands, and holds a Ph.D. in microsystems and microelectronics from the École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland.

CORINTIS

OCP GLOBAL SUMMIT | 2026

Panelists



Yin Hang

Technical Lead Thermal Engineer, Meta Platforms

Yin Hang is a technical lead thermal engineer at Meta Platforms Infrastructure Foundation team, where she develops thermal solutions for IT hardware, specializing in advanced cooling solutions for Meta's in-house accelerators.

Yin earned her PhD from Purdue University.

Panelists



Oscar Farias Moguel

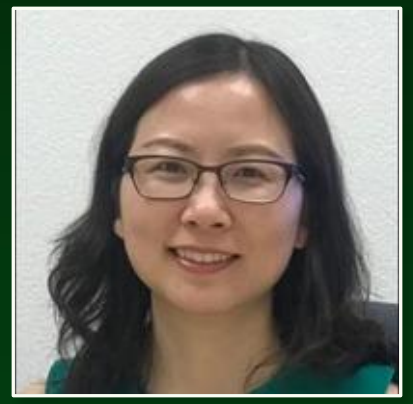
Principal Thermal Engineer, Microsoft

Oscar Farias Moguel is a Principal Thermal Engineer at Microsoft, where he focuses on technology pathfinding for next-generation cloud and AI infrastructure. As part of the Systems Planning and Architecture (SPARC) organization, he works on evaluating and maturing advanced cooling technologies for future datacenter applications, helping bridge the gap between emerging innovations and hyper-scale deployments.

Oscar holds a PhD in Mechanical Engineering from The University of Sheffield, UK.

Microsoft

Panelists



Weihua Tang

Technical Lead Manager, Google Cloud

Weihua Tang is a Technical Lead Manager at Google Cloud, where she develops thermal solutions for IT hardware, specializing in optimizing cooling technologies for data centers.

Prior to Google, she dedicated 14 years to Intel, focusing on processor testing, packaging development, and thermal-mechanical architecture for platform systems. Weihua holds 12 US patents.

Weihua earned her PhD in Mechanical Engineering from the University of Minnesota and holds master's and bachelor's degrees in Heating, Air Conditioning and Gas Engineering from Tongji University in Shanghai, China.

Microsoft

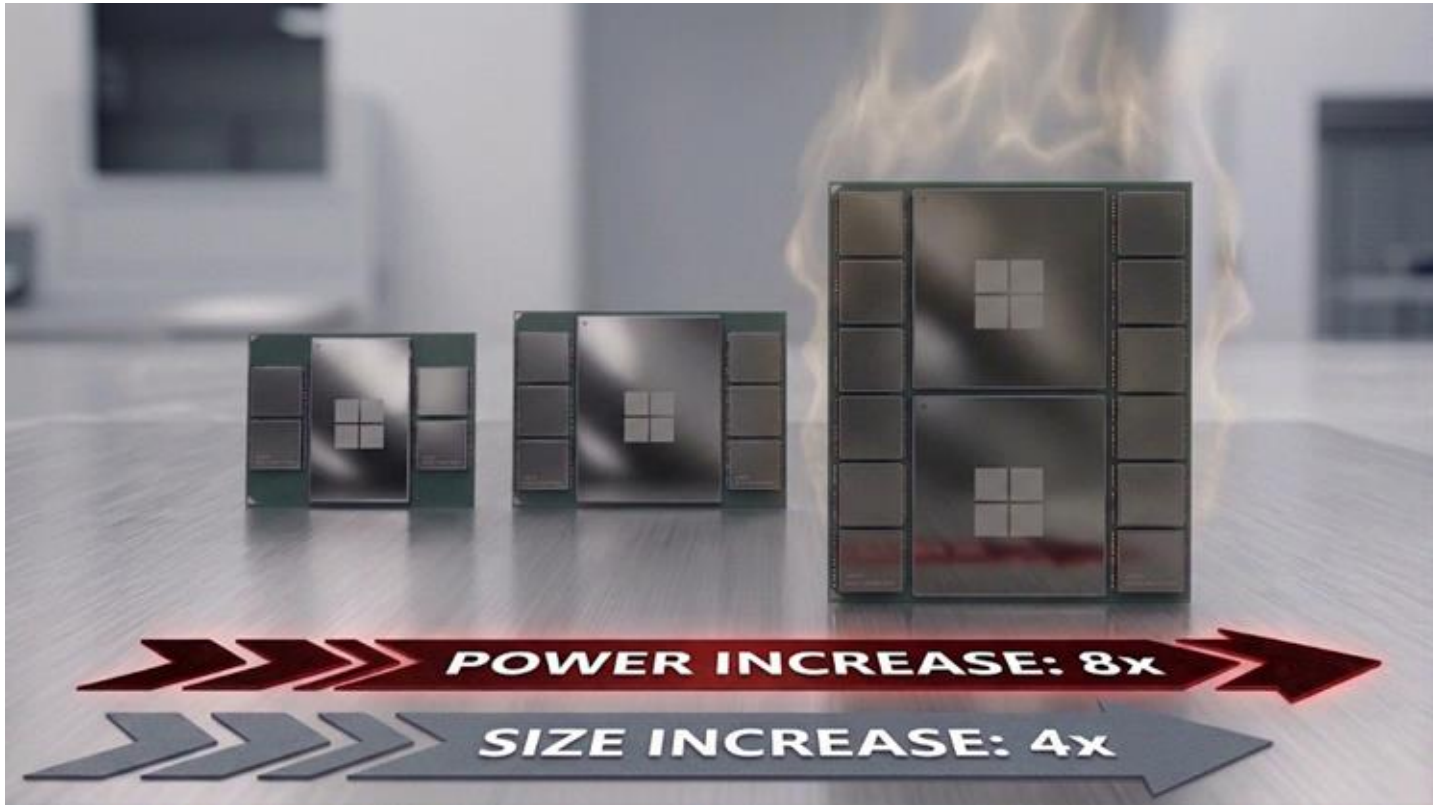
COOLING:
COLD PLATE



Pushing the Single-Phase Cold Plate Limit: A unitary approach

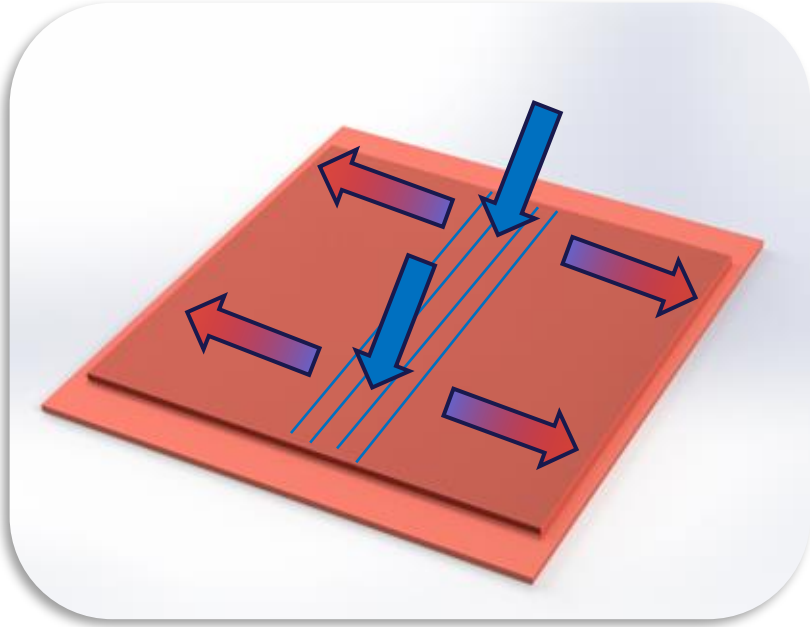
Oscar Farias Moguel
Principal Thermal Engineer
Systems Planning and Architecture (SPARC)

Single-Phase Cold Plate: Current Challenge



3D renders created with Microsoft Copilot. Not representative of any product or roadmap.

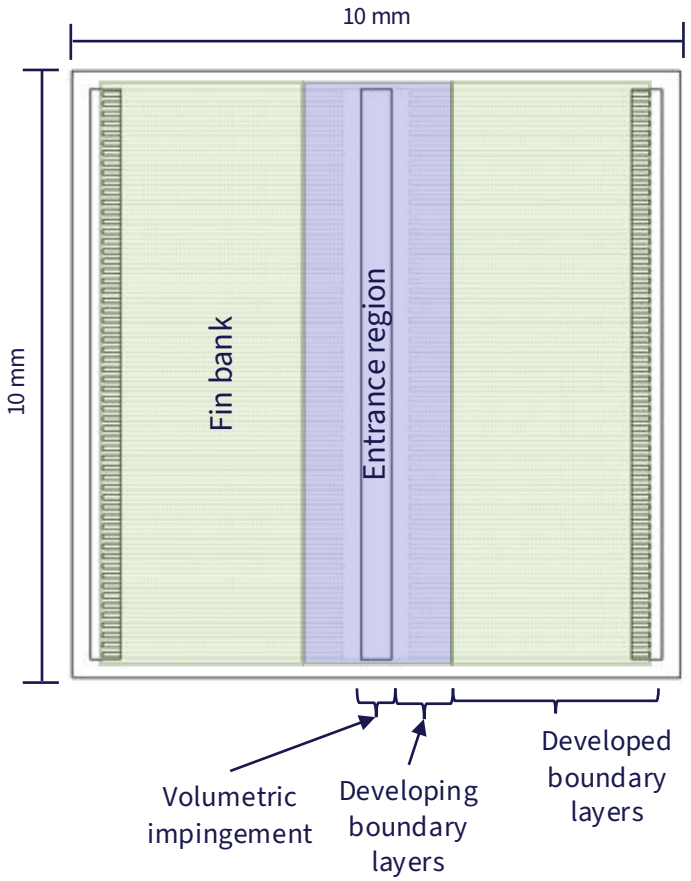
Processor architectures complexity is increasing



Traditional cold plates rely on a monolithic fin bank, resulting in significant fluid temperature rise and pressure drop.

Microsoft Azure

Single-Phase Cold Plate: Optimization Opportunities



Anatomy of a cold plate unitary cell

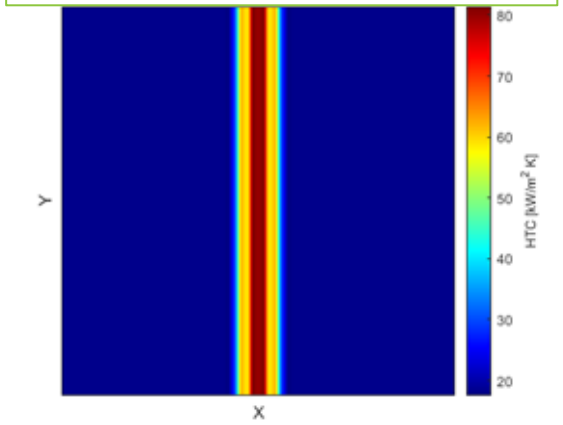
Optimization avenues for a cold plate unitary cell:

Entrance region:

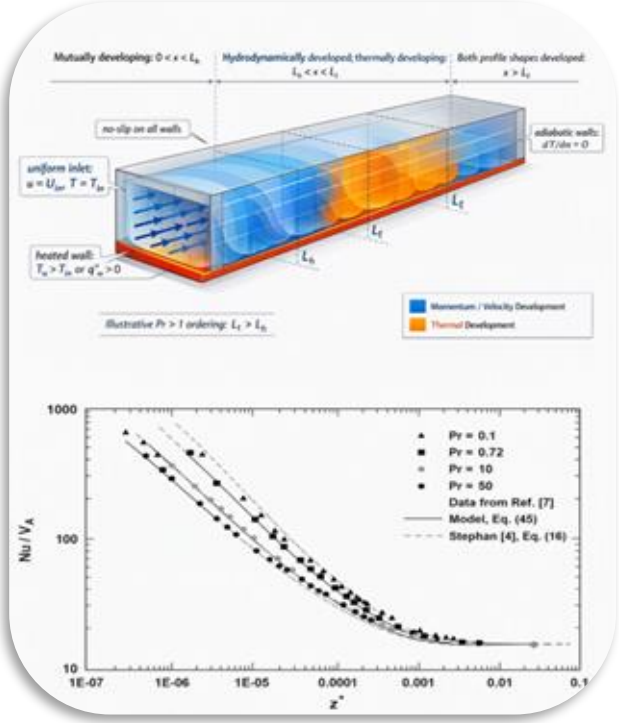
- No caloric gain
- Impingement effect
- Boundary layer development

Fin bank:

- Smaller feature size
- Boundary layer disruption



HTC map of an optimized unitary cell

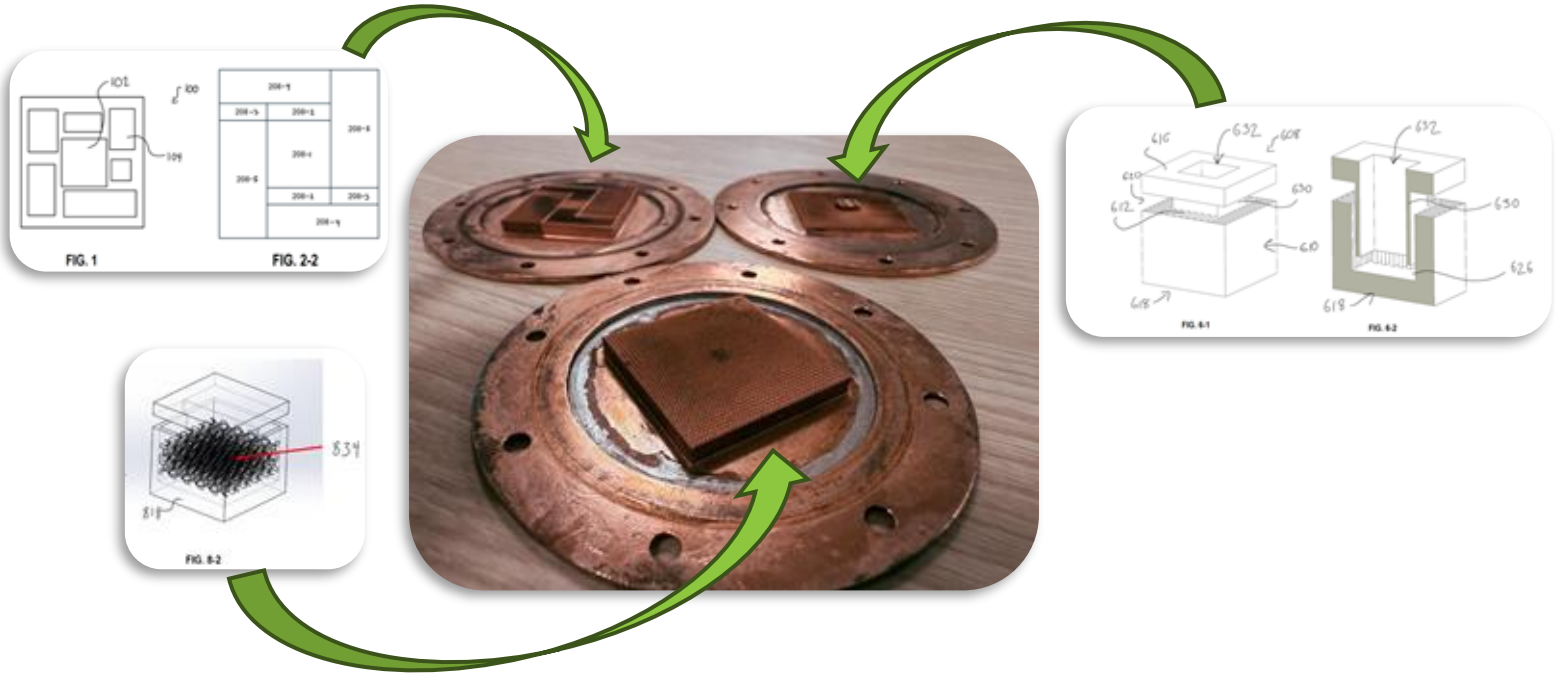


Plot 1. Nusselt number along the axis direction in a rectangular duct (one heated plus 3 adiabatic walls)

Upon the entrance region in a fin bank, there is a ~1 mm in length that will have a 150x higher Nu ≈ 6x more HTC. Is this enough to mitigate large hot spots? We think so!

Microsoft Azure

Single-Phase Cold Plate: Optimization Tests



Small form factor evaluation



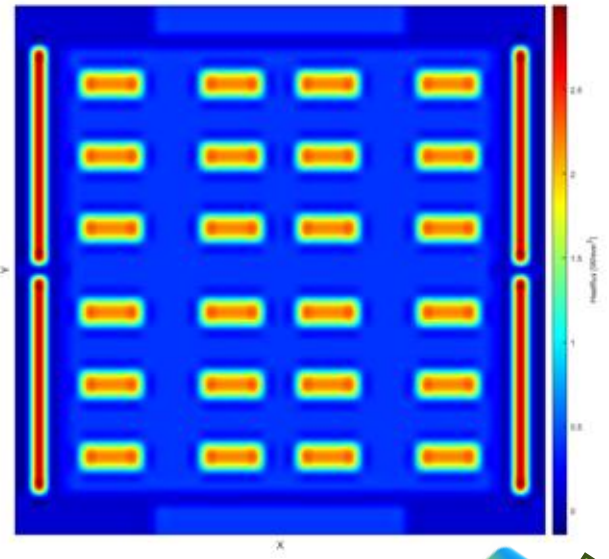
Representative form factor evaluation with a partner company (future processor architecture)

Up to 10C junction temperature reduction was measured

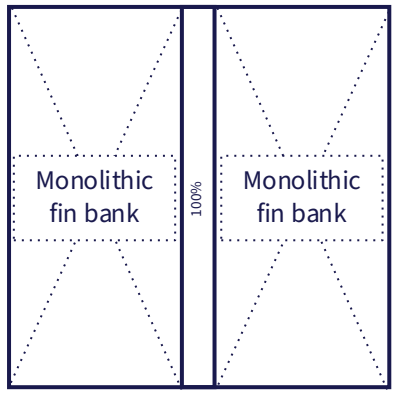
Cold plate prototypes based on a unitary cell approach, as testing lead by Microsoft SPARC

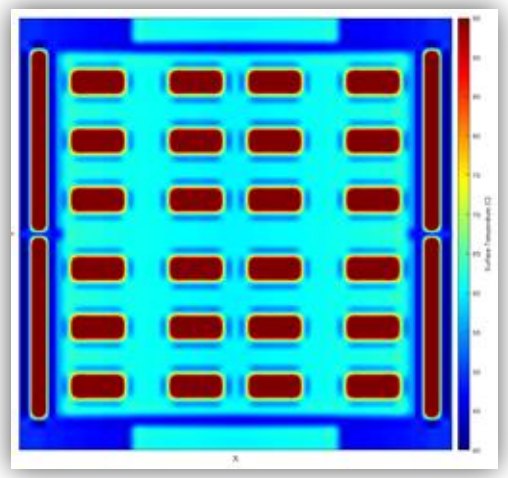
Microsoft Azure

Single-Phase Cold Plate: Unitary Cell Methodology



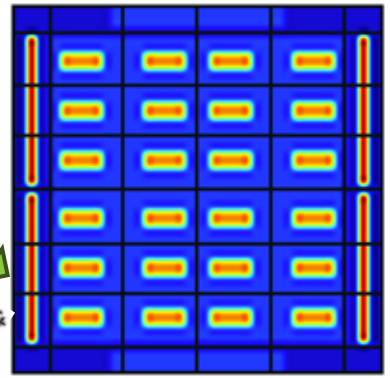
Hypothetical processor heat flux distribution





Traditional cold plate cannot provide enough cooling. All hotspots **overheat**.

Microsoft Copilot

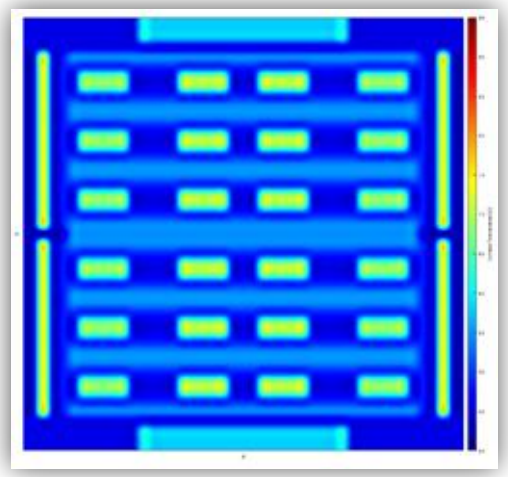


Unitary cell distribution optimization

DOE

10%	20%	60%	60%	20%	10%
140%	130%	120%	120%	130%	140%
140%	130%	120%	120%	130%	140%
140%	130%	120%	120%	130%	140%
140%	130%	120%	120%	130%	140%
140%	130%	120%	120%	130%	140%
140%	130%	120%	120%	130%	140%
10%	20%	60%	60%	20%	10%

Fluid allocation adjustment



A cold plate using a unitary cell design philosophy can cool the hotspots below the desired target.

Microsoft Azure

CORINTIS

Cooling

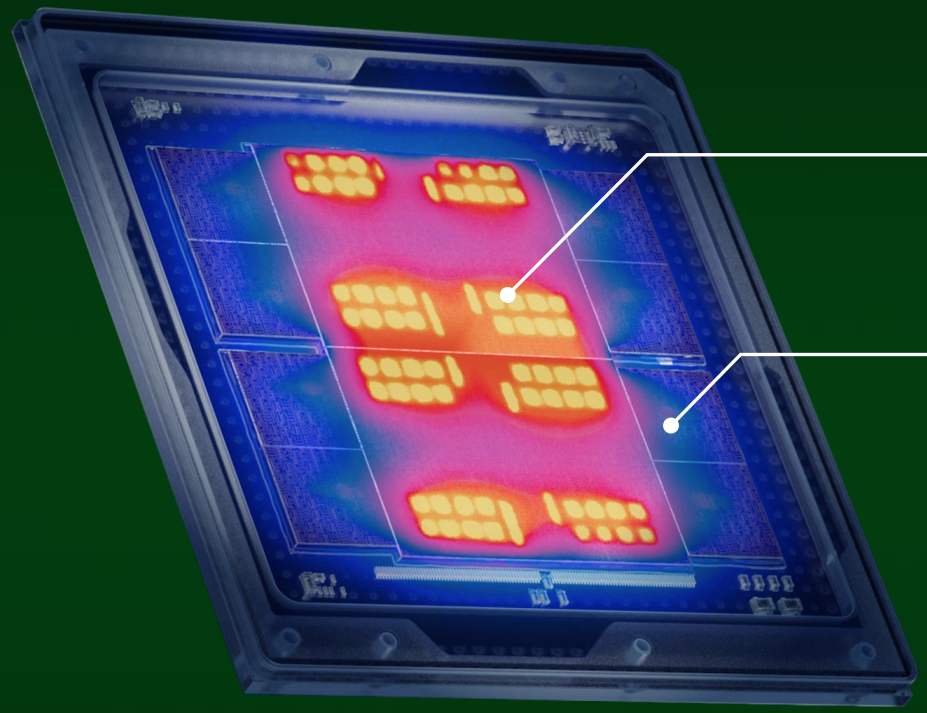


Microfluidic cores: chip-specific liquid cooling to advance cold plate performance

Remco van Erp

Co-founder & CEO - Corintis

Chips are heterogeneous - cooling isn’t



Non-uniform power

Hotspots concentrate in a fraction of the die area

Non-uniform conduction

3D chip stacks move heat at very different rates

Non-uniform limits

ASIC and memory tolerate different peak temperatures

Chips are not a uniform heat source – Cooling needs to match what happens in the package

Microfluidic core

CHIP-SPECIFIC THERMAL COMPONENTS TO INCREASE SINGLE-PHASE COLD PLATE PERFORMANCE

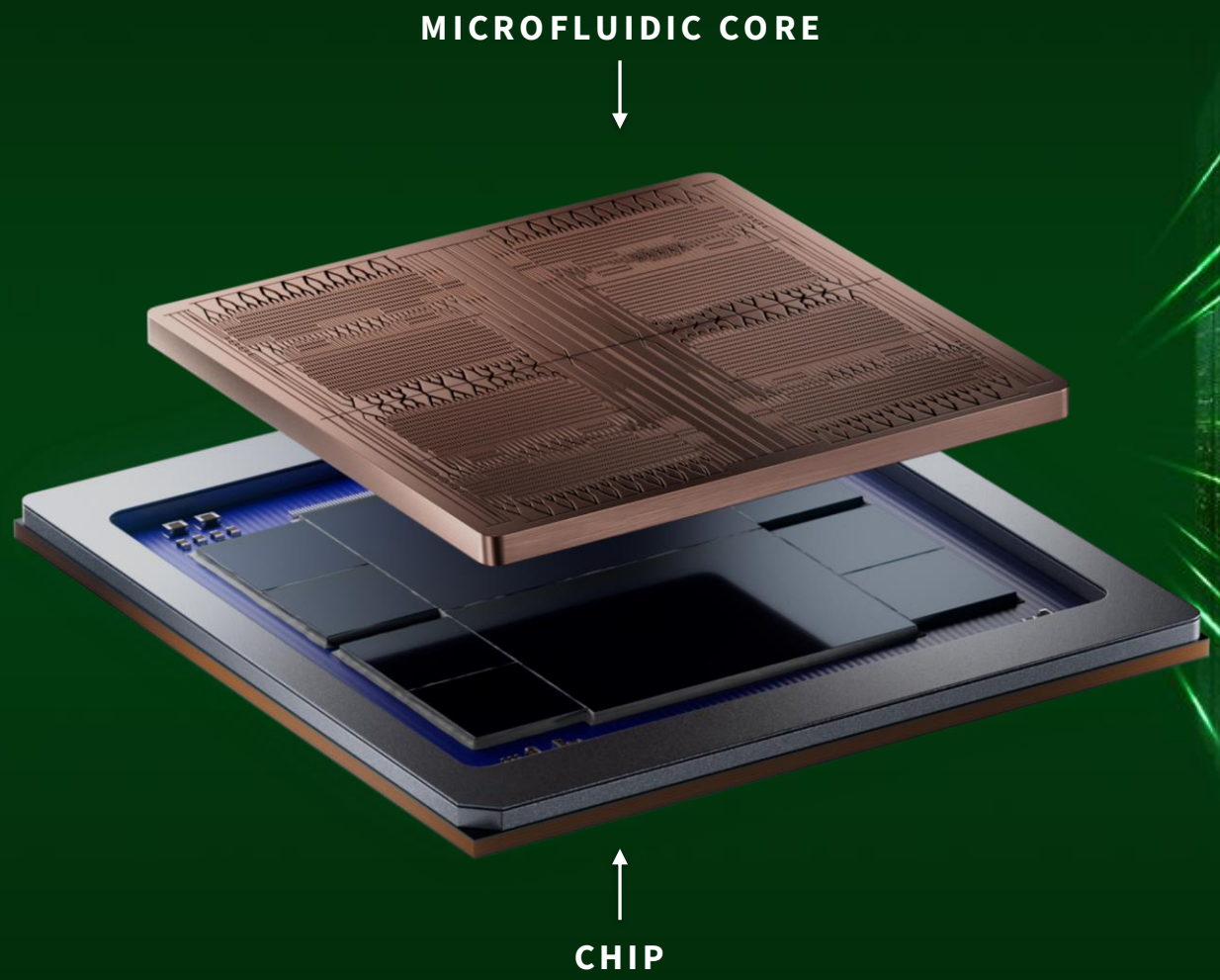
01 **Single-phase** drop-in solution

02 **Co-designed** with the chip

03 **10–20%** lower temperature

04 **Compatible** with existing supply chain

05 **Mass-production** technology

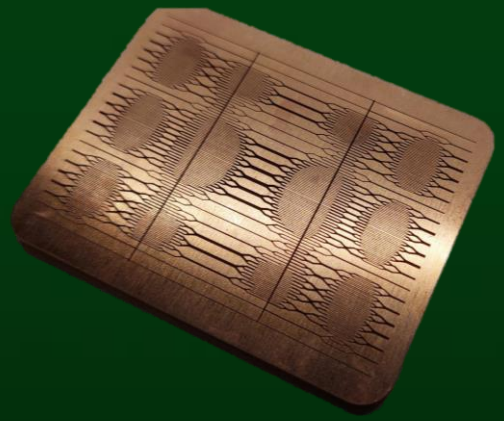


Experimental results on NVIDIA H200 GPU

SKIVED COLD PLATE

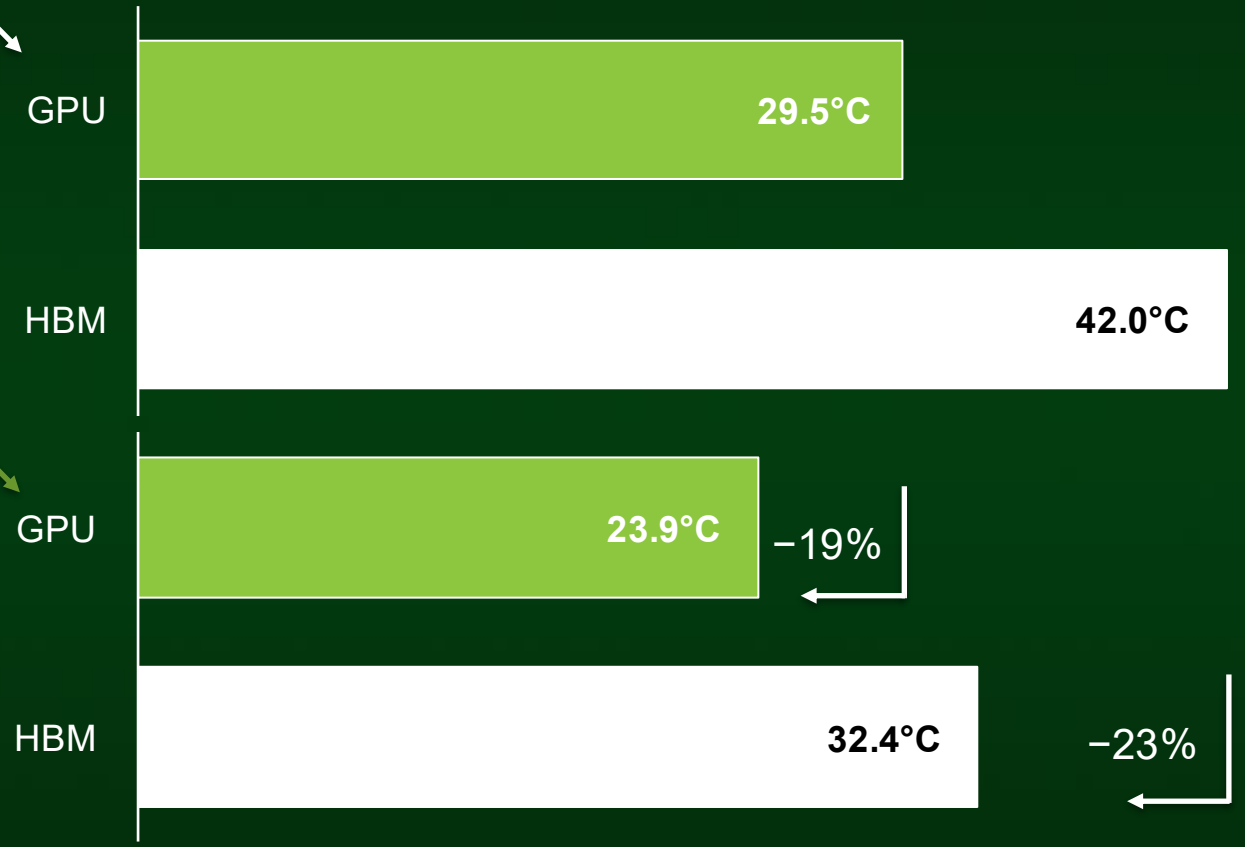


MICROFLUIDIC COLD PLATE



Junction-to-inlet temperature rise

°C · NVIDIA H200 at 1 LPM · lower is better



Same coolant, same 1 LPM flow, same test rig.

Focus area 1: Design & simulation tools

1 DESIGN/SIMULATION

CHALLENGE

Product cycles are extremely short, but it can take 12+ hours to simulate cold plates, making manual cooling optimization impractical.

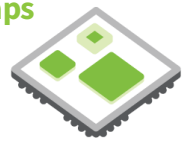
ACTION

Fast & **accurate** simulation tools based on interoperable standards and cooling design optimization algorithms to increase performance within short cycle times.

What we do:
Glacierware

Chip Inputs

Package model (ECXML)
Temperature targets
Power maps



Facility inputs

Pressure drop/flow rate
Filtration





Focus area 2: Advanced manufacturing

2 MANUFACTURING

CHALLENGE

Cold plates today rely on skiving, which is mature, but limits design freedom to straight fins.

ACTION

Alternative **scalable** manufacturing methods, such as additive manufacturing, to unlock complex geometries that improve cold plate performance

What we do:
Core Foundry



Channel and fin width:	Large design freedom in	Volume:
<100 µm	3D	Millions/year

Focus area 3: High resolution test vehicles

3 TEST & VALIDATION

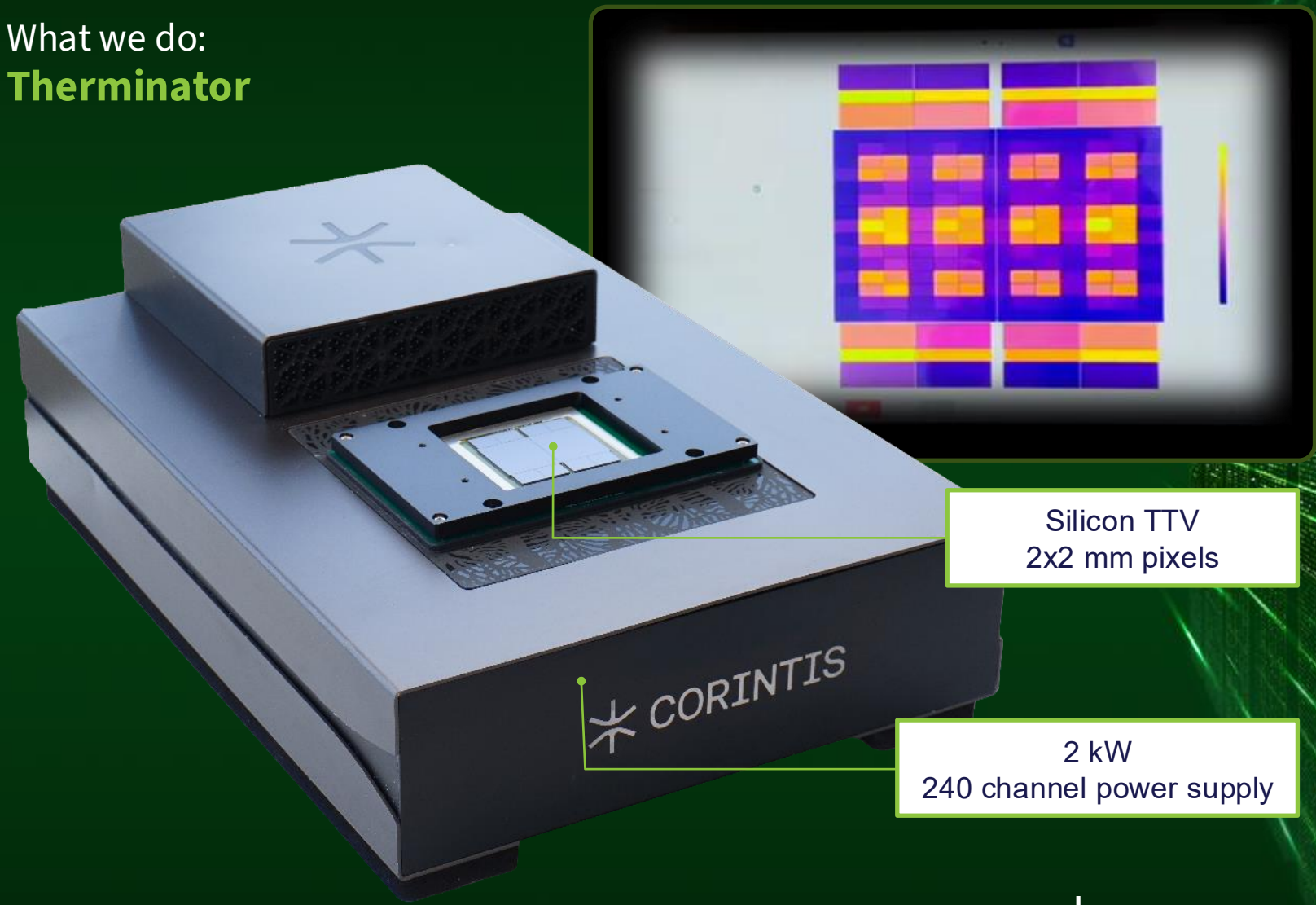
CHALLENGE

Chip designers don’t have access to real silicon until late-stage product development, so testing occurs on uniform copper cartridge heaters.

ACTION

High-resolution silicon thermal test vehicles that enable **rapid & representative early-stage performance validation.**

What we do:
Therminator



COOLING:
COLD PLATE

Pushing the Single-Phase Cold Plate Limit

Design Practice, Field Learnings, and the Runway

Weihua Tang

Thermal Systems Technical Lead Manager, Google

OCP PLATINUM Member

PANEL DISCUSSION | Cooling Environments — Cold Plate Track • OCP Global Summit 2026

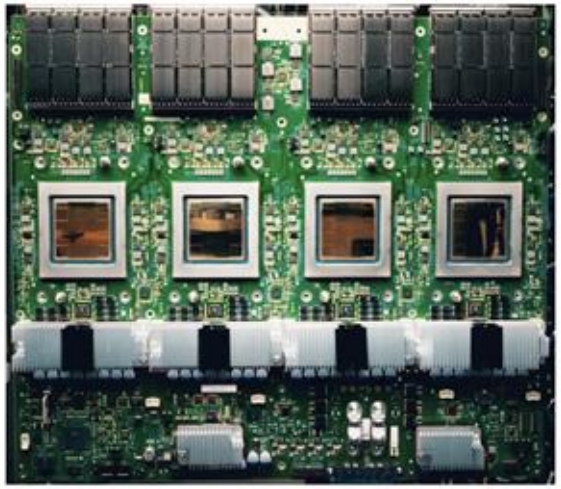
Scaling Single-Phase Cold Plates: Design & Thermal Actions

CHALLENGE: SYSTEM INTEGRATION & HYDRAULIC LIMITS

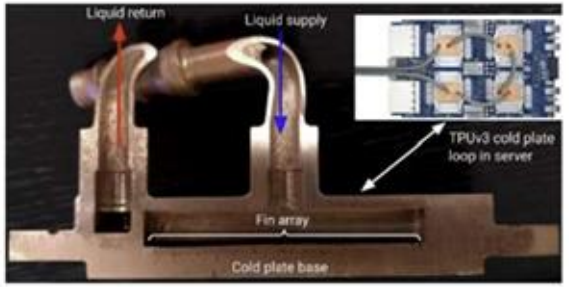
- Higher power, dense keep-out zones, and strict height limits drive high rack coolant flow and pressure drop toward connector limits.
- Higher coolant flow yields diminishing cooling gains while causing a steep surge in pumping power.

ACTION: SILICON & COLD PLATE CO-DESIGN

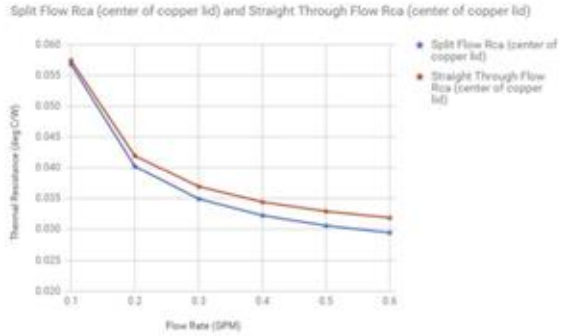
- Co-architect the silicon floorplan, chip package, and cold plate hydraulics together.
- Split incoming coolant into short parallel micro-fin sections and tailor local fin geometry, channel depth, and targeted coolant flow to the chip heat map.



Ironwood 4-Chip Liquid-Cooled Tray
Source: Google Cloud, Hot Chips 2025



Split-Flow Microchannel Cold Plate Cross-Section
Source: Google, Hot Chips 2025 Liquid Cooling Tutorial



Split-Flow vs. Straight-Through Rca vs. Flow (GPM)
Source: Google, Hot Chips 2025 Liquid Cooling Tutorial

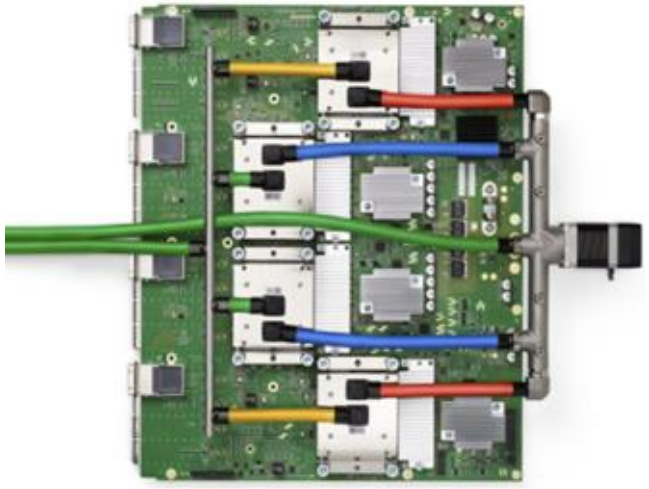
Scaling Single-Phase Cold Plates: Design & Thermal Actions

CHALLENGE: THERMAL INTERFACE, WARPAGE & HOTSPOT SPREADING

- Refining micro-fins alone yields minimal chip temperature reduction without lower interface resistance.
- Extreme localized hotspot heat flux overwhelms the lateral heat-spreading capacity of solid copper.

ACTION: THERMAL INTERFACE STACK & COMPOSITE BASES

- Prioritize resistance reduction across Thermal Interface Materials — where a large share of the thermal budget is lost.
- Integrate high-conductivity composite baseplates with higher thermal conductivity than pure copper.

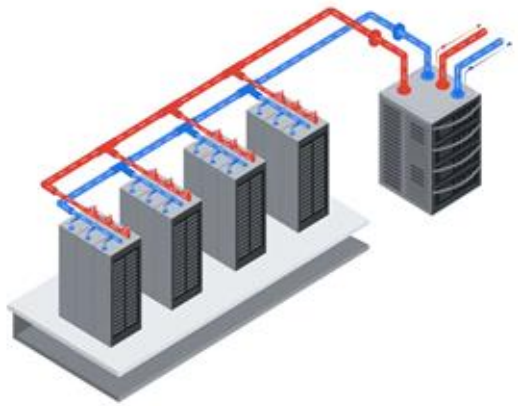


Spring-Loaded Direct-to-Die Parallel Cold Plate Loop
Source: Google, Hot Chips 2025 Liquid Cooling Tutorial

Scaling Single-Phase Cold Plates: Operations & Material Actions

CHALLENGE: DEPLOYMENT & OPERATIONAL CHALLENGES

- Microchannel debris lodges inside ultra-fine microchannels.
- Leak-sensor reliability issues and heterogeneous rack deployment.
- Secondary-side cooling system fluid chemistry management.



Multi-Rack CDU & Parallel Rack Manifold Loop
Source: Google Cloud, Hot Chips 2025 Tutorial



Quick-Disconnect Couplings & Flexible Hoses
Source: Google, Hot Chips 2025 Liquid Cooling Tutorial

ACTION: GALVANIC CHEMISTRY, FILTRATION & LOOP GOVERNANCE

- Standardize durable coatings to raise safe erosion-corrosion velocity limits.
- Multi-tenant rack hydraulic impedance matching and field-hardened leak sensor qualification.
- Enforce water quality and corrosion inhibitors paired with fine rack filtration.

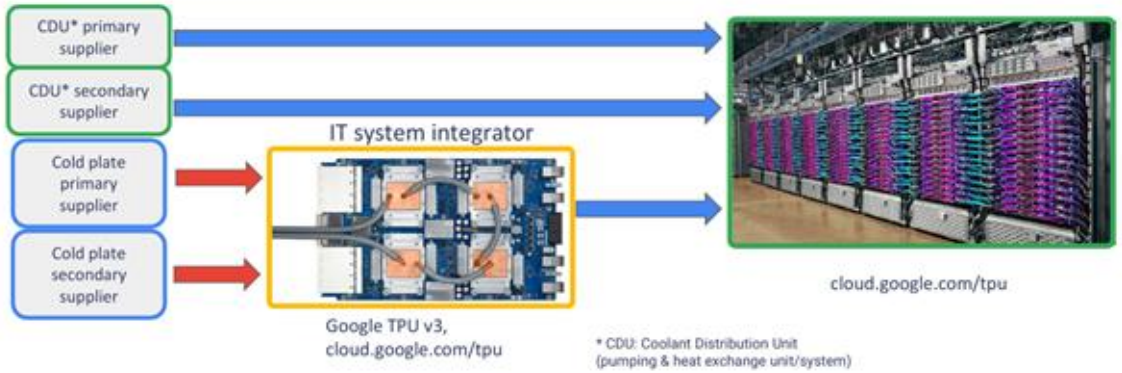


Custom 'Feeder Kit' Filtration & Purging Cart
Source: Google, Hot Chips 2025 Liquid Cooling Tutorial

Scaling Single-Phase Cold Plates: Operations & Material Actions

CHALLENGE: SUPPLY CHAIN & MANUFACTURING TRADE-OFFS

- Pure Copper Supply & Cost Volatility.
- Ultra-Fine Fin Skiving & Yield Risk.
- Multi-Vendor & Material Qualification.



Multi-Supplier Cold Plate & CDU Supply Chain
Source: Google, Hot Chips 2025 Liquid Cooling Tutorial

ACTION: ALTERNATIVE MATERIAL SYSTEMS (BEYOND PURE COPPER)

- High-temperature engineered polymers that eliminate galvanic corrosion and cut copper mass.
- Standardized testing for long-term creep, glycol aging, and seal integrity on alternative materials.

pH	6 < pH < 8
Type	Type II Deionized water alternate: water-glycol to support -40C shipping
Max particle size	<100 microns
corrosion inhibitor, biocides, & ratio	800 Water: 6 Inhibitor: 1 biocide
Corrosion inhibitor	Required
Biocides	non oxidizing
Wetted Materials List	ASHRAE chapter 6
Flammability	Minimum of V-0 (non-metallic material); VW-1 (wiring, sleeving/tubing); and HF-2 (foam)
Metal/alloys * indicates alloy details to be added	304SS, 316SS
	Forged brass with nickel plated valves
	Type L copper - brazed only, no solder
Polymer/Elastomer * indicates polymer details to be added	EPDM
Operating temperature range	up to 70C continuous
Pressure range (connect, disconnect and operating	150 PSig
Reliability	15 years
Power and Electrical	3 phase, 5 wire system with voltage range of 180 VAC to

Google's contribution to a an open specification for a liquid cooled rack
Source: Google, Hot Chips 2025 (datacenters.lbl.gov)

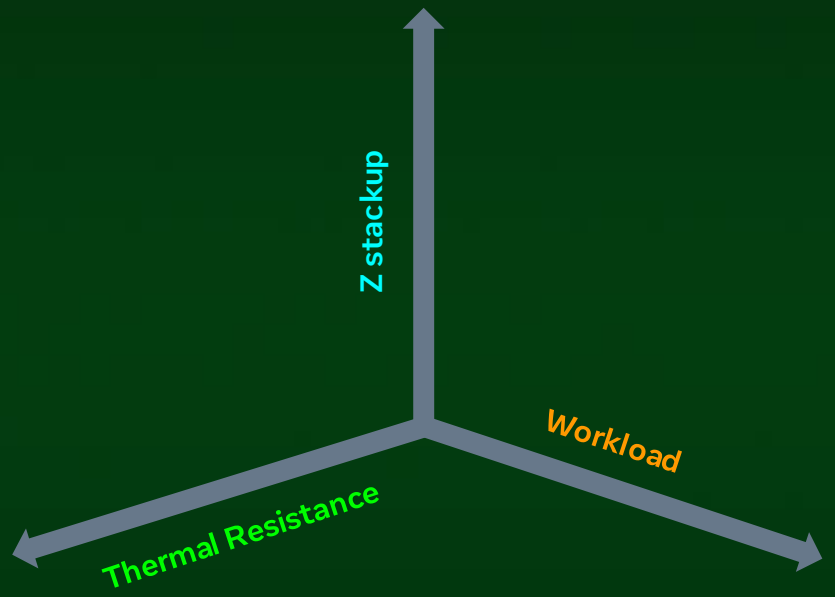
COOLING:
COLD PLATE

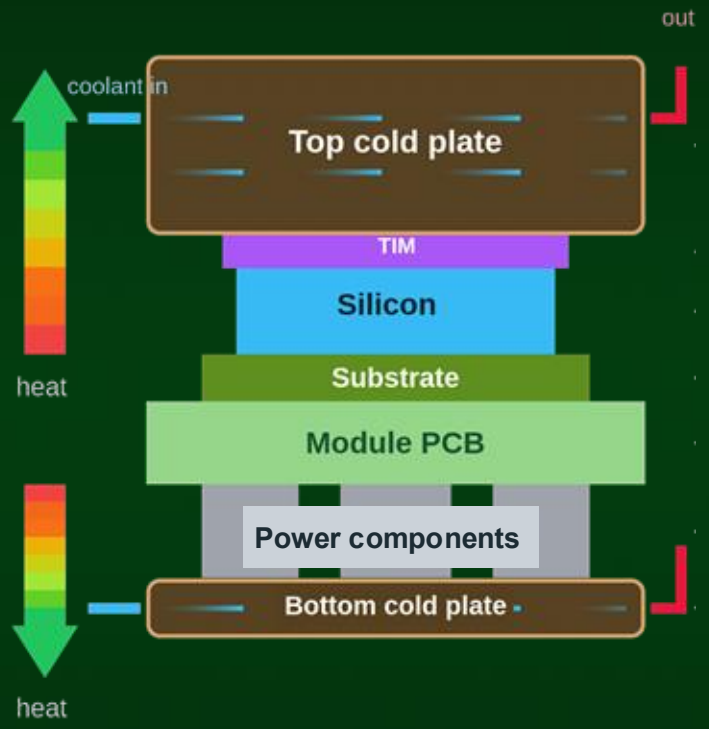


Pushing the Single-Phase Cold Plate Limit

Yin Hang
Thermal Engineer, Meta

Cooling is **NOT** an one-dimensional problem



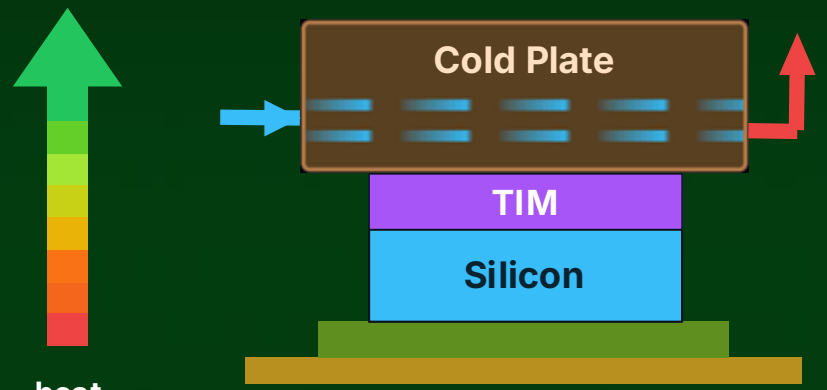


TIM = thermal interface material

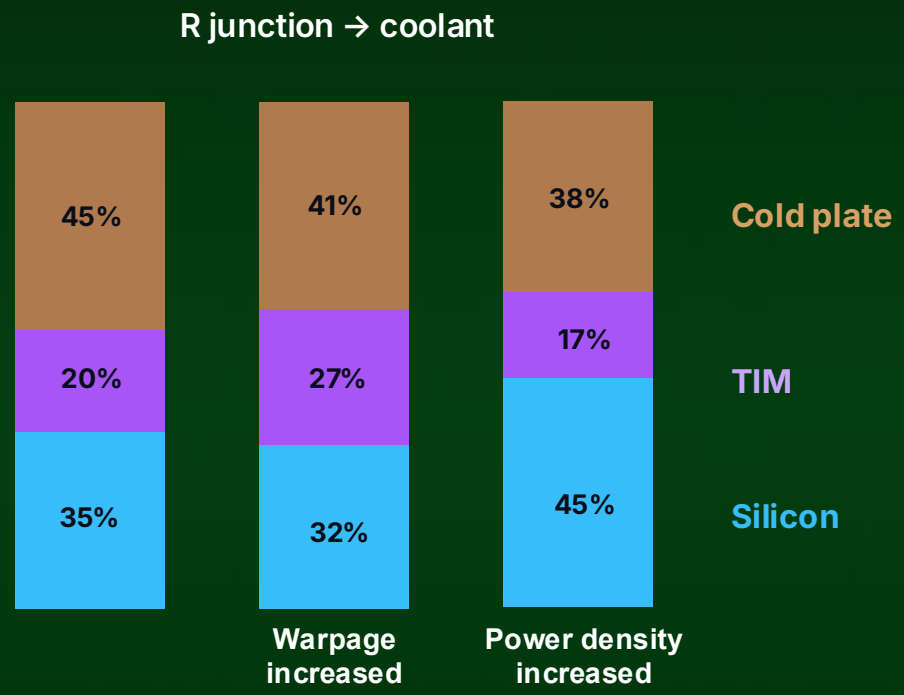
Top cold plate	18.85
Package	6.13
Module PCB	4.47
Power components	7.70
Bottom cold plate	4.50

Confidential

Cold Plate is **NOT** the only bottleneck



TIM = thermal interface material

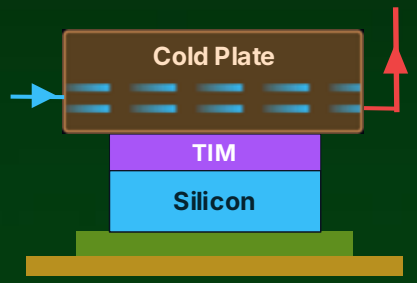


Thermal resistance reduction translates to many many watts directly

Confidential

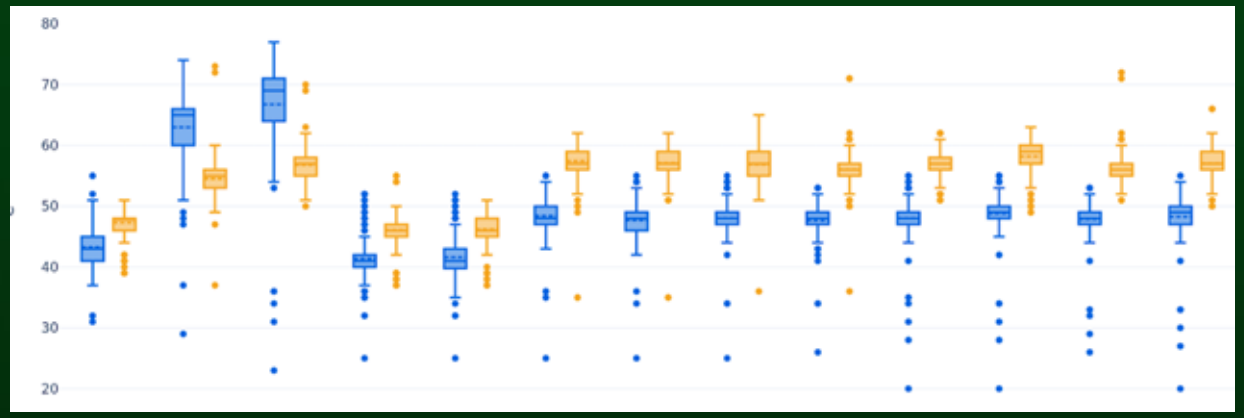
Cooling is **NOT** just a cold plate

X kW | XX kW | XXX kW | XX MW | X to XX GW

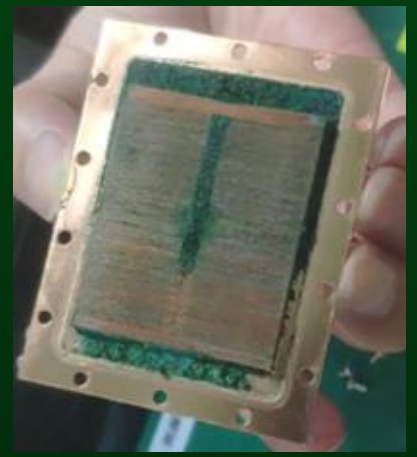


TIM = thermal interface material

tray → Rack → Data Hall → Cluster







Call to Action

- **Expand the option set** for pushing single-phase cooling limits
- **Align on simulation and validation guidelines** to benchmark thermal performance
- **Align on test matrix and quality control** across cold plate manufacturing methods
- **Drive the mass production and engagement model** to accelerate advanced cold plate adoption
- **Keep innovation on the full stack** to push the single phase cooling limit

Join us — scan the QR code to get involved.