

Electronic Components Sector

FC-BGA (ABF) substrate technology seminar report

We invited Mr. Toshihiko Nishio of SBR Technology to conduct a seminar on future technological trends for flip chip ball grid array (FC-BGA) substrate (Ajinomoto build-up film [ABF] substrate) on July 14. Main topics of discussion included technological trends for cores (organic cores, glass cores, high-density interconnect [HDI] cores, and ceramic cores), embedded multi-die interconnect bridge with through-silicon vias (EMIB-T) from the standpoint of substrate, and trends for chip-on-wafer-on-substrate (CoWoS), chip-on-panel-on-substrate (CoPoS), and chip-on-wafer-on-platform (CoWoP). We provide an overview of the seminar below and summarize implications for the electronic components sector.

Our view

- For CoWoS and CoPoS, connection (soldering) reliability during mounting has become an issue due to larger reticle sizes, and it appears that this could necessitate the use of high-rigidity substrates and glass core substrates. Meanwhile, although EMIB-T achieves higher connection reliability than CoWoS and CoPoS as a result of not using an interposer, Mr. Nishio cited a need to establish both mass production capabilities for the substrate and assembly processes. Considering this point, we think that CoWoS and CoPoS will require substrate technologies that deliver high rigidity and flatness, and that larger reticle sizes could increase Ibiden's relative competitive advantages. We also think that Ibiden and other Japanese companies could become key suppliers for EMIB-T. We think larger reticle sizes could increase Ibiden's competitive advantages over the medium term.

Seminar overview

- CoWoS-S/CoWoS-L:** (1) Chip-on-wafer-on-substrate with silicon interposer (CoWoS-S) is a structure in which a local silicon interconnect (LSI) and high-bandwidth memory (HBM) are mounted on a large silicon interposer, with ABF substrate below the interposer. However, as interposers increase in size, warping also increases and mounting (soldering) reliability decreases. Mr. Nishio said a reticle size of 3.3x is the upper limit for this reason. (2) Chip-on-wafer-on-substrate-large (CoWoS-L) does not use a silicon interposer, and instead has a structure in which redistribution layer (RDL) wiring is formed on a mold and silicon bridges are positioned at the connection points between LSIs and HBM. TSMC has disclosed plans to expand reticle size from 3.3x to 5.5x and then to 9.5x by 2029. However, ensuring flatness during assembly is difficult and connection problems are more severe because large blocks are formed using materials with different coefficients of thermal expansion (CTE; e.g., mold resin, copper RDL wiring, silicon bridges, chips, and ABF substrate). Rubin Ultra, based on a 5.5x reticle size, has faced difficulty in implementation evaluations, and Mr. Nishio thinks a 9.5x size will be very hard to achieve. Soldering has been identified as an issue for 9.5x reticle size as of 1H 2027, and although evaluations are currently underway for Rubin Ultra with 5.5x reticle size, Mr. Nishio said this is not going well. He said that if CoWoS-L with 9.5x reticle size does not succeed, limitations on packaging technology could make it difficult to achieve the Nvidia Feynman generation

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in 2029. Substrate sizes also increase to 85mm × 85mm for 3.3x reticle size, 110mm × 110mm for 5.5x reticle size, and 130mm × 140mm for 9.5x reticle size.

- EMIB/EMIB-T:** (1) EMIB is a packaging technology from Intel that embeds silicon bridges in the package substrate and connects LSI and HBM with localized fine-pitch wiring. Large silicon interposers are not required. The bump pitch for HBM4 could shrink from 65μm to 36μm in the future, and because this is finer than the typical LSI connection pitch, it requires high-density wiring between the HBM and LSI. (2) EMIB-T is a structure in which through-silicon vias (TSV) are formed in a silicon bridge to enable signal and power delivery to HBM and LSI from the substrate side. The ability to optimize power supply on the bridge enables the suppression of power noise in HBM operating at high frequencies and low voltages. In addition, because HBM and LSI with different sizes and connection conditions can be mounted individually on the substrate without using a large interposer, it eliminates the need to bond an entire large module at once, as is done with CoWoS-L, making the overall interposer less susceptible to warping and offering advantages for back-end process yields. Mr. Nishio said Intel claims EMIB-T can support up to 12x reticle size and can serve as an alternative for CoWoS-L. (3) While Intel has a mass production track record with conventional EMIB, Mr. Nishio explained that EMIB-T has not yet been established as a mass production technology, given a lack of reliable mass production capacity for external customers at Intel Foundry Services (IFS) and inadequate capabilities on the substrate side as well. Broadcom and Google have expressed interest, but whether Intel can launch EMIB-T as a mass production technology is a key focus point. (4) EMIB-T faces challenges not only for developing substrate but for assembly processes as well, but Mr. Nishio said IFS plans to license assembly technology to Amkor Technology and outsource assembly to Amkor.
- CoPoS/CoWoP:** (1) CoPoS is a production method in which the CoWoS processes that are normally done on a 300mm wafer are instead implemented on a 310mm square panel. This method improves productivity by using glass carriers and fully utilizing the area of a square panel. Mr. Nishio said the launch of this technology could proceed as TSMC plans, or could be delayed by up to around two years. However, Mr. Nishio believes this technology is relatively easy for TSMC to control, because any delays can be offset by increasing existing CoWoS capacity. (2) CoWoP is a packaging technology that Nvidia aims to adopt in the future. CoWoP eliminates conventional ABF substrate and directly mounts interposers equipped with graphics processing units (GPUs) and HBM on substrate-like printed circuit boards (SLP). Reducing the number of intermediate substrates is expected to simplify the structure, shorten signal paths, increase design flexibility for heat dissipation, and reduce costs. Mr. Nishio said Nvidia intends to reduce its reliance on Japanese substrate makers and use the PCB supply chains in Taiwan and China. (3) However, CoWoP requires miniaturization to an SLP trace width of 10μm or less for mass production, versus the current 15-20μm. Other remaining challenges include PCB processing precision, yield, and flip-chip mounting. Consequently, Nvidia needs to change chip-side wiring rules and bump pitch, but this would make standardization with existing CoWoS chips difficult. With Nvidia prioritizing support for the Feynman generation, Mr. Nishio believes it has limited capacity for simultaneously developing CoWoP as a separate technology, and has doubts about the feasibility of CoWoP. Mr. Nishio noted that while Nvidia's HGX products use SMX and have a dual-layer structure with one PCB mounted on another PCB, it might want to eliminate the intermediate PCB in this dual-layer structure.
- Organic cores:** (1) ABF substrates that use an organic core are currently the mainstream for advanced packaging. The shift to chiplets and the increase in package sizes have created a need for larger substrates. Packaging is also embedding a rising percentage of silicon components, such as AI chips and HBM. CTE mismatches between substrate and chips cause warping during assembly and solder connection failures. It is important for organic cores to have low CTE and high rigidity. (2) Nittobo's T-glass is a type of glass

cloth used in organic cores, and its ability to control substrate CTE and help to improve strength and electrical properties make it an extremely important material. At present, other glass cloth makers such as Taiwan Glass are unable to keep pace technologically, and Mr. Nishio said Nittobo is effectively the only supplier for high-end products. Nittobo is moving forward with capex in response to requests to increase production from Nvidia, Broadcom, and other end-users, but because it also sees risk from competitors catching up and future oversupply, Mr. Nishio said it is gradually expanding capacity while watching demand. (3) Low CTE and high rigidity make substrate harder and increases the difficulty of drilling. Mr. Nishio said Union Tool is the leader in supplying drilling tools capable of stable micro-hole machining in such hard materials, and other companies are unable to keep pace.

- Glass cores:** Glass cores are superior in terms of low CTE, high rigidity, and flatness, and can mitigate warping in large packaging. Consequently, Mr. Nishio said Intel, AMD, and others view glass cores as a future core material. While many substrate makers are developing glass cores, virtually none are capable of mass production, and Mr. Nishio said Absolics is currently the only company that has mass production facilities and has advanced to the stage of small-scale production. Ibiden, Shinko Electric Industries, and Unimicron are still at the development stage and have not announced specific start dates for mass production. Samsung Electro-Mechanics announced the construction of a mass production plant with Sumitomo Chemical and plans to start mass production prototyping from 2028, but customer certifications will take time after completing plant production. Mr. Nishio said Dai Nippon Printing has not made a decision on full-scale investment. Consequently, glass cores still have inadequate infrastructure, including mass production plants, and Mr. Nishio thinks mass production will be difficult until 2030. The recent announcement at the JPCA Show 2026 that TSMC will cooperate with Ibiden and Innolux to develop glass core substrate for CoPoS has attracted attention.
- Other core materials:** (1) HDI cores replace conventional cores comprised of two layers of copper clad laminate (CCL) with around eight HDI layers (multilayer PCB). HDI cores make it easier to use existing PCB technologies than glass cores, and evaluations are underway. However, substrate makers will need to cooperate with external parties if they are unable to make high-rigidity cores in-house, resulting in a more complex supply chain. Mr. Nishio said production is currently not possible at either Ibiden or Shinko Electric Industries. (2) Regarding ceramic cores, ceramic substrate was used in IBM mainframes and Intel products from the 1980s to the 1990s, and although the mainstream then shifted to organic, there are existing material technologies and mass production plants for ceramic. Mr. Nishio said ceramic cores have attracted attention as one option amid the slow launch of glass cores, but also noted lingering issues in terms of drilling holes in ceramic and bonding with ABF.

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Completed 21 Jul 2026 11:04 AM JST

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