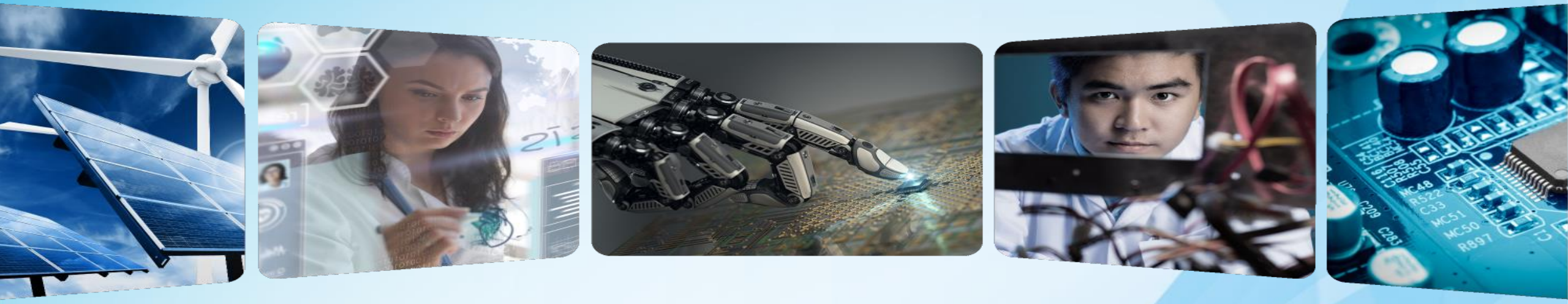
Glass Packaging and Its Reliability

(IEEE Santa Clara Valley EPS Chapter Distinguished Lecture)

John H Lau
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September 24, 2026



This Lecture is supported by the IEEE Electronics Packaging Society's Distinguished Lecturer Program

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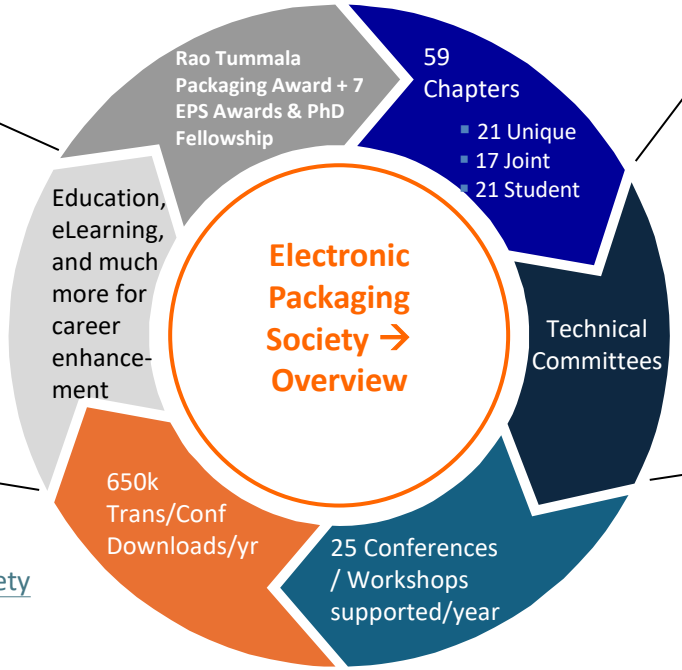
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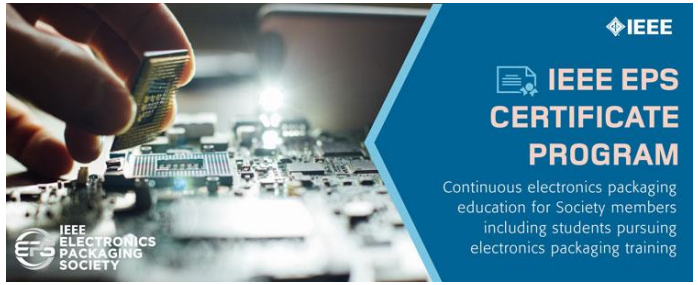
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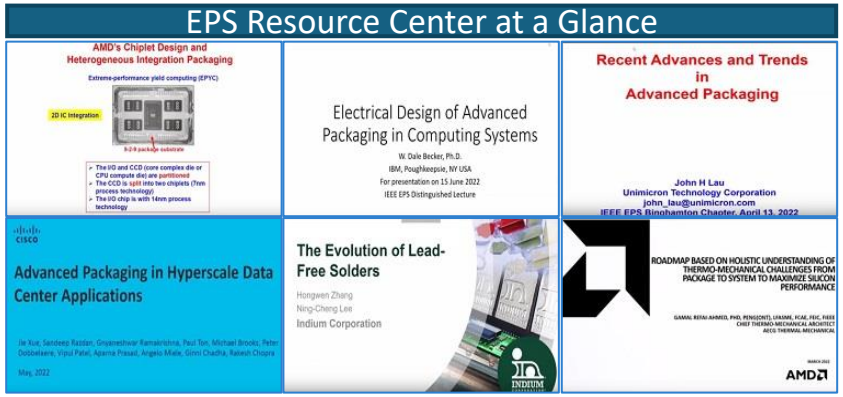


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CONTENTS

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- Definition of Glass Packaging
- Glass as a Temporary Wafer or Panel Carrier
- Intel’s Glass-core Substrate
- TSMC’s Glass-core Substrate/Interposer
- Panel Size Update
- Solder Joint Reliability on Glass-core Substrate
- Summary and Recommendations

Advanced Packaging in Artificial Intelligence (AI) Era

In the past

The performance of a semiconductor product has been driven by Moore's Law. Today, 2nm is in high volume manufacturing.

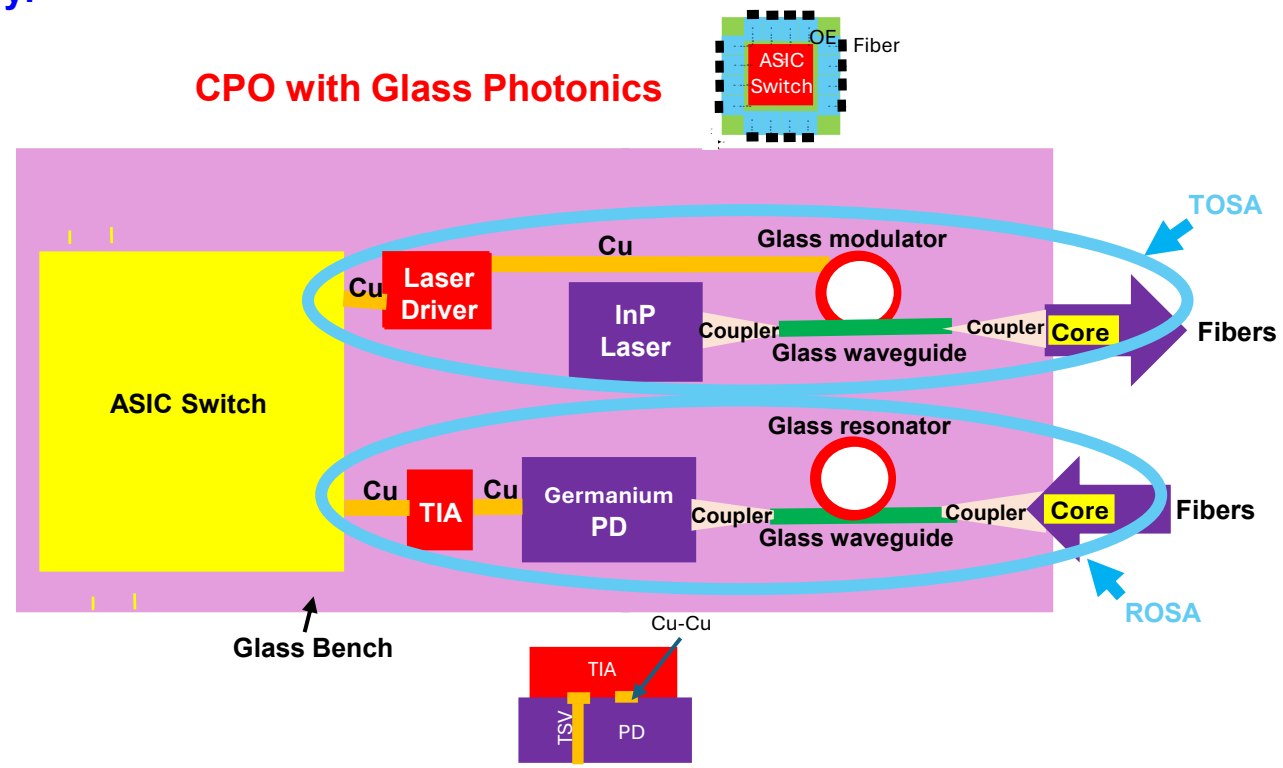
Now and the future

The performance is not only driven by purely Moore's Law but also by:

- how the chips are partitioned and split into smaller chiplets
- how the chiplets are stacked
- how the chiplets are interconnected (Bridges)
- how the chiplets are cooled
- how the chiplets are packaged

The methods, among others, are:

- Chiplets heterogeneous integration [1, 2, 3, 4, 5, 7]
- Bridges connecting chiplets [1, 2, 3, 4]
- FOWLP/FOPLP, TCB, Cu-Cu hybrid bonding [1, 2, 3, 4, 5, 8]
- Panel-level packaging [1, 8]
- Glass packaging [1. 2]
- Co-packaged optics with Si/Glass photonics [1, 2]
- Superior quality and reliability [1, 2, 3, 6]
- Superior thermal management [2]
- Innovative materials and processes [1 - 10]
- Integrate into the existing manufacturing environments
- etc.



[1] Lau, J. H., and K. N. Chiang, *Hybrid Bonding, Glass, and AI-Assisted Simulation for Chiplets Heterogeneous Integration*, (547 pages), Springer, 2026.
[2] Lau, J. H., and X. Fan, *Hybrid Bonging and Thermal Management for Chiplets and Heterogeneous Integration*, (645 pages), Springer, April 2025.
[3] Lau, J. H., *Flip Chip, Hybrid Bonding, Fan-In, and Fan-Out Technology*, (501 pages), Springer, 2024.
[4] Lau, J. H., *Chiplet Design and Heterogeneous Integration Packaging*, (525 pages), Springer, 2023.
[5] Lau, J. H., *Semiconductor Advanced Packaging*, (498 pages), Springer, 2021.
[6] Lau, J. H., and N. C. Lee, *Assembly and Reliability of Lead-Free Solder Joints*, (527 pages), Springer, 2020.
[7] Lau, J. H., *Heterogeneous Integrations*, (367 pages), Springer, 2019.
[8] Lau, J. H., *Fan-Out Wafer-Level Packaging*, (303 pages), Springer, 2018.
[9] Lau, J. H., *3D IC Integration and Packaging*, (458 pages), McGraw-Hill, 2016.
[10] Lau, J. H., *Through-Silicon Via (TSV) for 3D Integration*, (487 pages), McGraw-Hill, New York, 2013.

Why Glass Packaging?

It is because of high-performance computing (HPC) and Data Centers driven by Artificial Intelligence (AI)!

- The AI computing power arms race has expanded beyond core chip processing capabilities to encompass a materials revolution - the very "skeleton" of the technology.
- Glass substrates/interposer - once seemingly unassuming but now undergoing a spectacular transformation within the realm of semiconductor packaging - have emerged as the central protagonists of this revolution.
- As the computing power of AI chips continues to escalate - alongside the integration of increasingly high-bandwidth memory (HBM) - packaging processes have grown correspondingly complex. Consequently, traditional copper-clad laminates (CCLs) - typically composed of resin and fiberglass fabric - have begun to encounter their physical limits.
- When substrate/interposer dimensions exceed 120mm to 140mm, issues such as the "warping" of organic materials and thermal dissipation bottlenecks place chip stability in jeopardy.
- Leveraging their inherent physical properties, glass substrates/interposers have therefore made a cross-industry leap - transitioning from the display panel sector to the battleground of advanced semiconductor packaging.

Definition of Glass Packaging

The glass (substrate or interposer) is a part of a package structure!

or

A glass package must have a glass substrate or interposer!

Glass panel or wafer as a temporary carrier of FOWLP or FOPLP – not part of a package

Glass as a Temporary Panel Carrier for FOPLP

People say: "… the glass substrate of fan-out panel-level packaging (FOPLP) …"

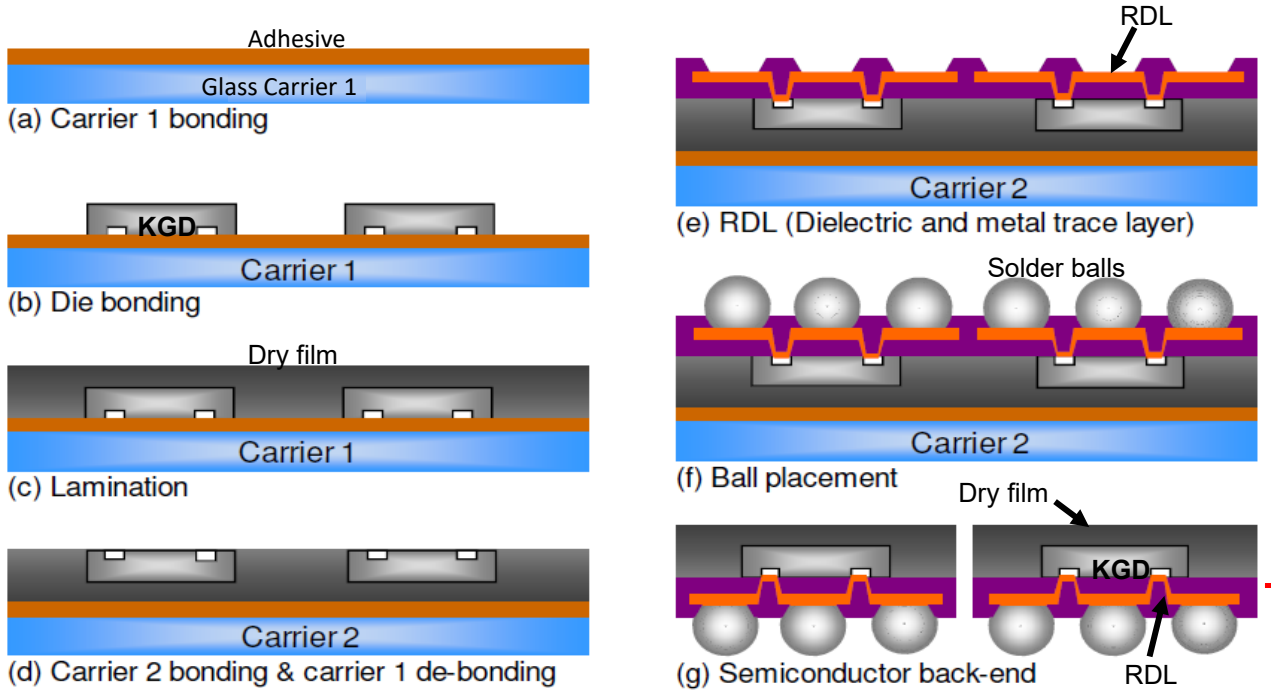
This is wrong!

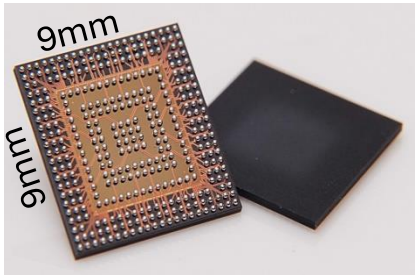
There is no glass substrate in the FOPLP!

FOPLP is not a glass packaging!

FOPLP process with Glass as a Temporary Carrier

G2: 370mm x 470mm

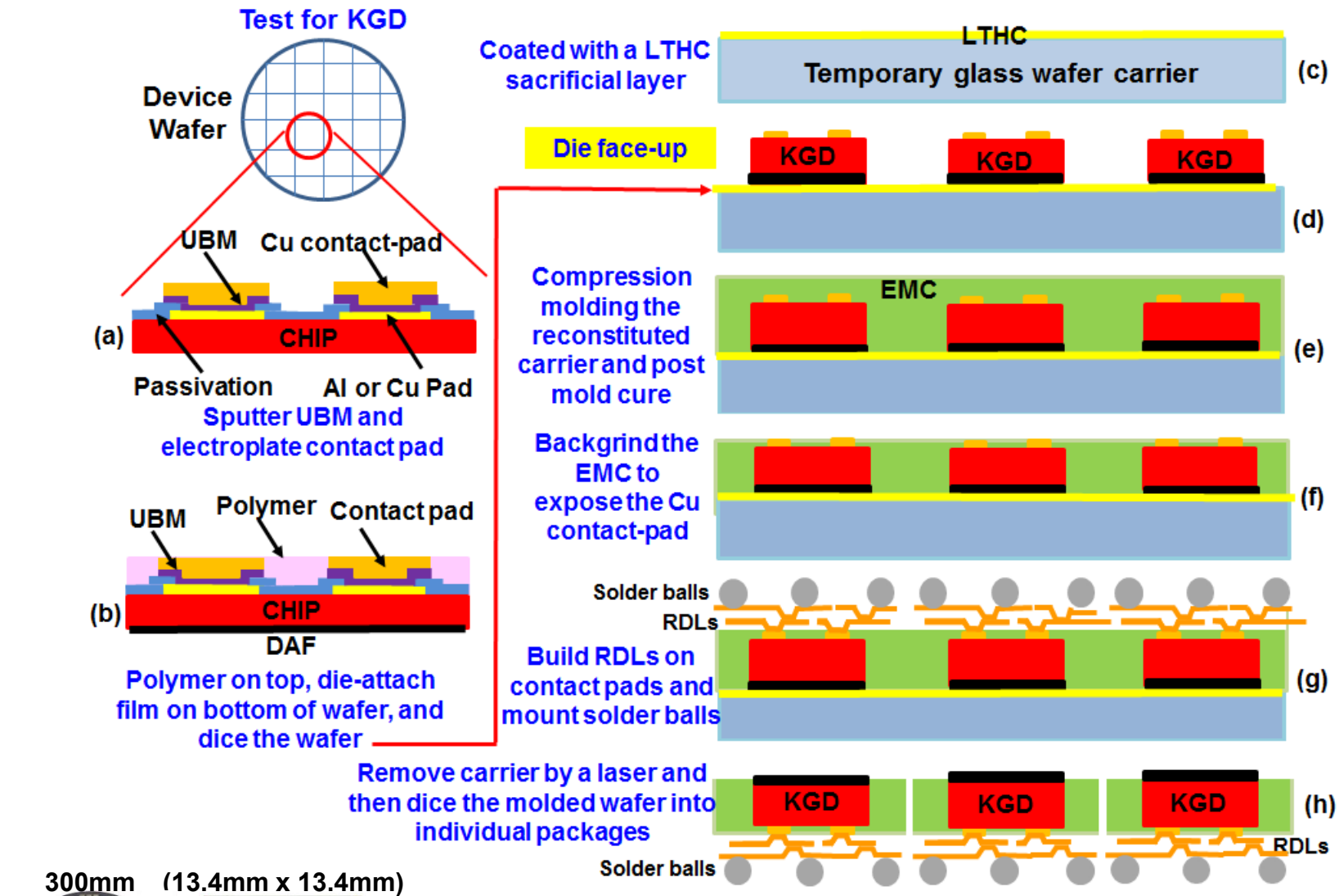




- **FOPLP with RDLs substrate**
- **There is no glass substrate**

H. Chang, D. Chang, K. Liu, H. Hsu, R. Tai, H. Hunag, Y. Lai, C. Lu, C. Lin, and S. Chu, "Development and Characterization of New Generation Panel Fan-Out (PFO) Packaging Technology", *IEEE/ECTC Proceedings*, 2014, pp. 947-951

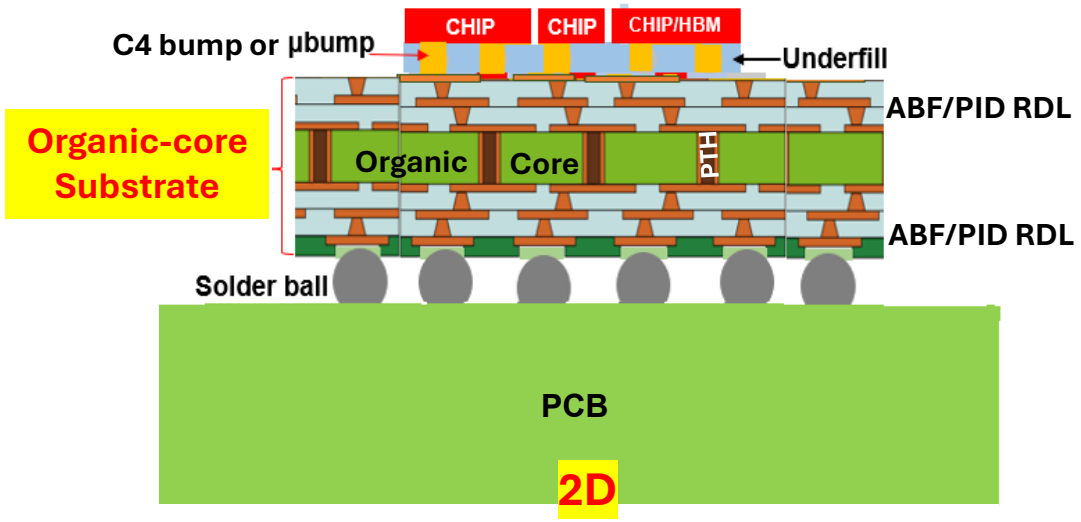
Glass as a Temporary Wafer Carrier for FOWLP

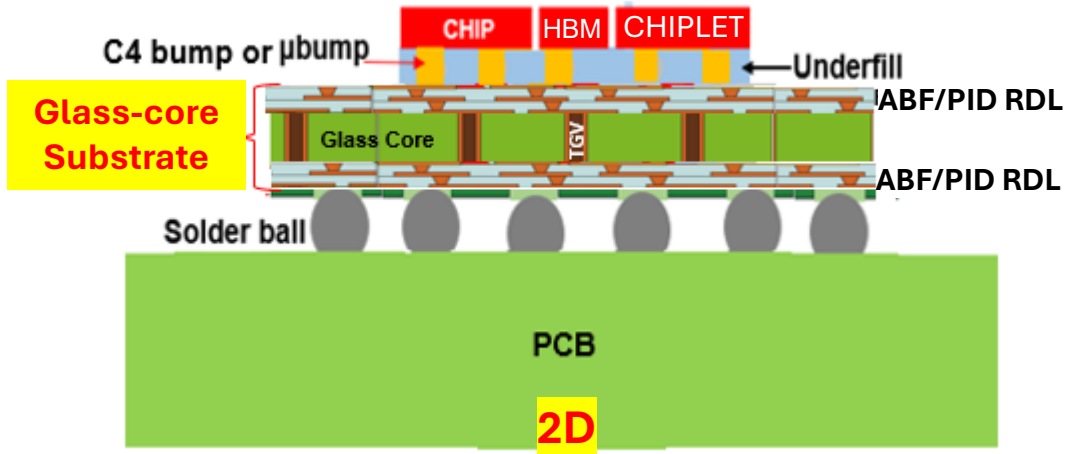


Lau, J. H., C. Ko, et al., "Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT*. Vol. 8, Issue 6, June 2018, pp. 991-1002.

Organic-core Substrate vs. Glass-core Substrate

Organic-core Substrate vs. Glass-core Substrate





The key advantages of glass-core substrate over the organic-core substrate are:

- Superior flatness
- Better dimensional stability
- Better heat resistance
- Finer L/S RDLs
- Cu-Cu hybrid bonding for chiplets
- etc.

Lau, J. H., and K. N. Chiang, *Cu-Interconnects, Glass, and AI-Assisted Simulation for Chiplets Heterogeneous Integration,* (547 pages), Springer, New York, April 2026.

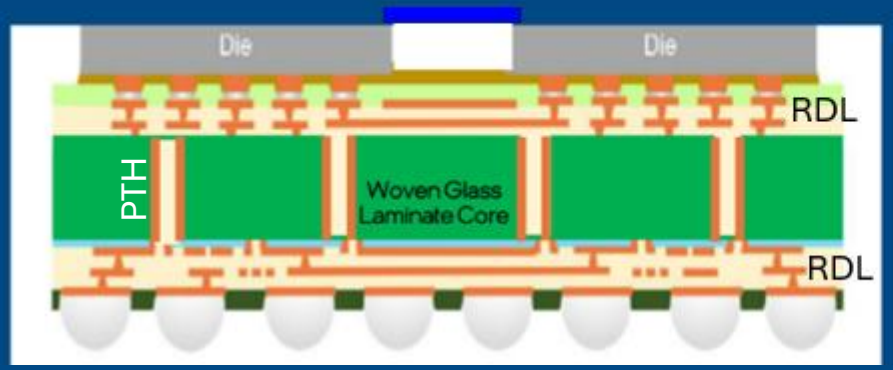
Intel's Glass Packaging

On September 18, 2023, …

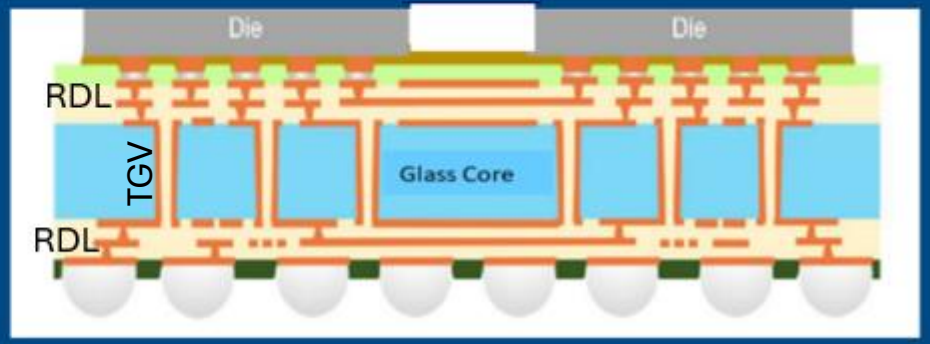
- **Intel has announced a new glass-substrate technology for the next generation of high-power processors.**
- **Intel is on the path to delivering 1 trillion transistors on a package by 2030 and its ongoing innovation in advanced packaging including glass substrates will help achieve this goal.**

Intel Glass Core Substrate

Organic Substrate



Glass Core Substrate



Compared to organic substrates, glass substrates offer:

- Superior flatness
- Better dimensional stability
- Better heat resistance
- Finer RDL (L/S)

*Based on internal analysis of Intel products and projections of future Intel products

intel

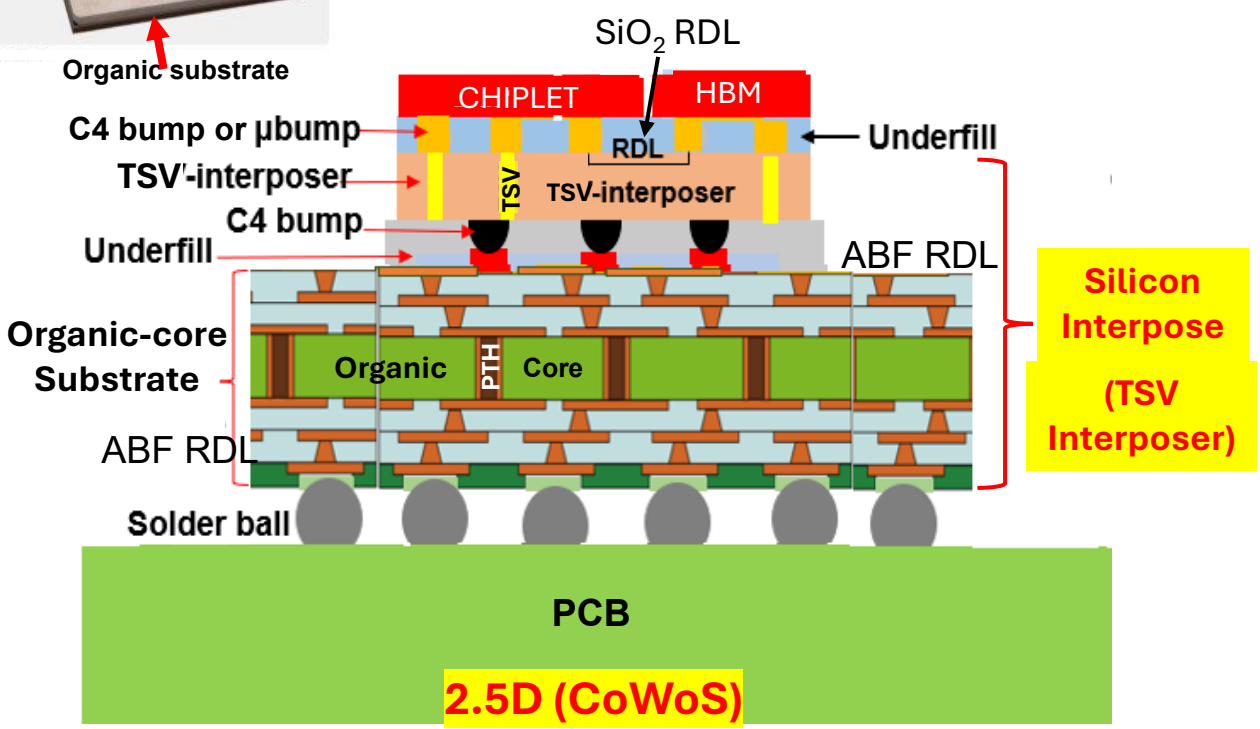
6

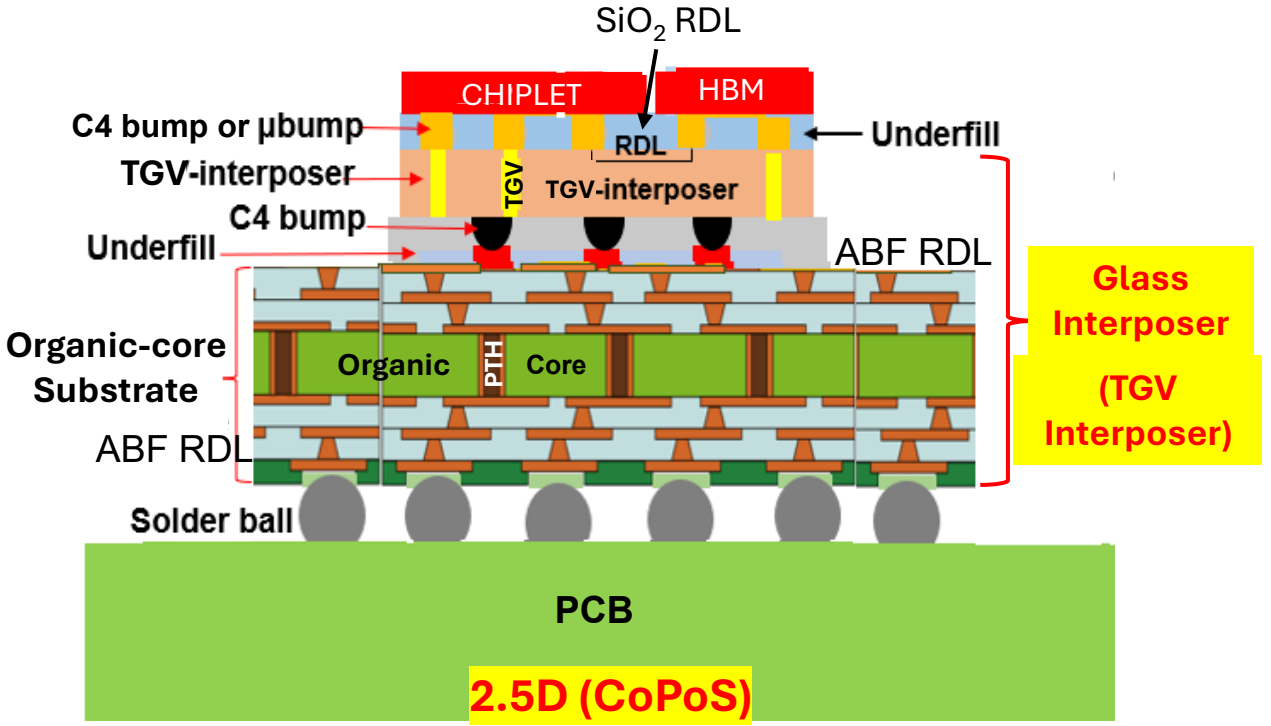
- **On September 18, 2023, Intel told the world that they had spent more than one billion dollars in glass packaging R&D. It is for their 1 trillion transistors on a package to be shipped by 2030**
- **During July 2025, Intel stopped all the in-house glass manufacturing activities and started licensing its extensive glass patents (> 700) to third suppliers.**
- **On July 28., 2026, Intel signed a memorandum of understanding with Lens International (HK) limited on how to fabricate crack-free through-glass via.**

TSV Interposer vs. TGV Interposer

Silicon TSV-interposer vs. Glass TGV-interposer





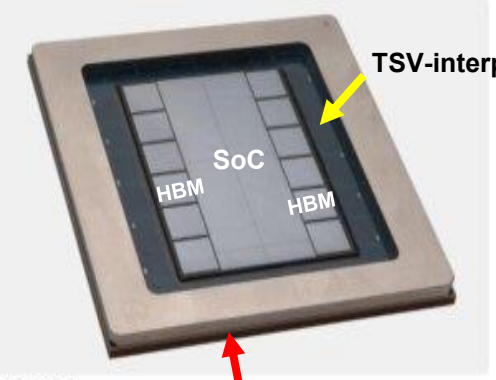


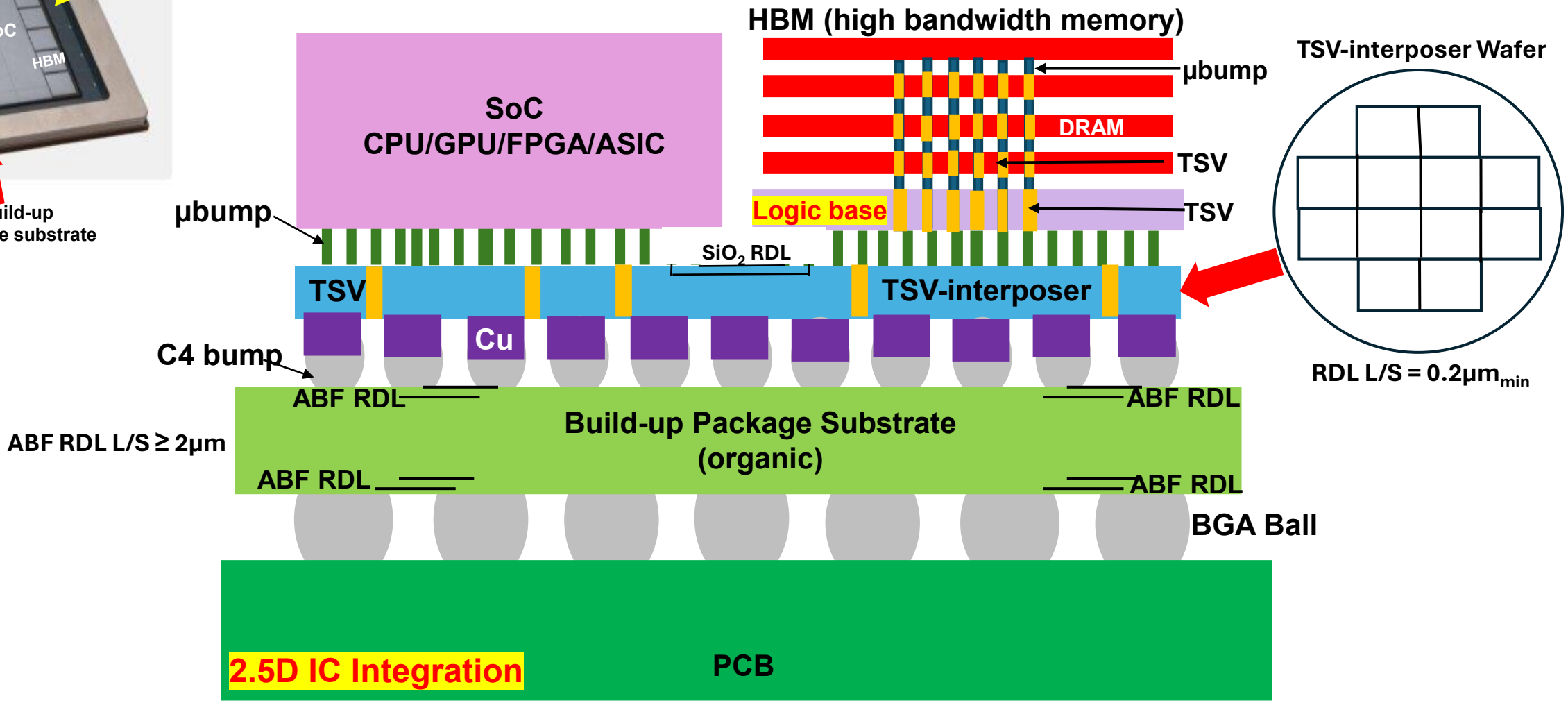
The key advantages of glass TGV-interposer over the silicon TSV-interposer are:

- Better electrical isolation
- Flatter surface
- Lower D_f and D_k
- Better area efficiency
- etc.

Lau, J. H., and K. N. Chiang, *Cu-Interconnects, Glass, and AI-Assisted Simulation for Chiplets Heterogeneous Integration,* (547 pages), Springer, New York, April 2026.

Package of Choice for HPC and Data Centers Driven by AI
CoWoS (chip on wafer on substrate)





CoWoS has been in HVM since 2013.

TSMC's Glass Packaging - CoPoS

During the TSMC 2025 North America Technology Symposium (April 23), the company announced its CoPoS (chip on panel on substrate) technology, which is competing with its CoWoS (chip on wafer on substrate) technology.

"310mm x 310mm Glass Panel"

There are many rumors on the CoPoS package structure!

Gag Order of CoPoS

For the very first time, in May 2026, TSMC issued a strict "gag order" and exclusivity mandate to its advanced packaging supply chain. This restriction targets companies involved in the panel-based CoPoS rather than the current-generation wafer-based CoWoS lines.

Nature of the "Gag Order" & Exclusive Agreements

Non-Disclosure Overhaul: TSMC is forcing Taiwanese materials, equipment, and manufacturing suppliers to sign aggressive legal agreements to ensure proprietary research and development secrets do not leak to rivals.

Mandatory Exclusivity: Beyond simple secrecy, the agreements act as a "lock-in" decree, legally barring these supply chain partners from selling the same CoPoS-generation tools or materials to any other semiconductor firms for several years during mass production.

The Strategic Intent

Blocking Intel and Samsung: Intel recently restarted advanced packaging expansions in Malaysia, and Samsung is heavily pitching its alternative solutions. Because some equipment manufacturers holding "TSMC Vendor Codes" began securing spillover orders from Intel, TSMC moved to legally choke off their access to next-gen supply lines.

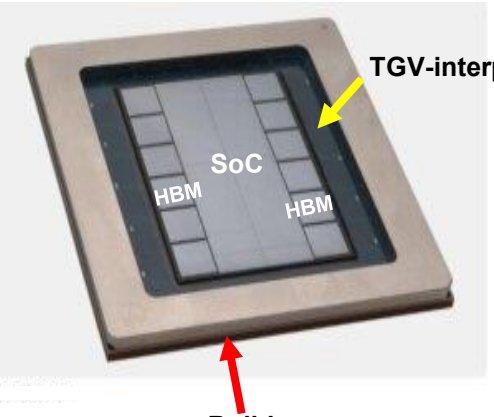
Defending the Packaging Moat: Next-gen AI chips are hitting size ceilings on traditional silicon interposers. Rival tech like Intel's EMIB has started peeling away some market interest. TSMC intends to build an impenetrable barrier around CoPoS to prevent competitors from capitalizing on its multi-year R&D investments.

What's the package structure of CoPoS?

The tear-down of the first CoPoS product in Q1 of 2029 will tell!

I guess there could be three versions!

CoPoS (Chip on Panel on Substrate): v1



SoC
CPU/GPU/FPGA/ASIC

μbump

HBM

μbump

TSV

DRAM

Logic Base

SiO_2 RDL

TGV

TGV interposer

Cu

C4 bump

ABF RDL

ABF RDL L/S ≥ 2μm

Build-up Organic Package Substrate

ABF RDL

BGA
Ball

PCB

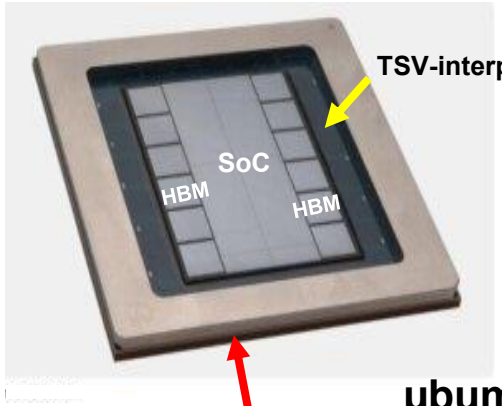
2.5D IC Integration

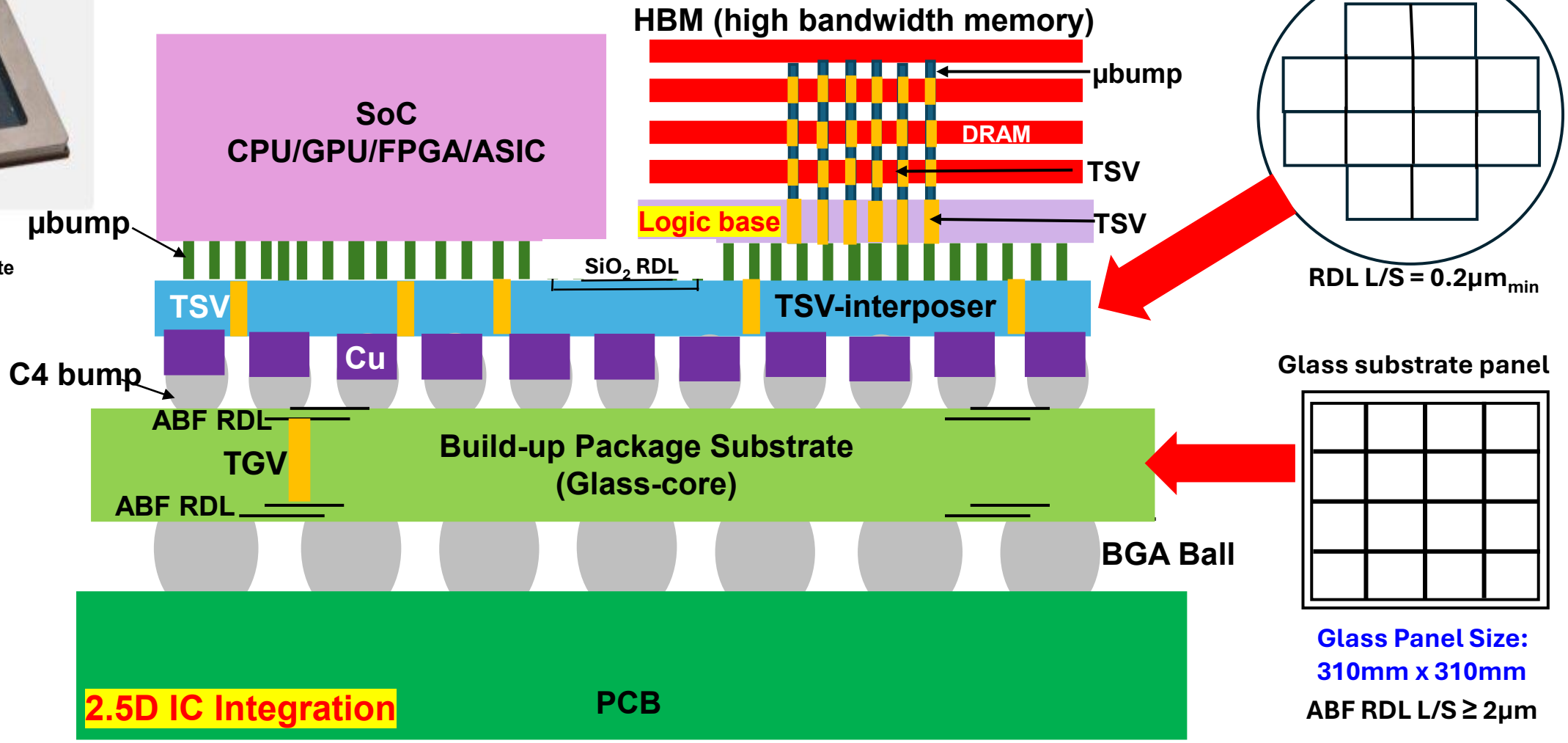
TGV Interposer Panel

Glass Panel Size:
310mm x 310mm

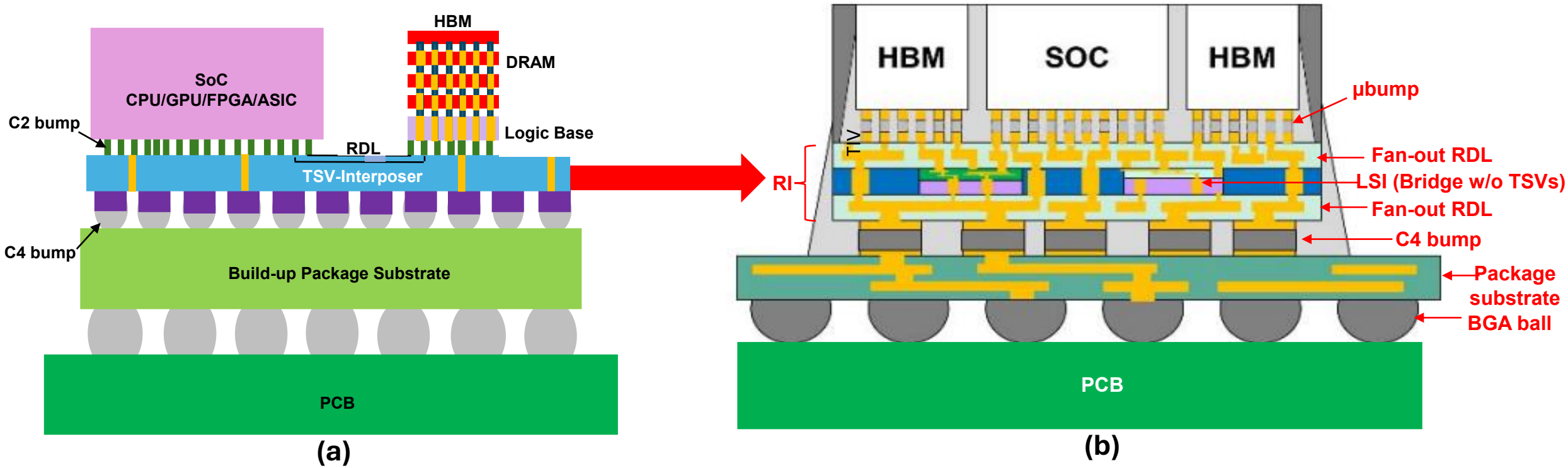
RDL L/S = $0.2\mu m_{min}$

CoPoS (Chip on Panel on Substrate): v2





TSMC's CoWoS-L with Embedded LSIs (Local Silicon Interconnects), i.e., Si-Bridges



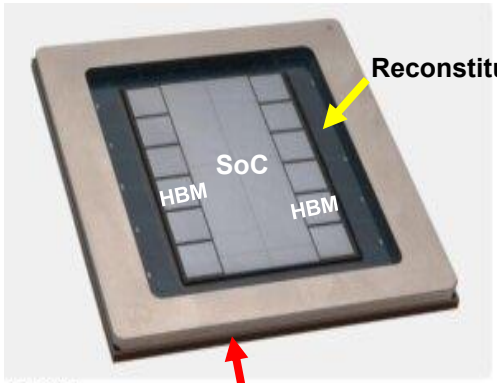
CoWoS

CoWoS-L (Bridge with Fan-Out RDLs)

TSV-Interposer is replaced by the RI (Reconstituted-Interposer) which consists of Si Bridge (LSI) embedded in Fan-Out EMC with fan-out RDLs

NVIDIA's Rubin has been shipped since June 1, 2026 with CoWoS-L

CoPoS (Chip on Panel on Substrate): v3



Reconstituted-interposer

Glass-core
package substrate

Si bridge chip wafer

Glass Temporary Carrier wafer

HBM SOC HBM

μbump

RI

TIV EMC

Fan-out RDL

LSI (Bridge)

Fan-out RDL

C4 bump

ABF RDL

Glass-core
Package substrate

TGV

Build-up Package Substrate
(Glass-core)

ABF RDL

BGA ball

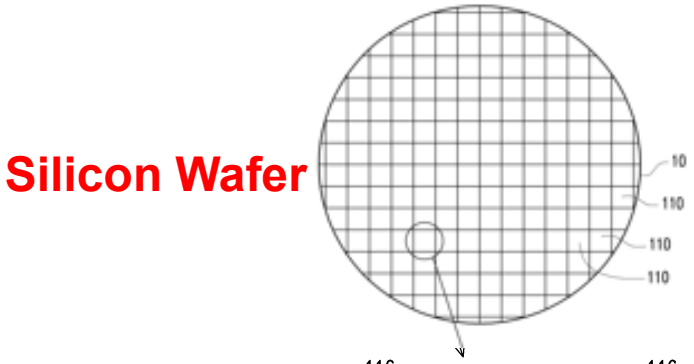
PCB

Glass Panel

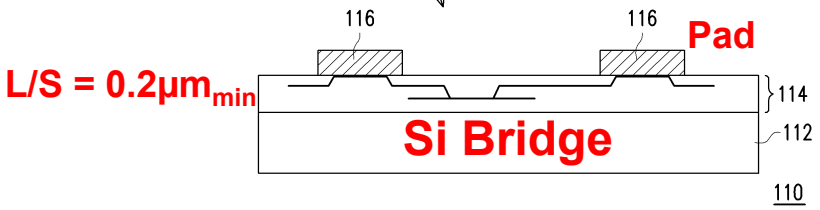
310mm x 310mm

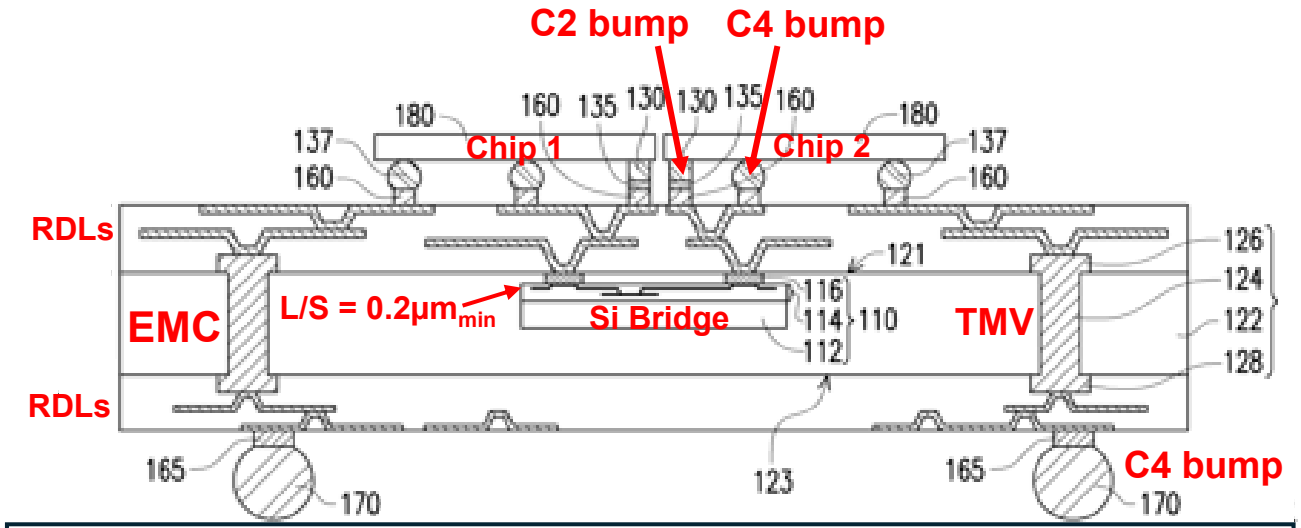
ABF RDL L/S ≥ 2μm

Bridge Embedded in Panel Fan-Out EMC with RDLs



Bridge RDLs are made by the 64nm process technology (L/S = 0.2μm$_{min}$)

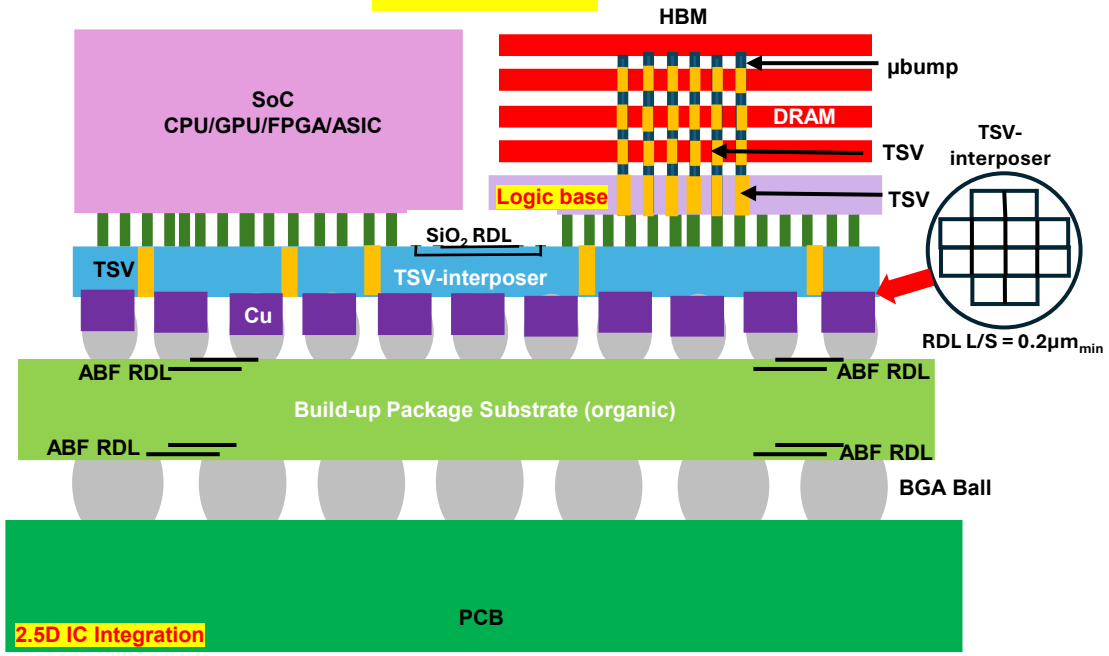




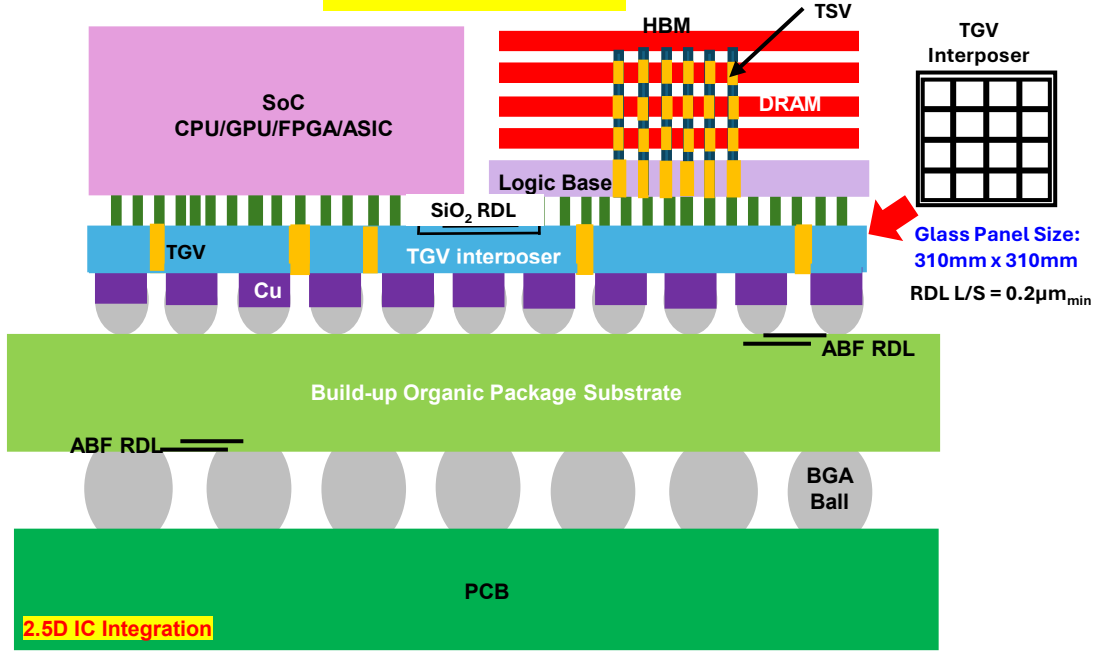
Package Substrate

Unimicron
U.S. patent 11,410,933,
filed on May 7, 2021.

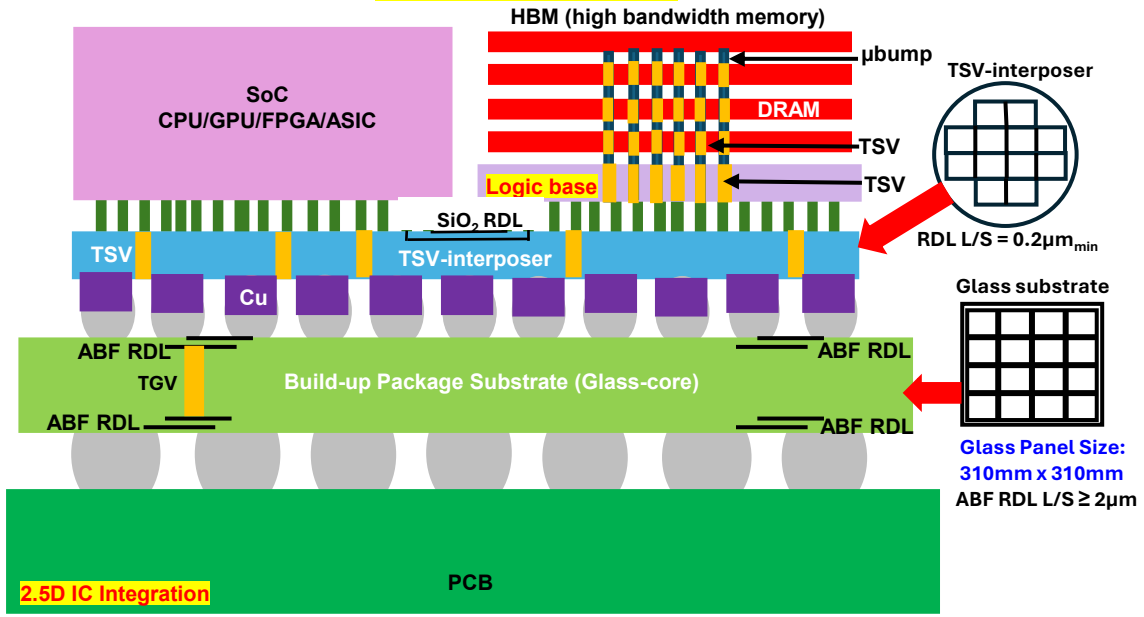
CoWoS



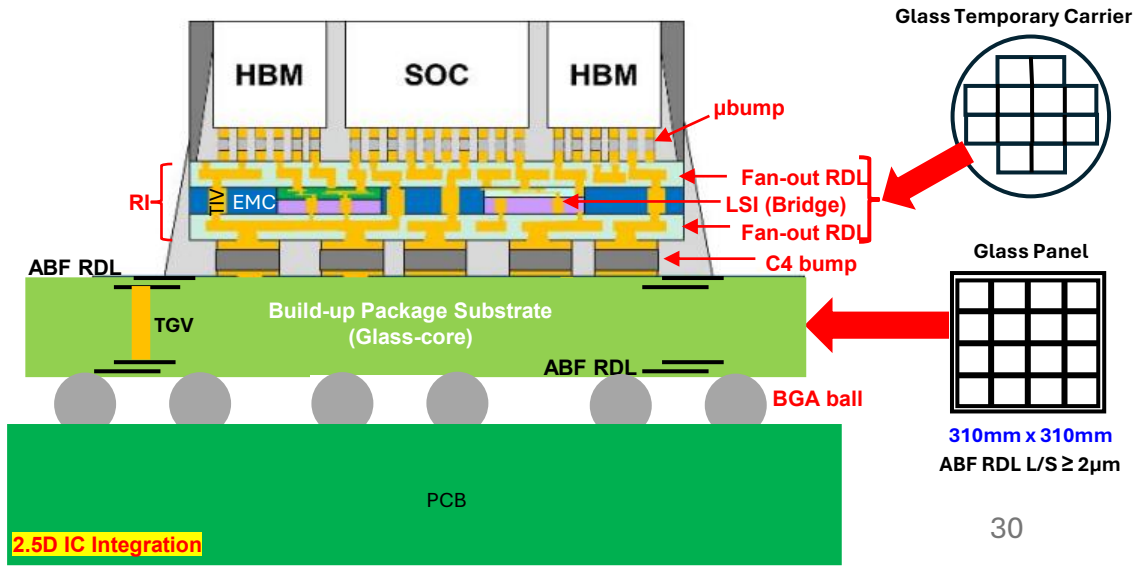
CoPoS-v1



CoPoS-v2

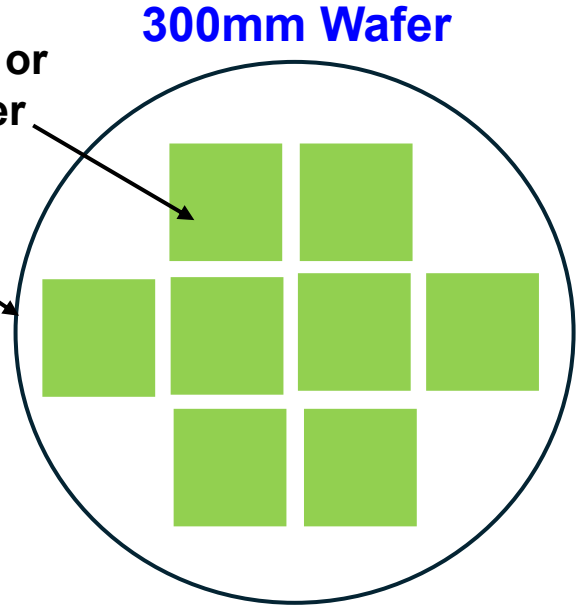


CoPoS-v3



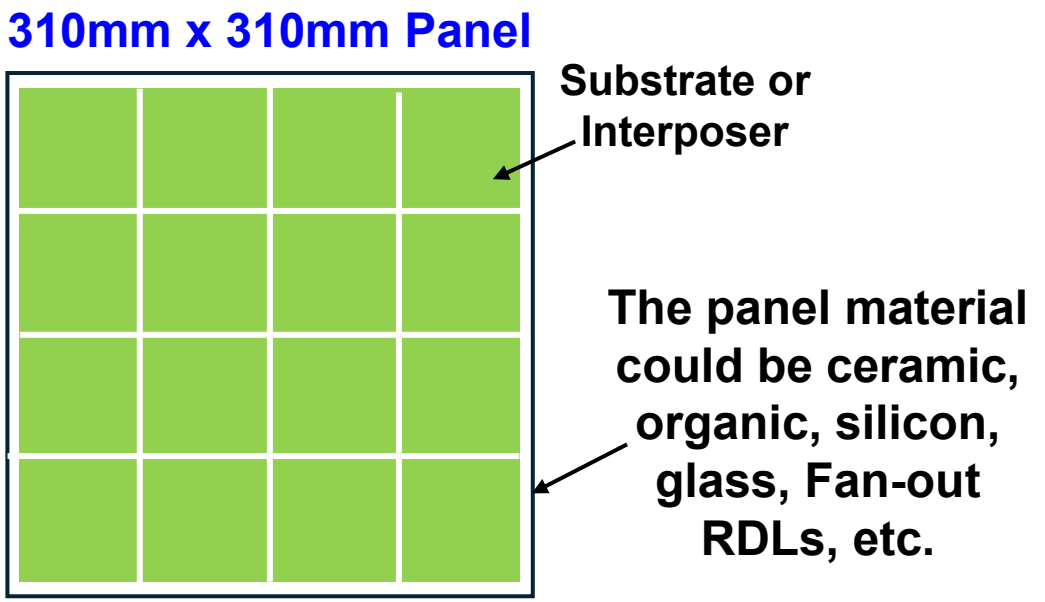
Interposers or Substrates Fabricated on a round wafer (WLP) and on a rectangular panel (PLP) – Area Efficiency.

WLP



- 8 Substrates or Interposers
- Area Efficiency ~ 50%

PLP



- 16 Substrates or Interposers
- Area Efficiency ~ 88%

- WLP has been in high volume production for more than 25 years.
- In the past few years PLP has been attracting lots of tractions. The one and only reason is PLP has better area efficiency (which leads to lower costs) compared to WLP.
- The larger the interposer (or substrate) size, the larger the area efficiency of the PLP (which leads to lower cost). This is very important for HPC and data centers in AI era. Because the interposer size is very large, e.g., 2500mm^2 (8HBM) or 3320mm^2 (12HBM). There are less than 10 physically possible interposers on a 300mm wafer.

Lau, J. H., *Semiconductor Advanced Packaging*, (498 pages), Springer, New York, 2021.

Status on CoPoS

- TSMC has planned to establish its first CoPoS pilot line at Chiayi in 2026, with mass production facilities located at its P4 and P5 plants in AP7, Chiayi.

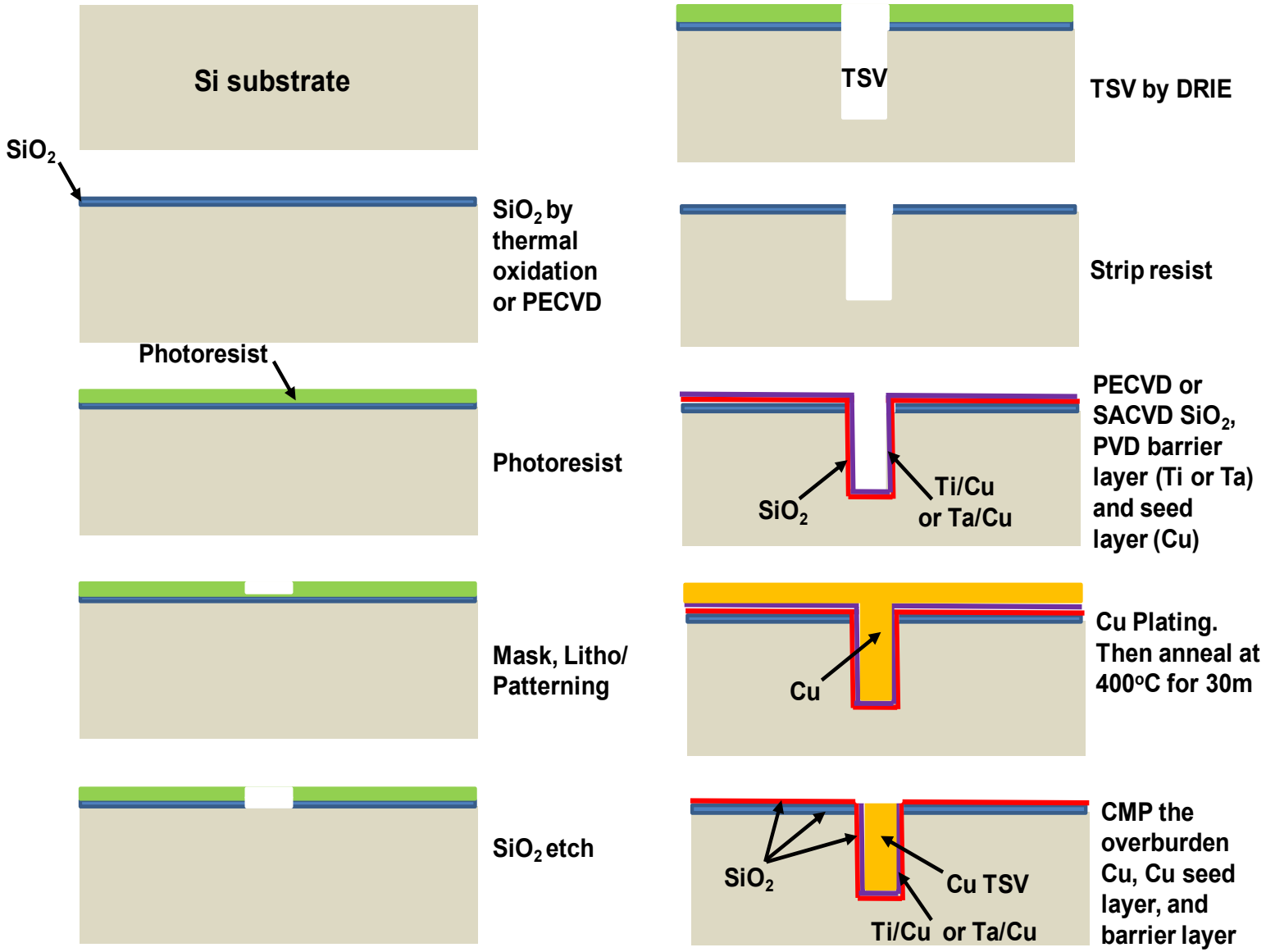
- Mass production is expected to begin as early as the first half of 2029.

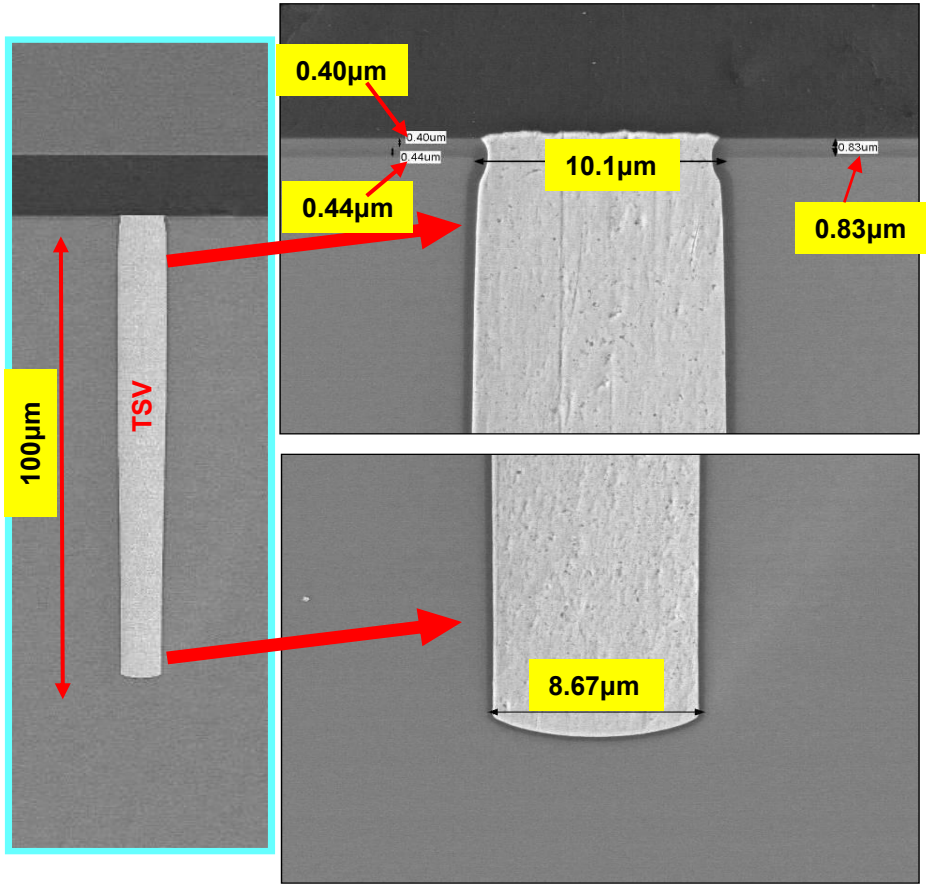
- The first wave of equipment supply chains has been largely finalized, with specifications and order volumes confirmed. These are:
  - International companies: KLA, TEL, Screen, Applied Materials, and Disco
  - Taiwanese companies: Innolux, Sin-Yun, Hung-Soo, Chung Hwa, Chromium, Chih-Sheng, and Da-Long

TSMC license some of Intel's glass patents and work with Ibiden and Innolux to make the TGVs and RDLs on a 310mm x 310mm glass panel.

TSV and RDLs

TSV Fabrication (Via-diameter = 5-10μm)

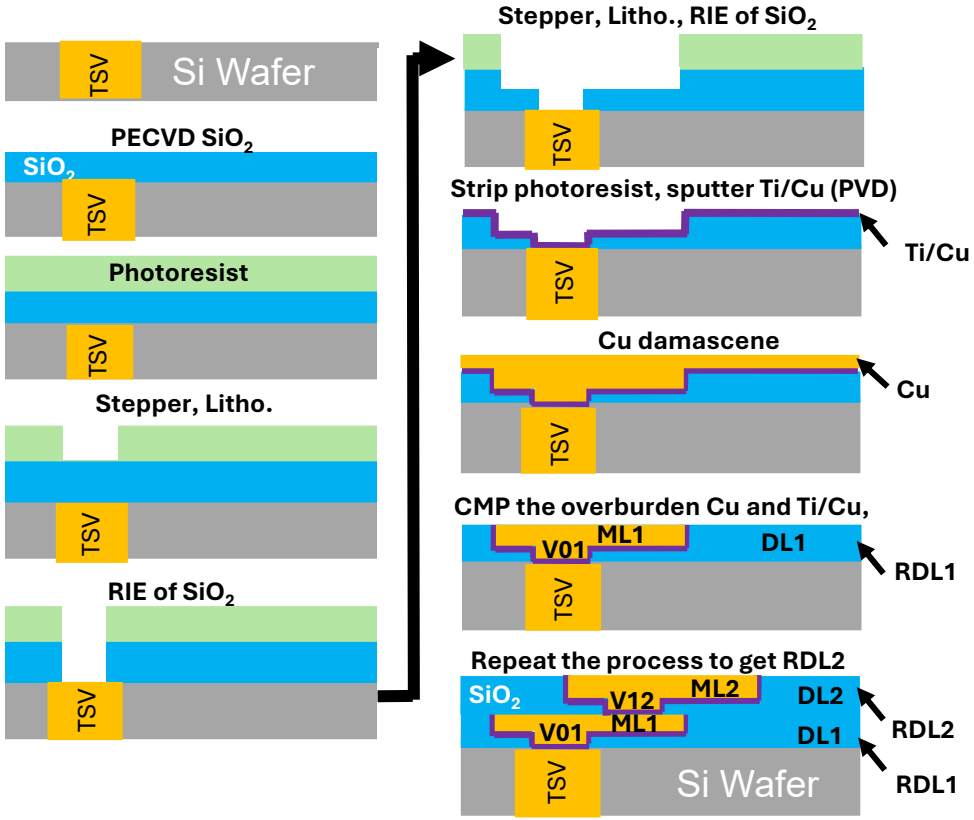


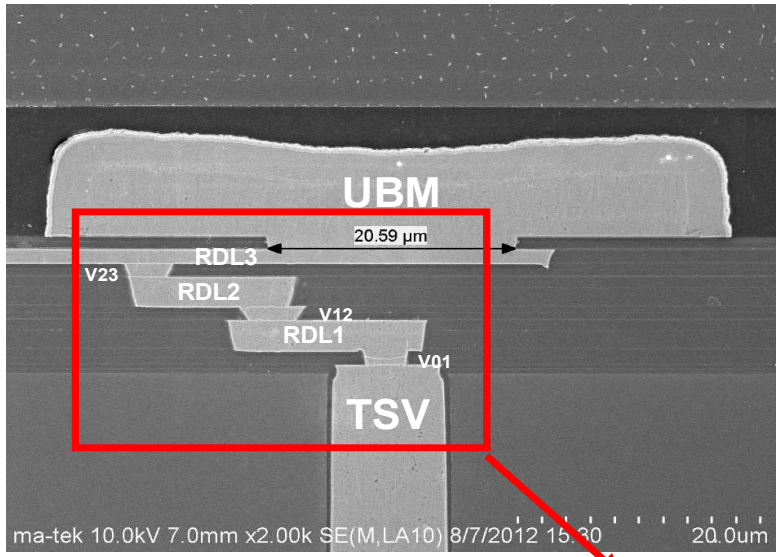


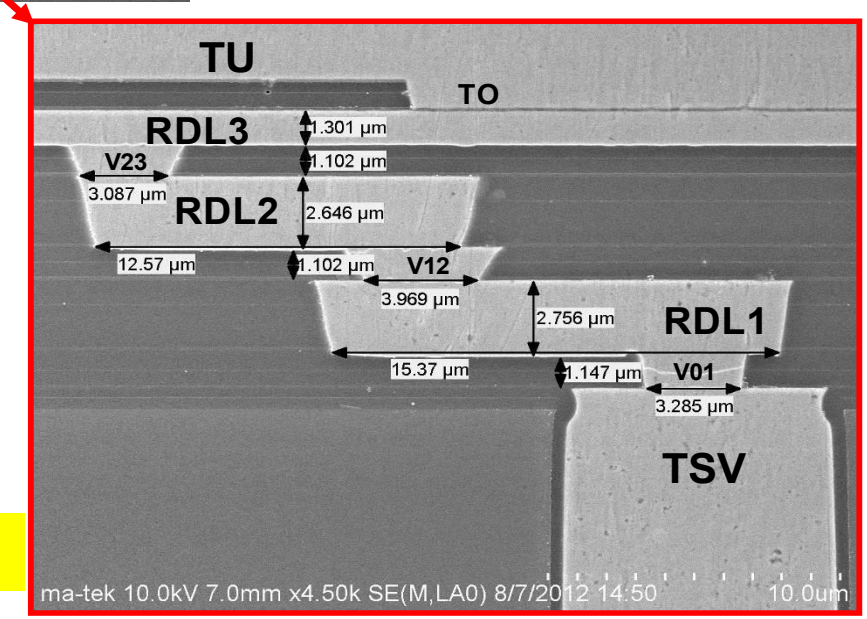
Lau, J. H., *Through-Silicon Via (TSV) for 3D Integration*, (487 pages), McGraw-Hill, New York, 2013.

RDL Fabrication (Minimum Pitch = 0.4μm)

PECVD + Dual Cu-Damascenes + CMP







- SiO_2 as dielectric layer (~1μm)
- L/S (< 2μm)
- PECVD
- Stepper
- PVD
- Dual Cu-damascene
- CMP

RDLs minimum pitch = 0.4μm

J. H. Lau, P. Tzeng, C. Lee, C. Zhan, M. Li, J. Cline, et al., "Redistribution Layers (RDLs) for 2.5D/3D IC Integration", *IMAPS 2013 Proceedings*. Also, *Journal of Microelectronic Packaging*, First Quarter 2014, pp. 16-24.

TGV and RDLs

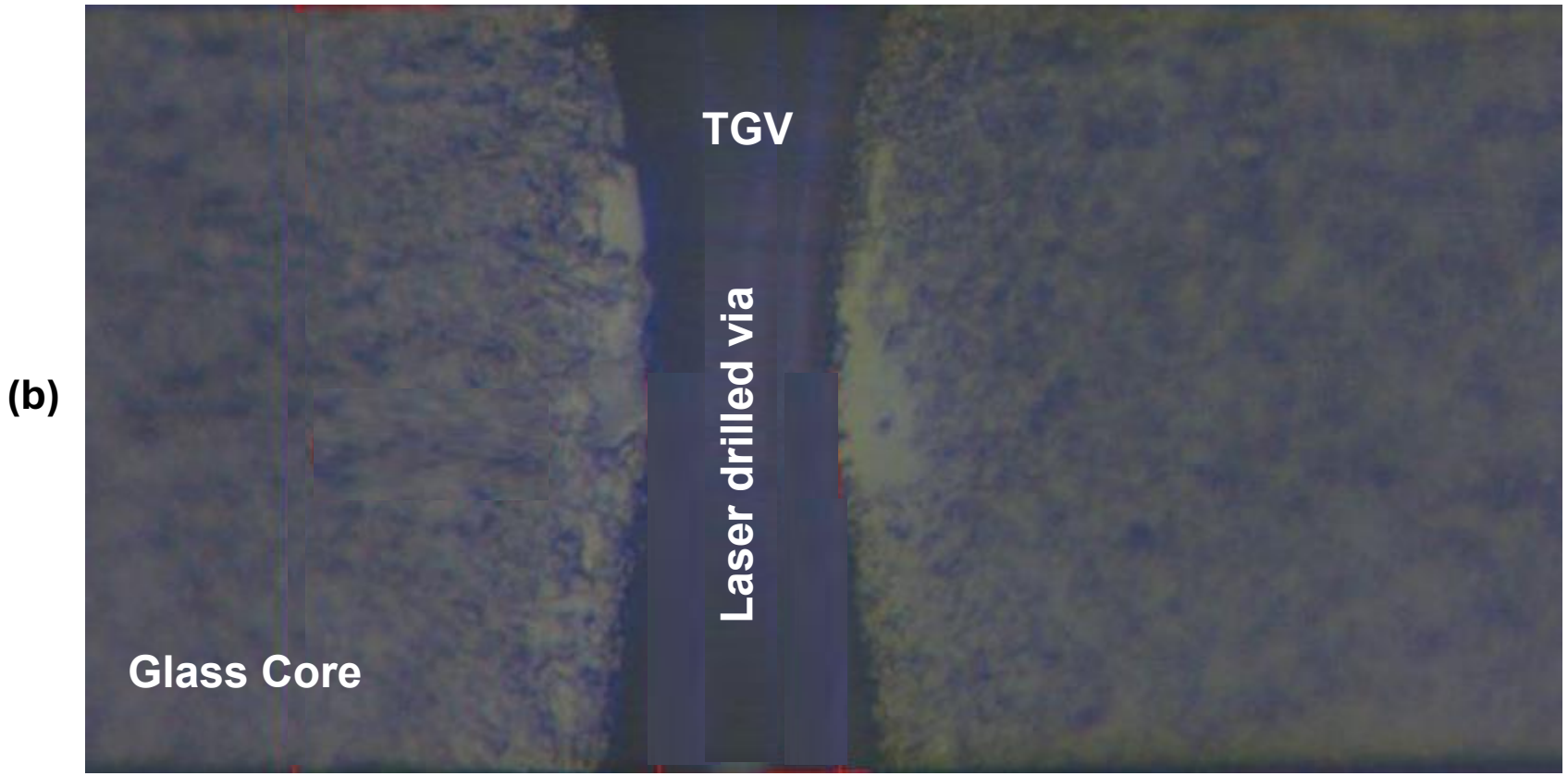
- The TGVs are usually fabricated by the laser drilling such as the laser induced deep etching (LIDE) developed by LPKF Laser & Electronics AG in 2017.

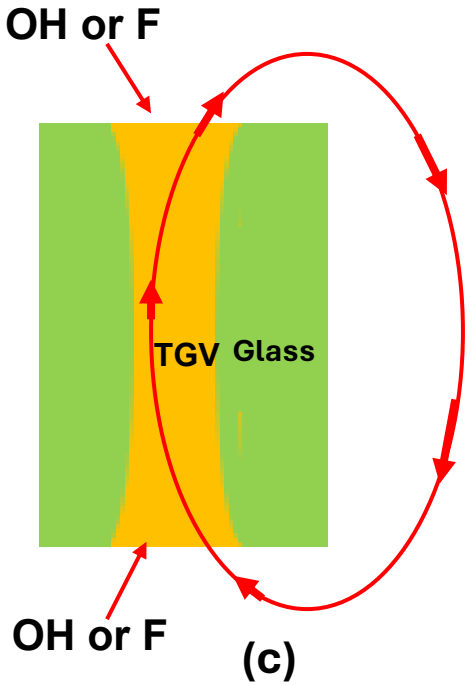
- The diameter of TGV in HPC and data centers in AI era is 20 - 50μm

- The most common used glass materials are:
  - SCHOTT AF 32 alkali-free flat glass
  - CORNING HPFS 7980 high purity non crystalline fused silica glass
  - Both materials have low CTE, which are close to that of silicon

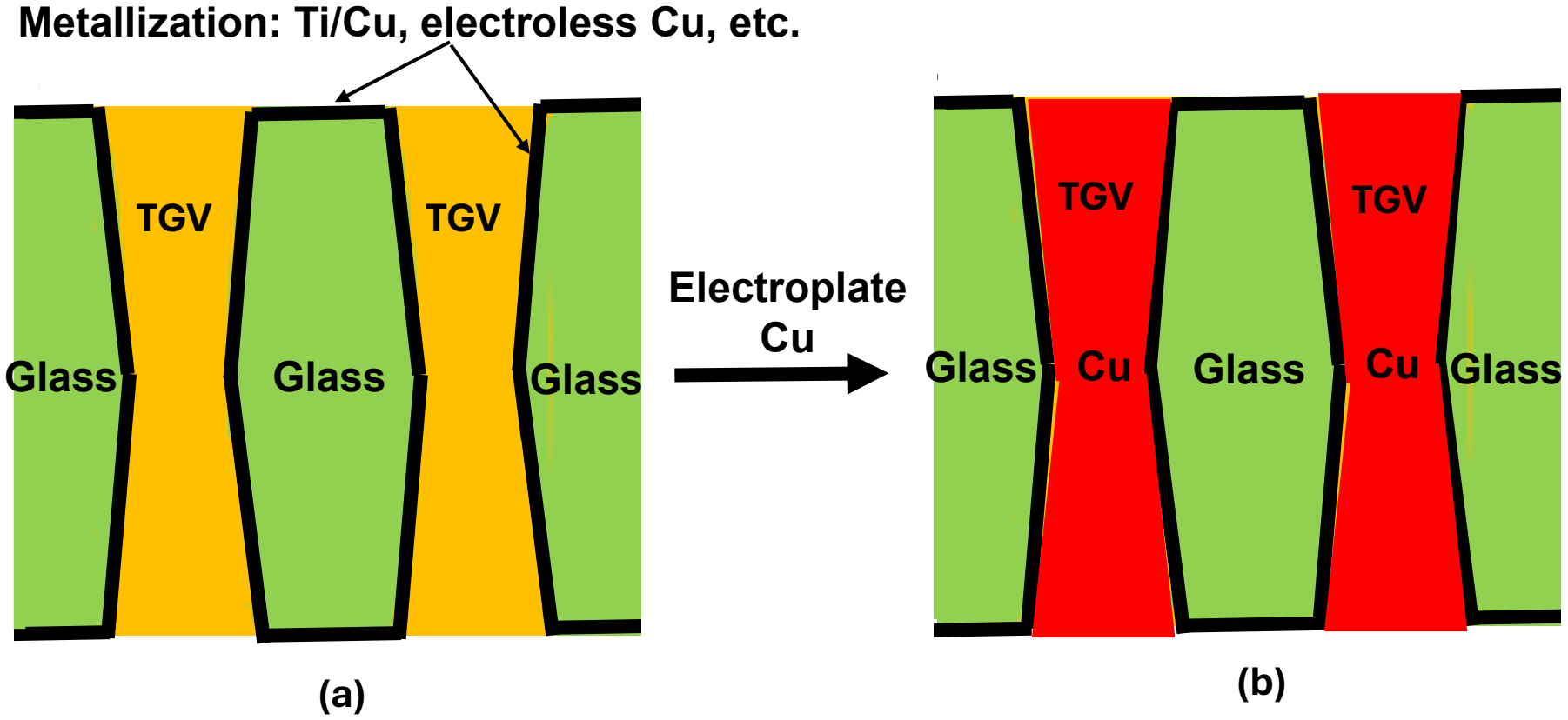
(a) TGV Process flow. (b) SEM image of a TGV. (c) Etch solution mechanism

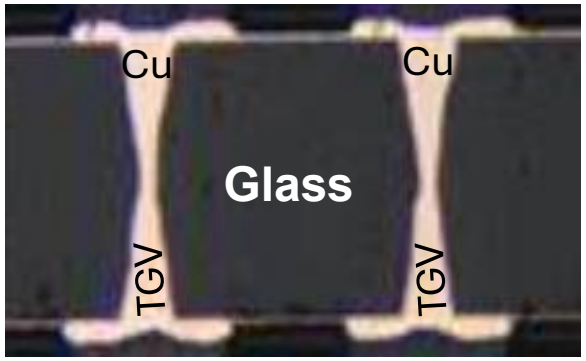






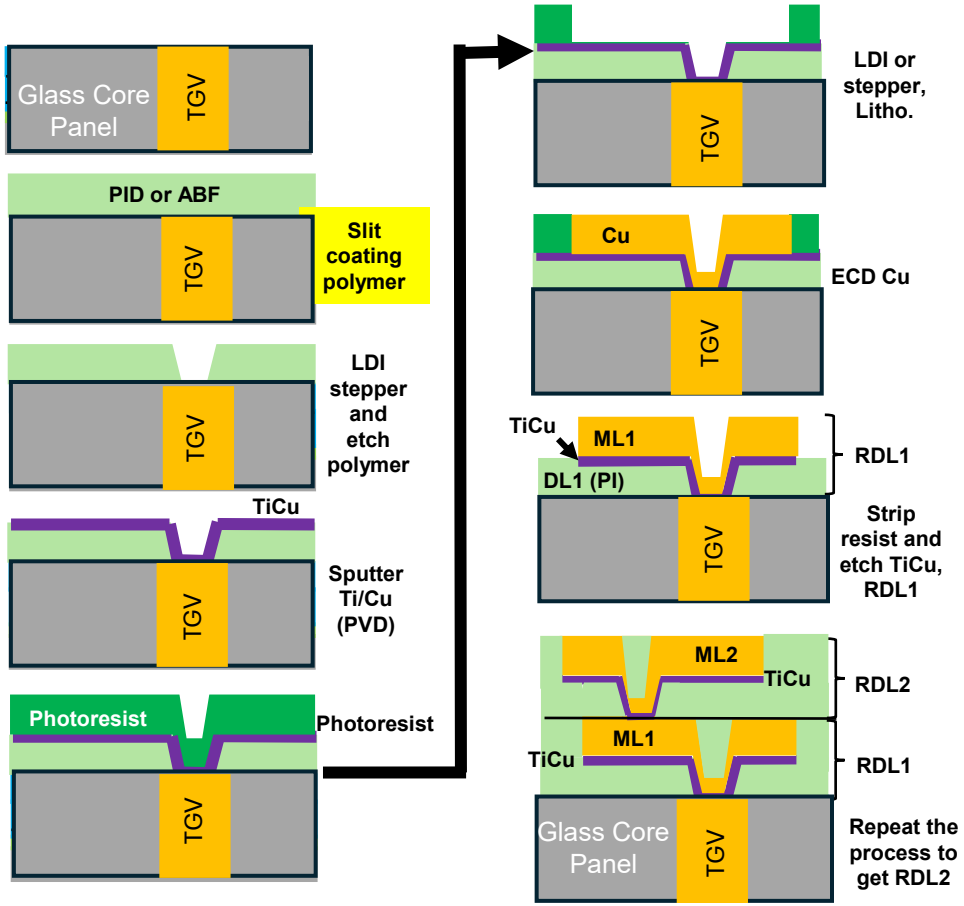
(a) TGV sidewall metallization. (b) Cu plating. (c) An image of Cu-filled TGV





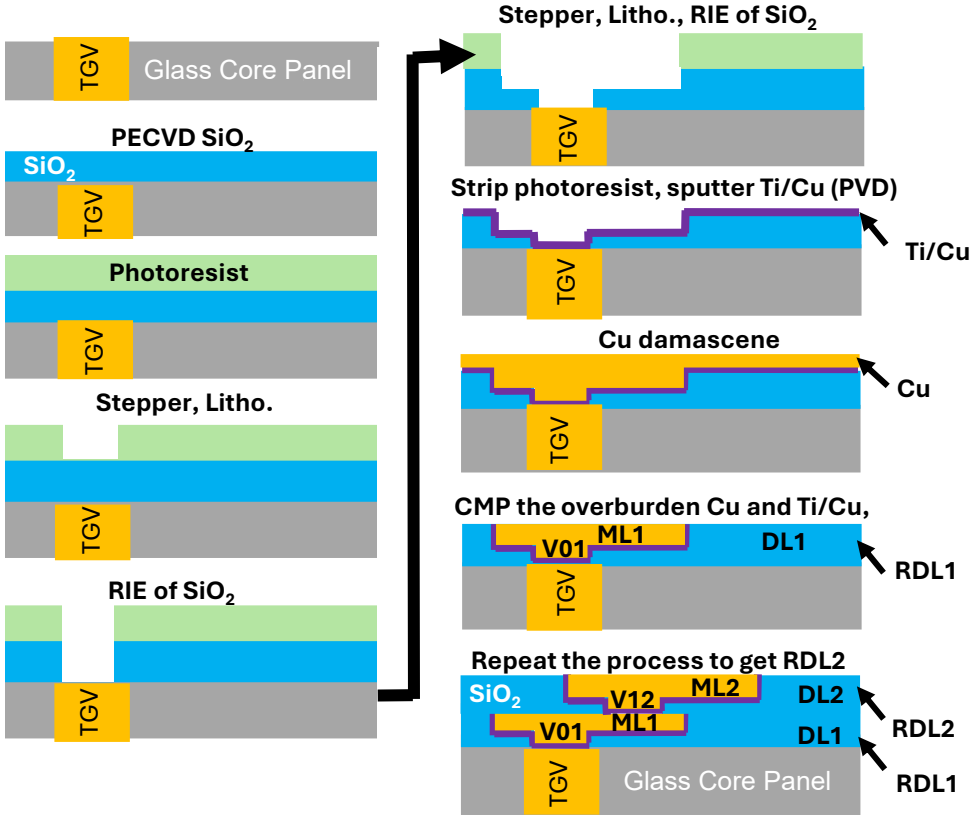
Lau, J. H., and K. N. Chiang, *Cu-Interconnects, Glass, and AI-Assisted Simulation for Chiplets Heterogeneous Integration,* (547 pages), Springer, New York, April 2026.

RDL Process Flow for (a) Glass Substrate (L/S ≥ 2μm), and (b) Glass TGV-interposer (L/S < 2μm)



(a)

- PID or ABF as dielectric layer (≦5μm)
- 10μm > L/S ≥ 2μm
- LDI or Stepper
- PVD
- ECD Cu

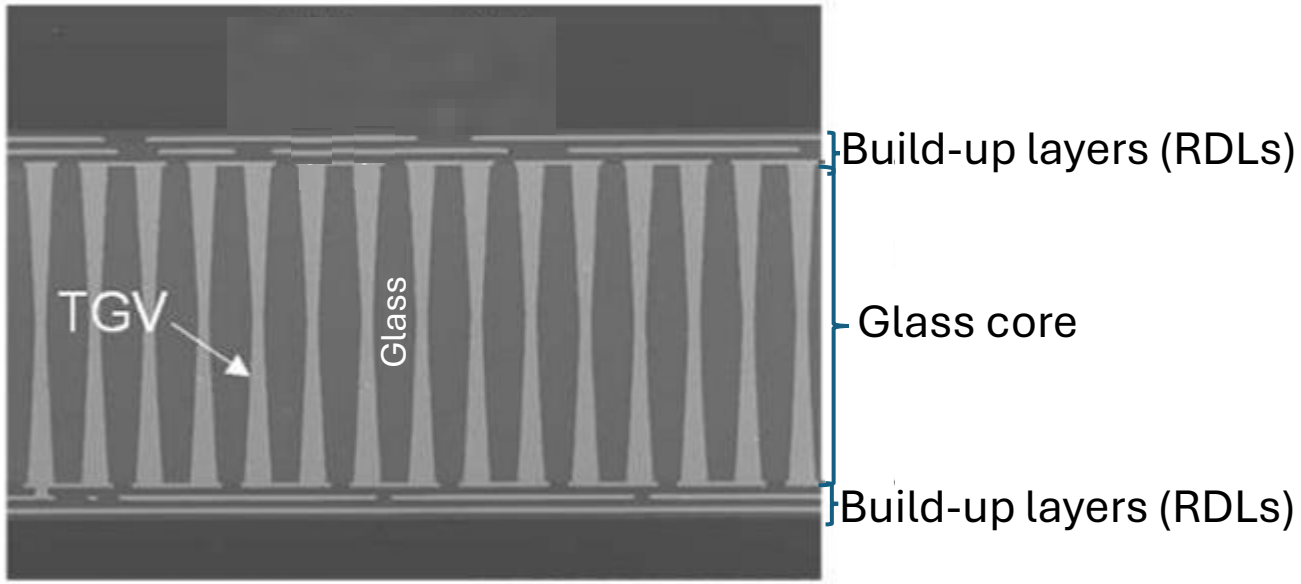


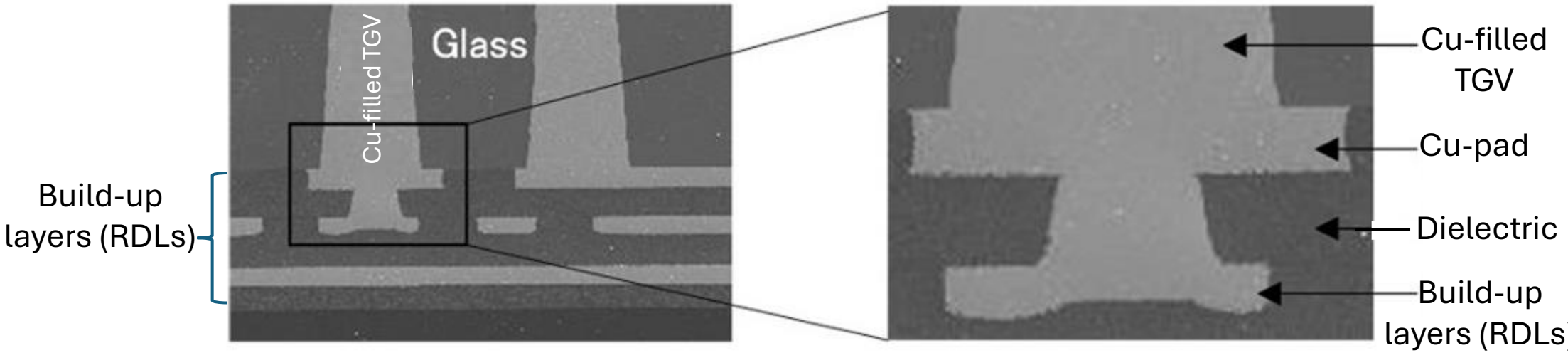
(b)

- SiO_2 as dielectric layer (~1μm)
- L/S (< 2μm), L = S = 0.2$μm_{min}$
- PECVD
- Stepper
- PVD
- Dual Cu-damascene
- CMP

Lau, J. H., and K. N. Chiang, *Cu-Interconnects, Glass, and AI-Assisted Simulation for Chiplets Heterogeneous Integration,* (547 pages), Springer, New York, April 2026.

SEM image of glass-core substrate with TGV and RDLs (build-up layers) L/S > 2μm





Lau, J. H., and K. N. Chiang, *Cu-Interconnects, Glass, and AI-Assisted Simulation for Chiplets Heterogeneous Integration,* (547 pages), Springer, New York, April 2026.

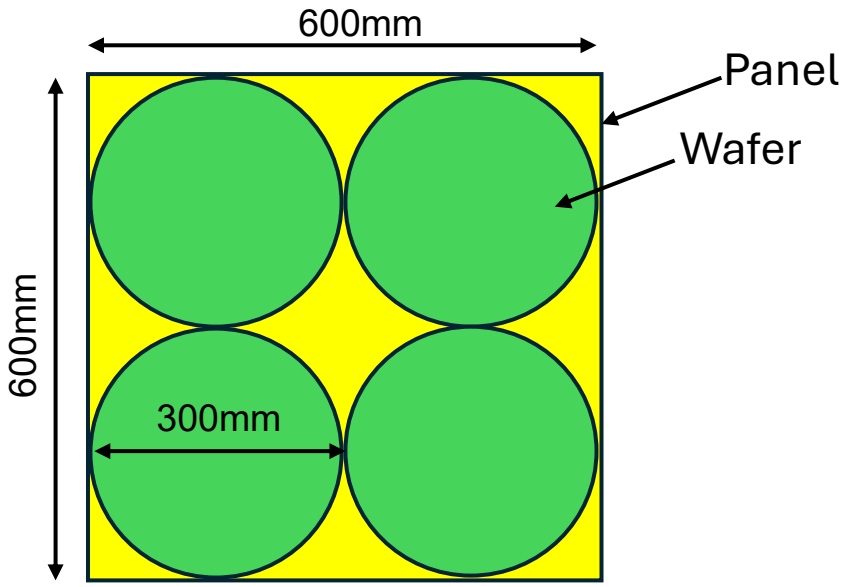
RDLs (L/S = 0.2µm$_{min}$) on Top of Glass TGV-Interposer have not been published in the literature yet!

Process Compraison between the TSV and TGV

Items	Through-Silicon Via (TSV)	Through-Glass Via (TGV)
Base Material	Silicon wafer	Alkali-free flat glass or fused silica
Via Formation	Deep Reactive-Ion Etching (DRIE)	Laser drilling / Laser Induced Deep Etching (LIDE)
Chemical Post-Processing	Gas-phase plasma etch chemistry	Anisotropic wet chemical etching (HF or NaOH)
Insulation Layer	SiO_2 (PECVD)	None - Glass is natively non-conductive
Metallization and Filling	Ti or Ta (PVD barrier layer)	Direct seed layer, e.g., Ti/Cu or electroless Cu
Sidewall Profile	Straight, vertical sidewalls.	Distinct taper angle (hourglass shape)
Via Filling	Electroplated with Cu	Electroplated with Cu
Maturity	Very	Not yet

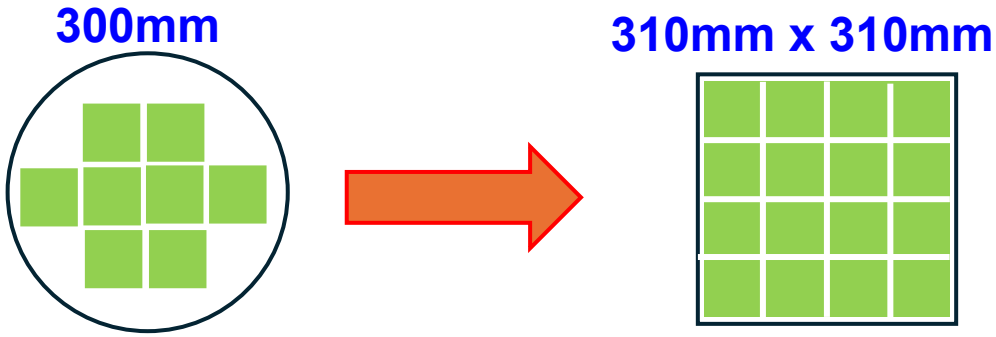
Standardization of Panel size for HPC and Data Centers in AI era

600mm x 600mm Panel vs. 310mm x 310mm Panel



Disadvantages

- More expensive equipment
- Larger floor space
- Longer Pick and Place time
- Larger warpage
- Higher yield loss
- Longer time to clean the equipment
- The large panel must be cut into smaller panels for solder ball mounted
- Etc.



- 8 Interposers
- Area Efficiency ~ 50%

- 16 Interposers
- Area Efficiency ~ 88%

Advantages

- Higher area efficiency compared with 300mm-wafer
- Similar process control as with 300mm-wafer
- Similar yield loss as with 300mm-wafer
- All the experience from 300mm-wafer can be adopted to 310mmx310mm panel

Cost! Cost! Cost!

Throughput & Processing Time Comparison: 300mm Wafer vs. 600mm x 600mm Panel

Chip Size & Format	Approximate Die Count	Pick & Place (P&P) Time	Total Time (P&P + Molding)
2mm × 2mm Chips			
300mm Wafer	~16,684 chips	100.1 minutes	115.1 minutes
600mm × 600mm Panel	~88,209 chips	529.3 minutes	544.3 minutes
3mm × 3mm Chips			
300mm Wafer	~7,328 chips	44.0 minutes	59.0 minutes
600mm × 600mm Panel	~39,204 chips	235.2 minutes	250.2 minutes
5mm × 5mm Chips			
300mm Wafer	~2,592 chips	15.6 minutes	30.6 minutes
600mm × 600mm Panel	~13,924 chips	83.5 minutes	98.5 minutes

- Speed = 10,000 Units Per Hour (UPH) (0.36 seconds per chip)
- Epoxy flow + Compression Molding time = 13 minutes
- Since the P&P time is so long for 600mm x600mm panel, the compression molding machine has to be idle for a long time

Line Balancing:
300mm Wafer vs. 600mm x 600mm Panel

	2mm x 2mm chip	3mm x 3mm chip	5mm x 5mm chip
Time to populate 1 panel (min)	529.3	235.2	83.5
Time to populate 1 wafer (min)	100.1	44	15.6
Comp. Mold. Equi. idle time (%) for Panel	94	88	78
Required Panel P&P cluster size for no idling	36	16	6

- P&P Speed = 10,000 Units Per Hour (UPH) (0.36 seconds per chip)
- Epoxy flow + Compression Molding time = 13 minutes

The Throughput Mismatch (1 P&P Machine : 1 Molding Machine)

- 2mm × 2mm Panel: (94% idle time).
- 3mm × 3mm Panel: (88% idle time).
- 5mm × 5mm Panel: (78% idle time).

How Factories Fix This: Line Balancing

For 2mm × 2mm Chips
Time to populate 1 panel: 529.3 minutes
Time to mold 1 panel: 15 minutes
Required P&P cluster size: 36 P&P machines running in parallel.
Result: Every 15 minutes, one of the 36 P&P machines finishes a panel and hands it off to the molding machine.
The molding machine never idles.

For 3mm × 3mm Chips
Time to populate 1 panel: 235.2 minutes
Time to mold 1 panel: 15 minutes
Required P&P cluster size: 16 P&P machines running in parallel.
Result: Every 15 minutes, one of the 16 P&P machines finishes a panel.

For 5mm × 5mm Chips
Time to populate 1 panel: 83.5 minutes
Time to mold 1 panel: 15 minutes
Required P&P cluster size: 6 P&P machines running in parallel.
Result: Every 15 minutes, one of the 6 P&P machines finishes a panel.

Status of Panel Size

- On April 23, 2025, TSMC announced they'll use 310mm x 310mm panel size for their CoPoS.
- In March 2026, while ASE originally planned for a 600mm x 600mm panel line, it scaled back to 310mm x 310mm to align with TSMC's panel size. ASE aims to have a fully automated 310mm x 310mm production line operational for pilot production by the end of 2026.
- On May 26, 2026, ASE formally announced the 310mm x 310mm panel size by the CEO (Dr. Tien Wu) of ASE at ECTC2026. Most of the successful experiences from 300mm wafer can be transferred to 310mm x 310mm.
- With the #1 foundry (TSMC) and the #1 OSAT (ASE) now aligned, the market is poised to shift from experimentation to volume production.
- Standardizing this panel size 310mm x 310mm is expected to help the entire semiconductor ecosystem scale AI chip packaging more reliably by providing a common platform for testing and manufacturing.
- I do think that 310mm × 310 mm format strikes a critical balance: it is large enough to capture the area efficiency (cost) and small enough to maintain the processing control (yield). All the experience from 300mm-wafer can be adapted to 310mm x 310mm panel.

ASE's 310mm x 310mm

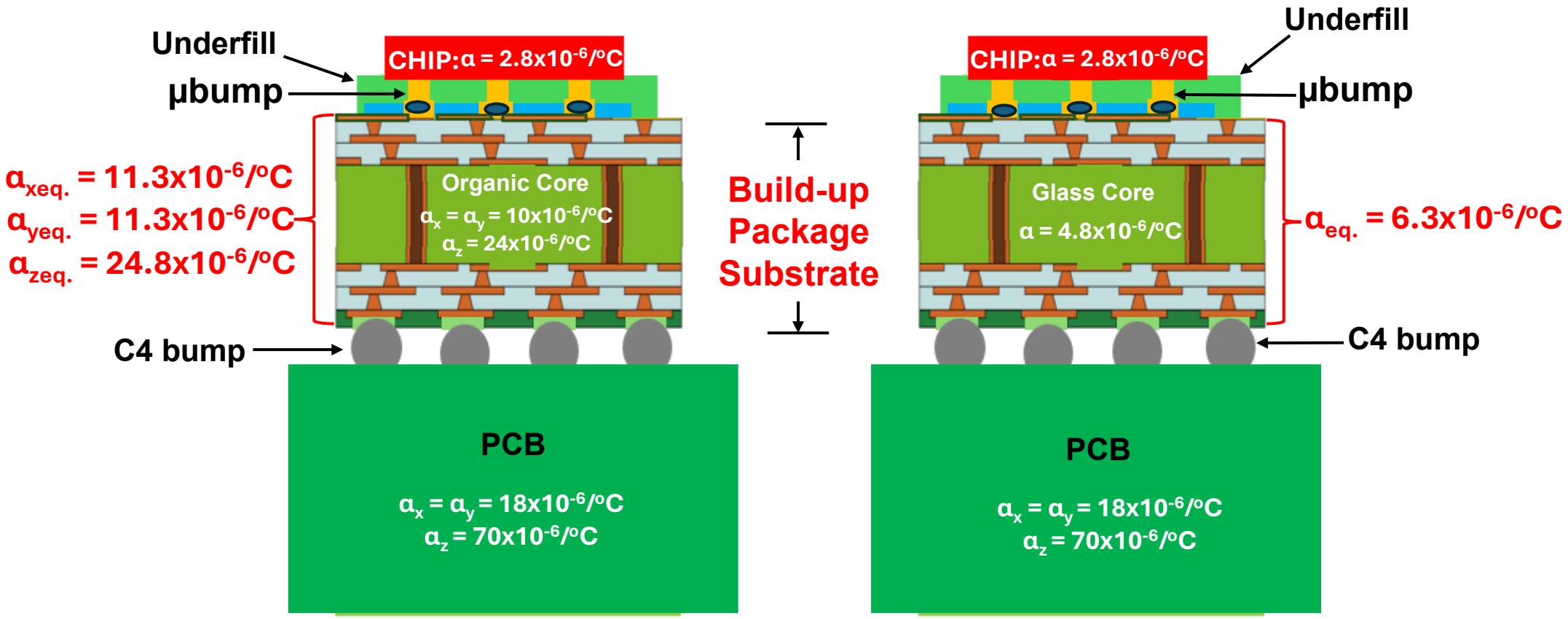


Flip Chip on Glass-core Substrate with µbumps

(Effects of glass-core substrate on Solder Joint Reliability)

Lau, J. H., N. Liu, M. Ma, and T. Tseng, "Flip Chip on Glass-Core Substrates with Microbump and Cu-Cu Hybrid Bonding", *Journal of Microelectronic Packaging*, Vol. 22, Issue 3, September 2025, pp. 44-60.

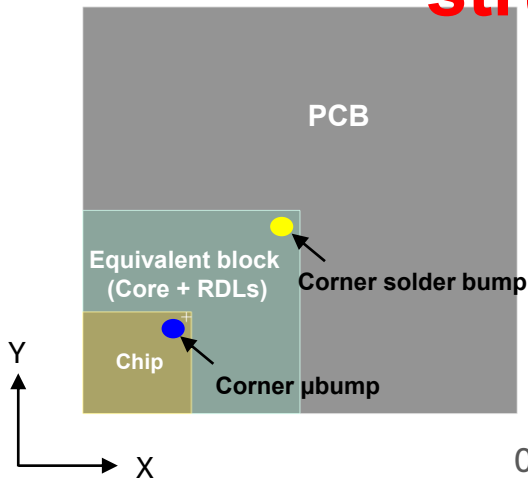
Flip Chip (a) on organic-core substrate, and (b) on glass-core substrate

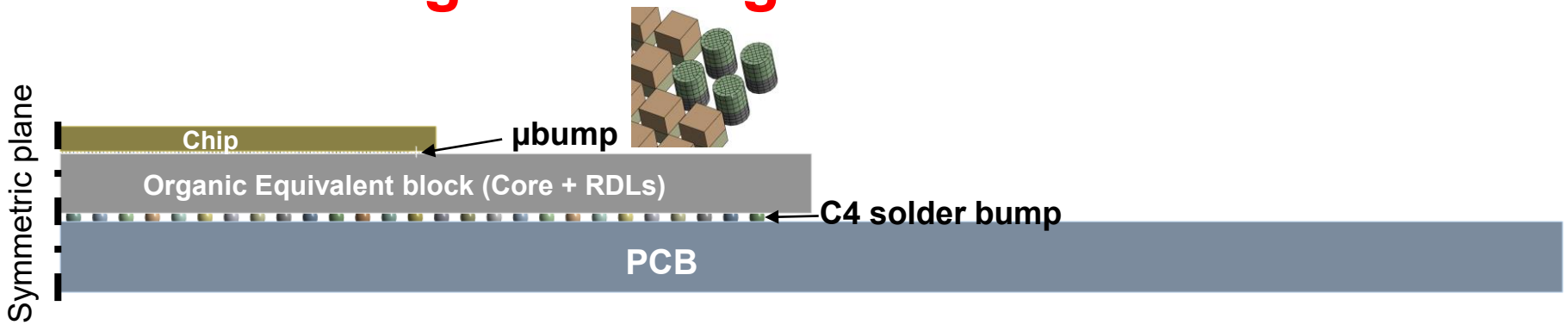


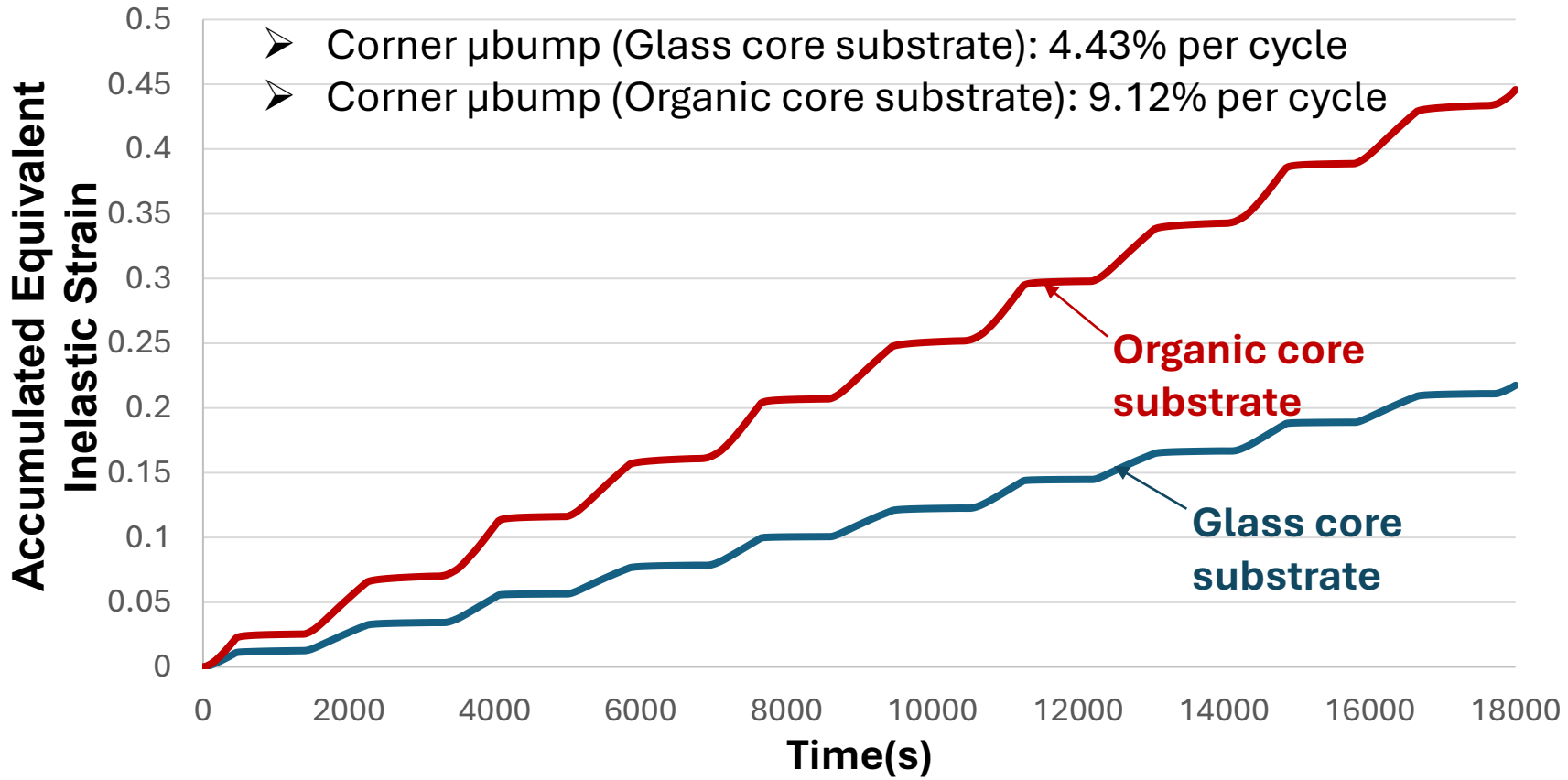
The chip dimensions are 10mm x 10mm x 350μm. The C4 bump is SAC. The μbump is Cu-pillar + Sn0.7Cu. Both solders obeyed Anand model. Build-up layers (RDLs) = 2 layers on top and 2 layers at the bottom. The thickness of each layer is 8μm (Cu metal layer = 3μm and dielectric layer = 5μm). The thickness of the glass core and organic core is 800μm. The thickness of the PCB = 1.57mm.

Lau, J. H., N. Liu, M. Ma, T. Tseng, "Solder joint reliability - glass core substrate versus organic core substrate", *Journal of Microelectronic Reliability*, Vol. 168, May 2025, pp. 115701.

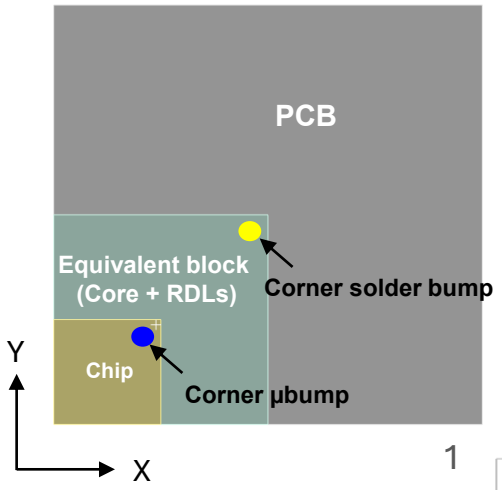
Maximum accumulated inelastic strain time-history in corner μbump of structures with organic and glass substrates

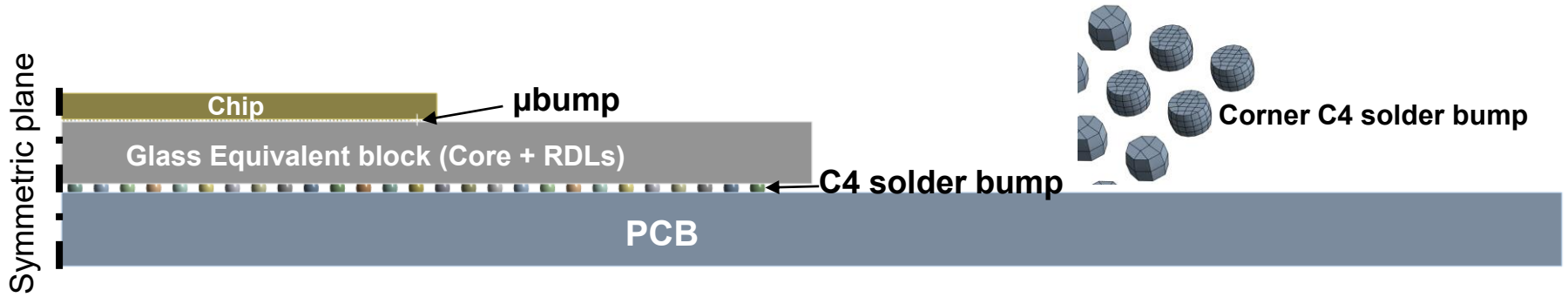


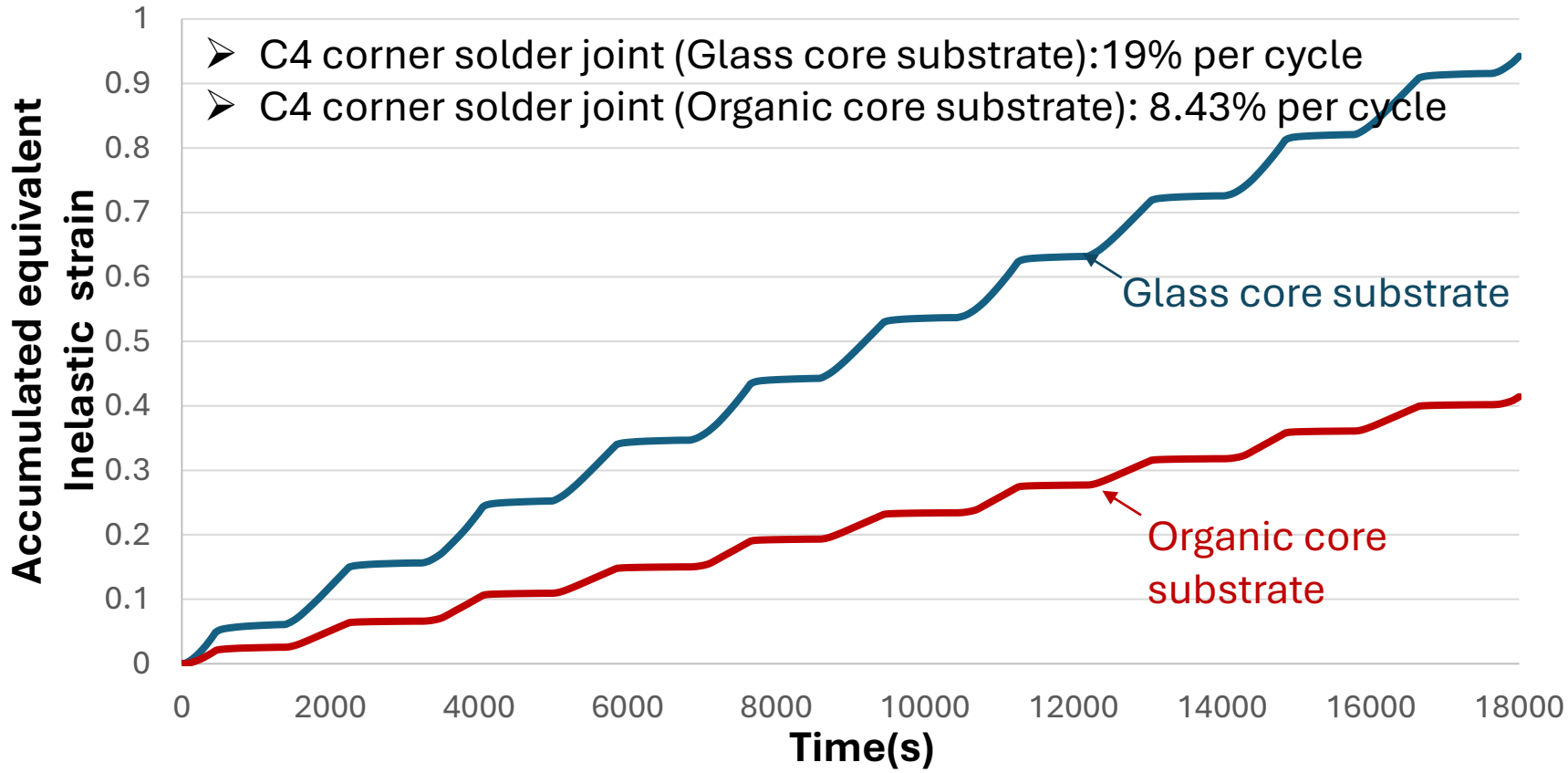




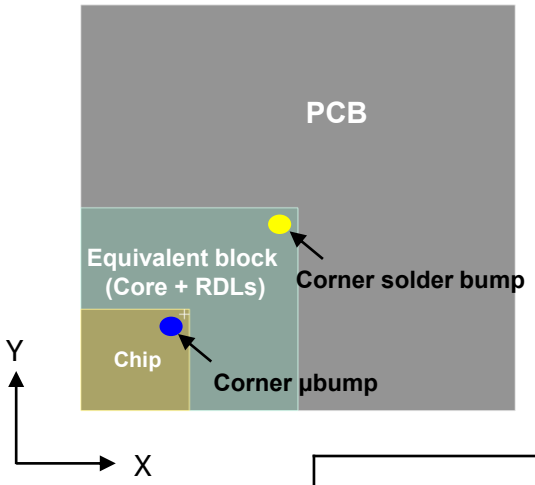
Maximum accumulated inelastic strain time-history in corner C4 solder joint of structures with organic and glass substrates

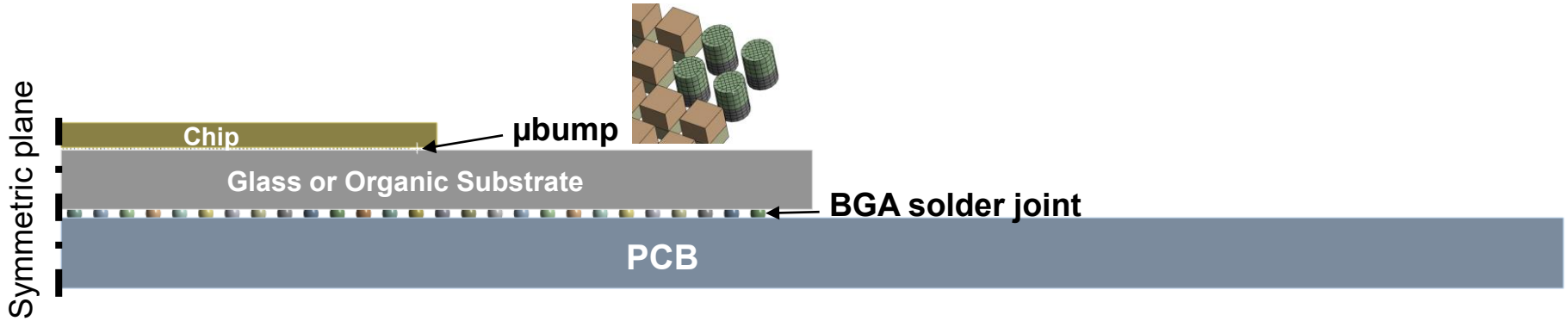






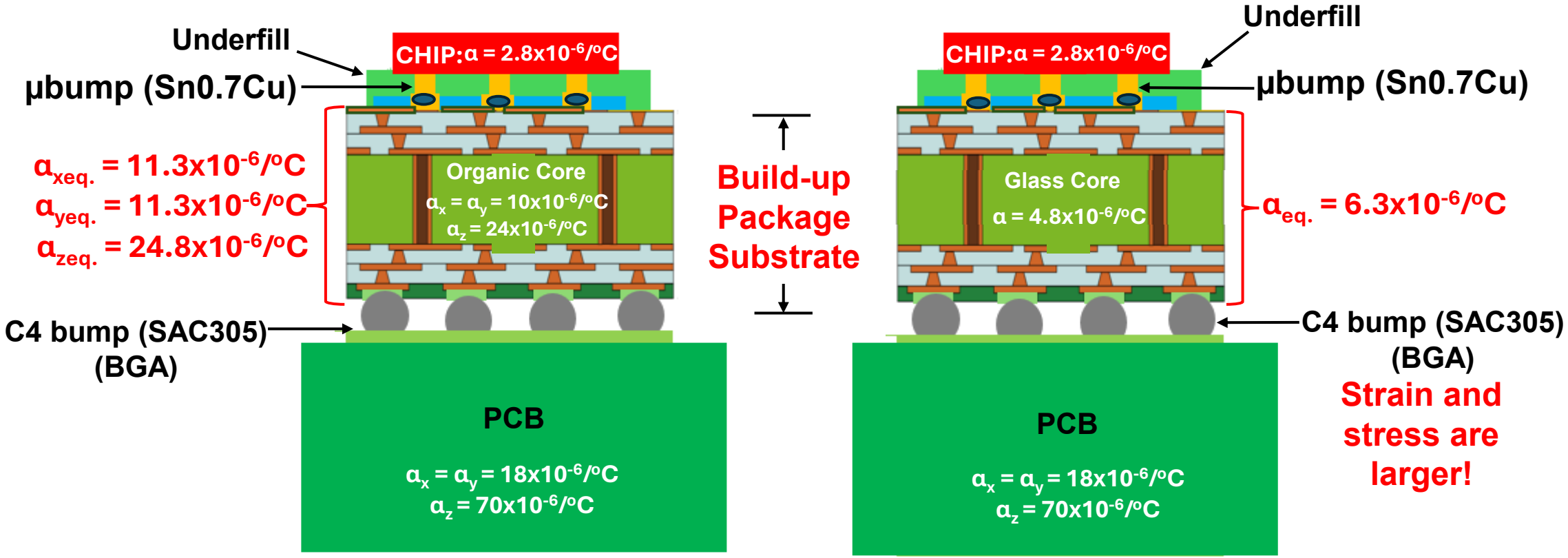
Max Accumulated equivalent inelastic strain: Glass-core Substrate vs. Organic-core Substrate





Interconnect Type	Organic Core Substrate (Max accumulated equivalent inelastic strain)	Glass Core Substrate (Max accumulated equivalent inelastic strain)	Technical Consequence / Status
Corner µbump Solder Joint with underfill	9.12% per cycle	4.43% per cycle	Low risk: Both are protected by underfill
Corner BGA Solder Joint without underfill	8.43% per cycle	19.0% per cycle	High risk: Glass core introduces more than doubles the inelastic strain on the PCB side where no underfill is presented

C4 Solder Joint Reliability: Glass core vs. Organic Core



SUMMARY

As a matter of fact, the CTE of the glass substrate should be closer to the PCB CTE. Say $10x10^{-6}/^{o}C$

.

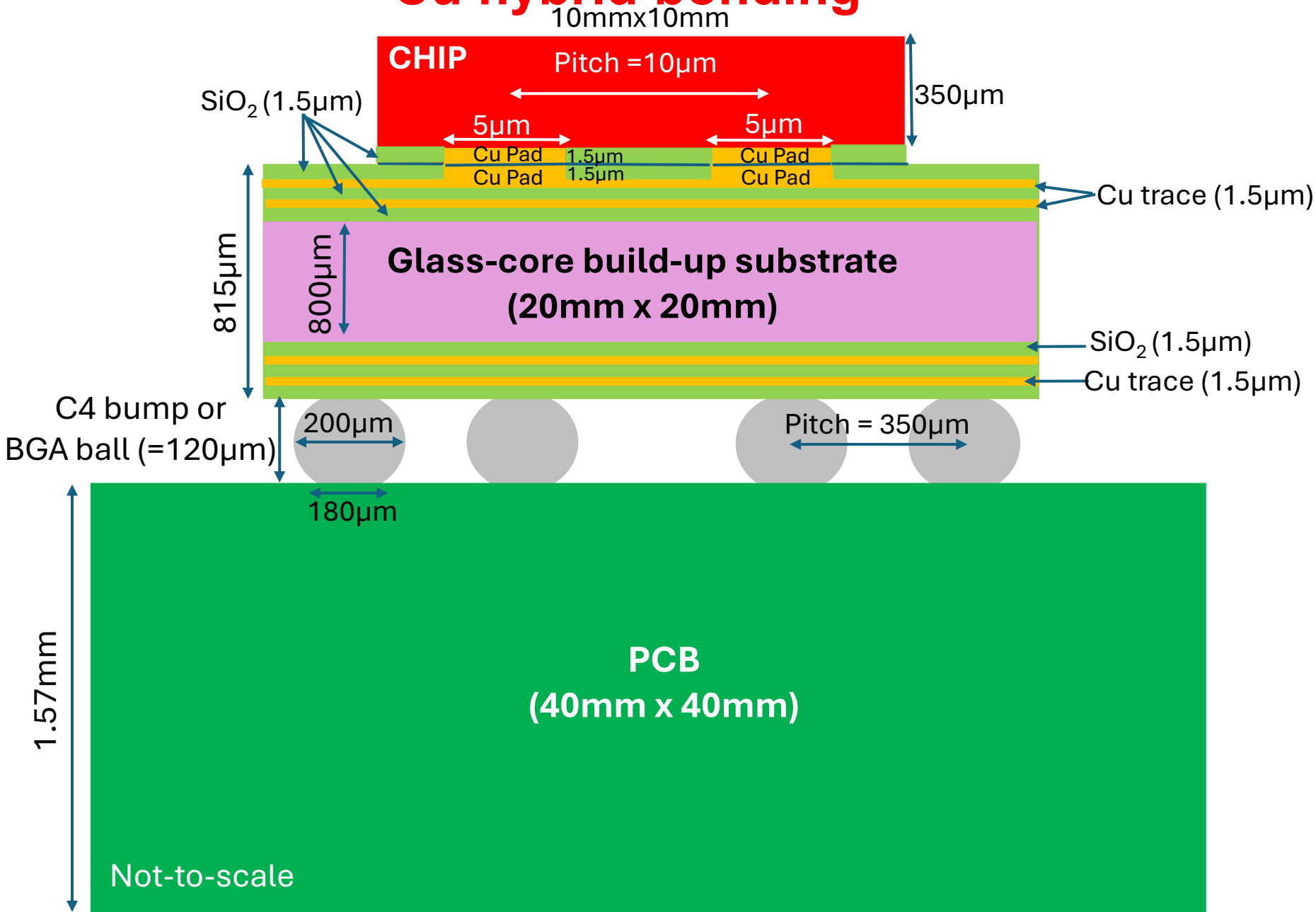
Because there is underfill protection of the µbump solder joint on the glass substrate but there is no underfill protection for the C4 or BGA solder joints on the PCB.

Especially for larger glass package substrates, especially housing the one trillion transistors..

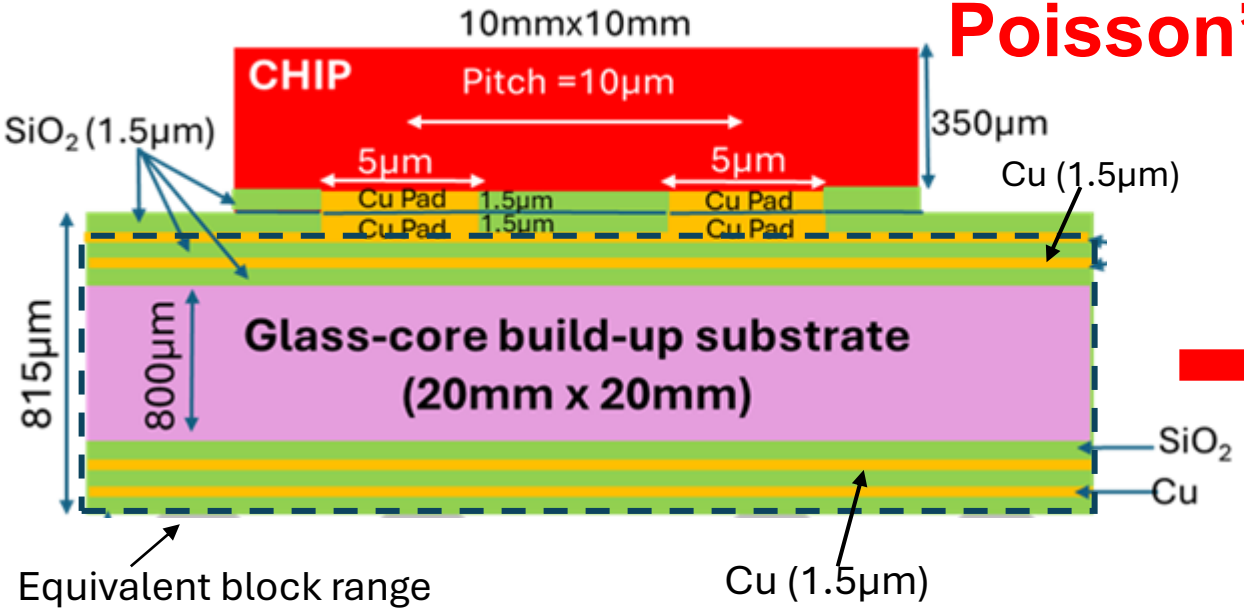
Flip Chip on Glass-core Substrate with Cu-Cu Hybrid Bonding

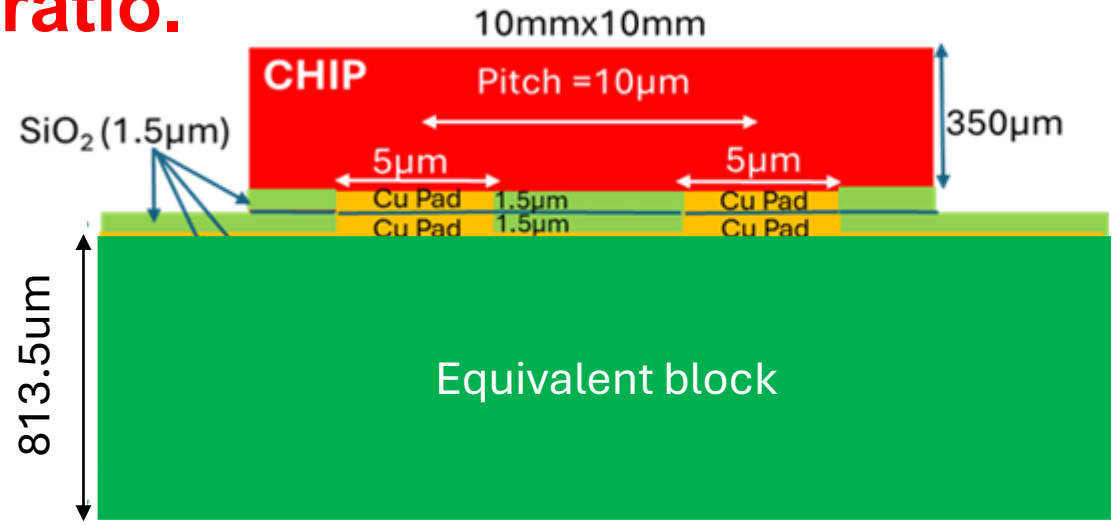
(Effects of glass-core substrate on Solder Joint Reliability)

Cross section of flip chip on glass-core substrate with bumpless Cu-Cu hybrid bonding



Equivalent Young's modulus, equivalent CTE, and equivalent Poisson's ratio.





☐ **For Equivalent Young's modulus: 70.3GPa**

$$\frac{121\times(1.5*4)+70\times(1.5*5)+72*800}{(1.5*4)+(1.5*5)+800} = 70.3\text{GPa}$$

☐ **For Equivalent Poisson's ratio: 0.29**

$$\frac{0.34\times(1.5*4)+0.17\times(1.5*5)+0.29\times800}{(1.5*4)+(1.5*5)+800} = 0.29$$

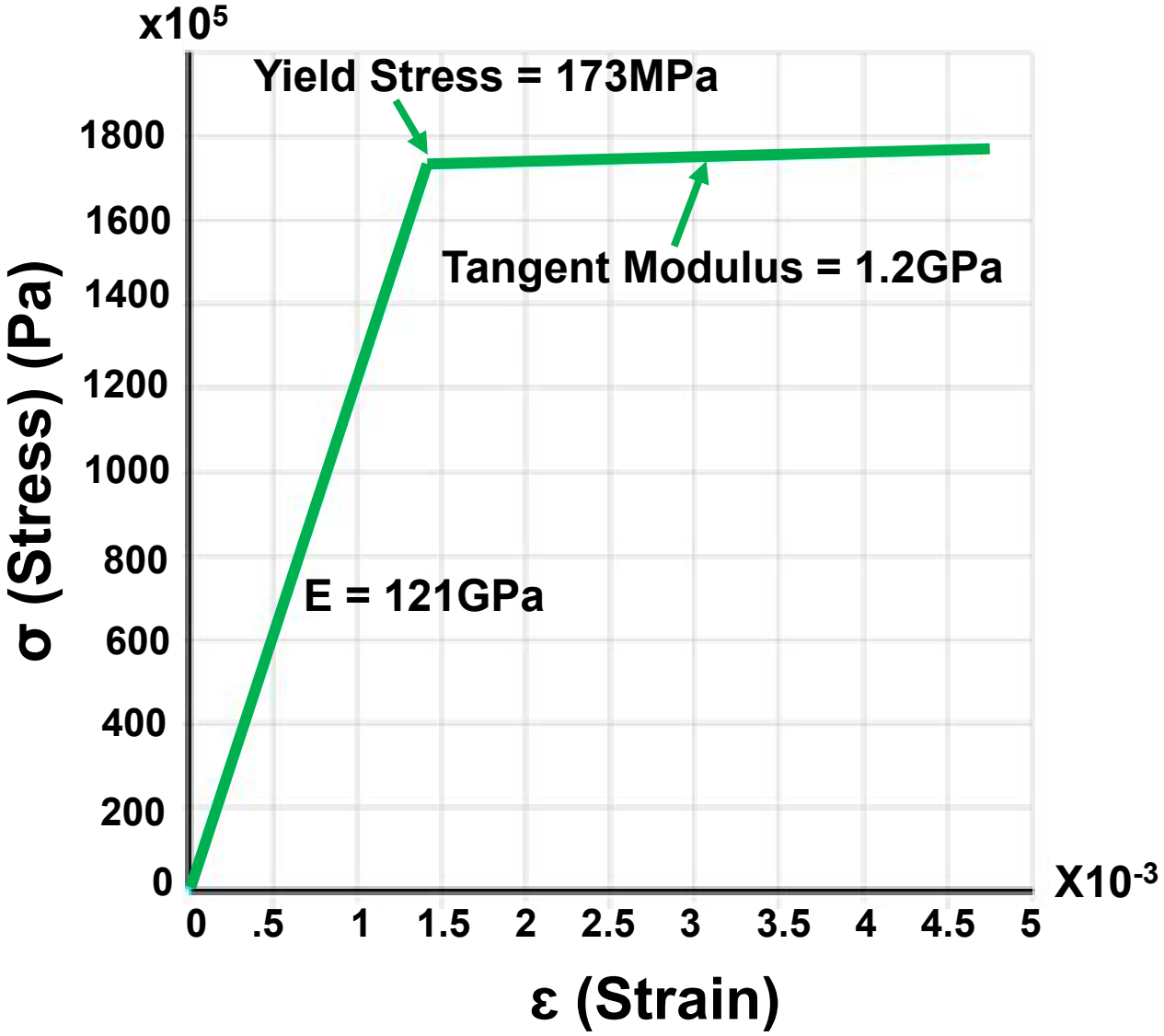
☐ **For Equivalent CTE (Glass = 4.8): 4.85x10^{-6}/°C**

$$\frac{16.3\times(1.5*4)+0.5\times(1.5*4)+4.8\times800}{(1.5*4)+(1.5*5)+800} = 4.85\text{x}10^{-6}/^{\circ}\text{C}$$

☐ **For Equivalent CTE (Glass = 10): 9.96x10^{-6}/°C**

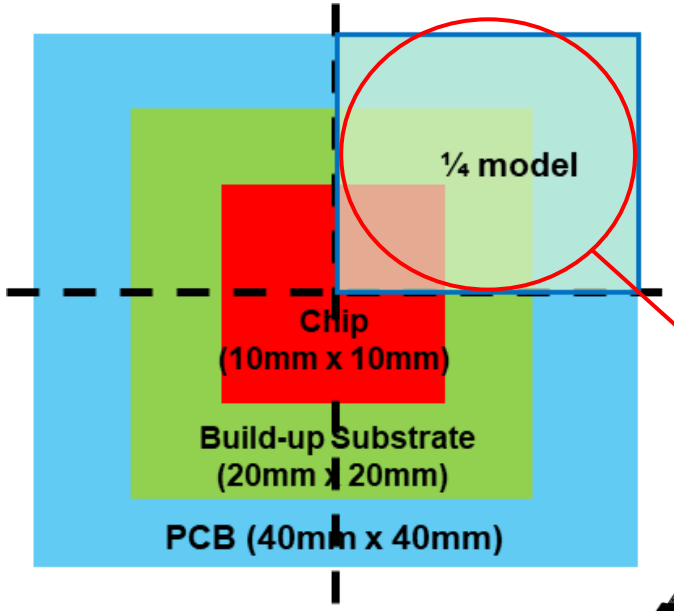
$$\frac{16.3\times(1.5*4)+0.5\times(1.5*4)+10\times800}{(1.5*4)+(1.5*5)+800} = 9.96\text{x}10^{-6}/^{\circ}\text{C}$$

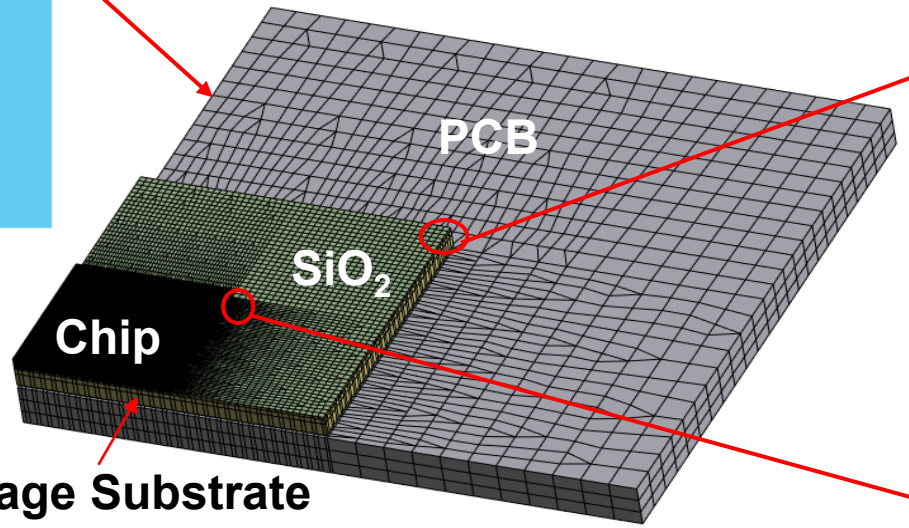
Elastoplastic of dual-damascene copper



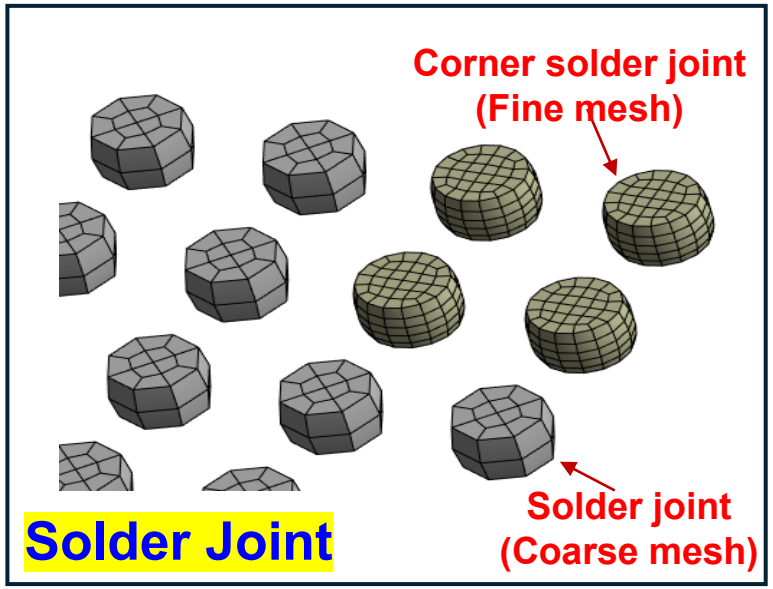
- Consider copper Bauschinger effect, Kinematic hardening is used in this material.

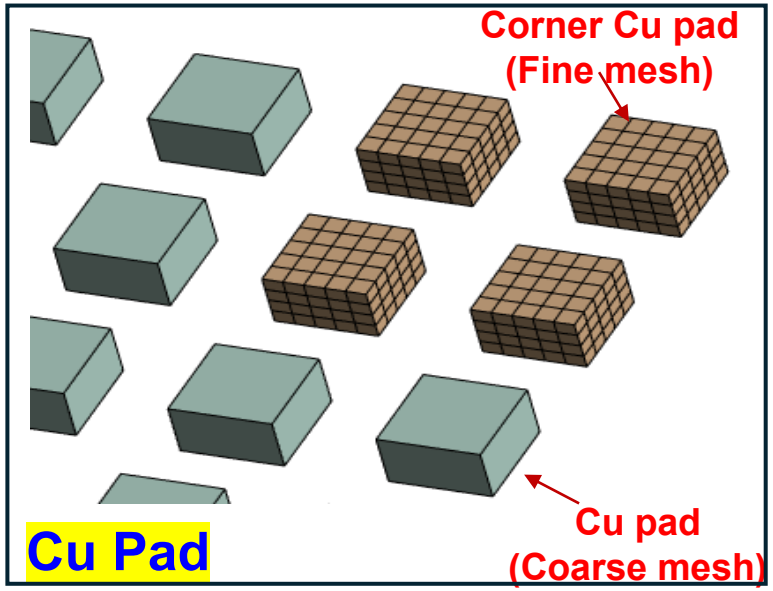
Finite element modeling of flip chip on glass-core substrate with Cu-Cu hybrid bonding



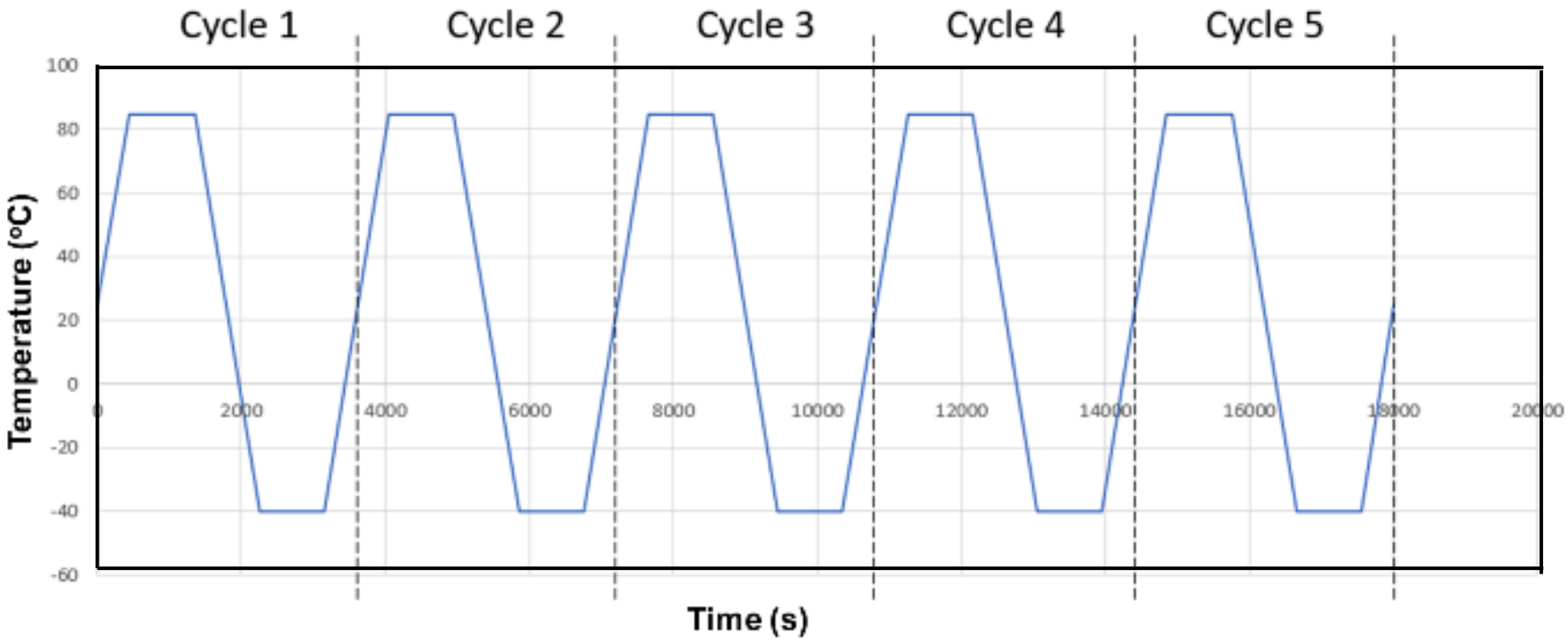


Package Substrate
(Equivalent block)



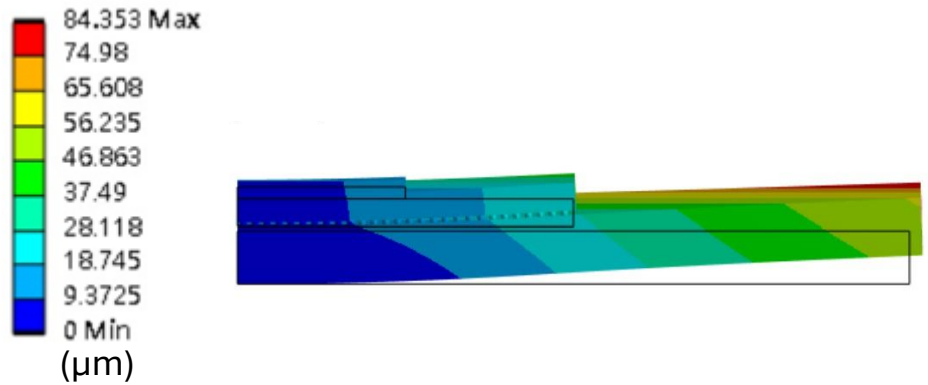


Thermal cycling boundary condition

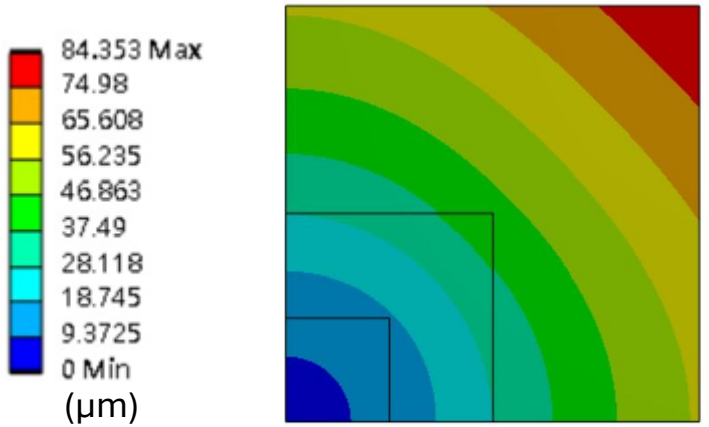


Deformation of structure with organic-core substrate.

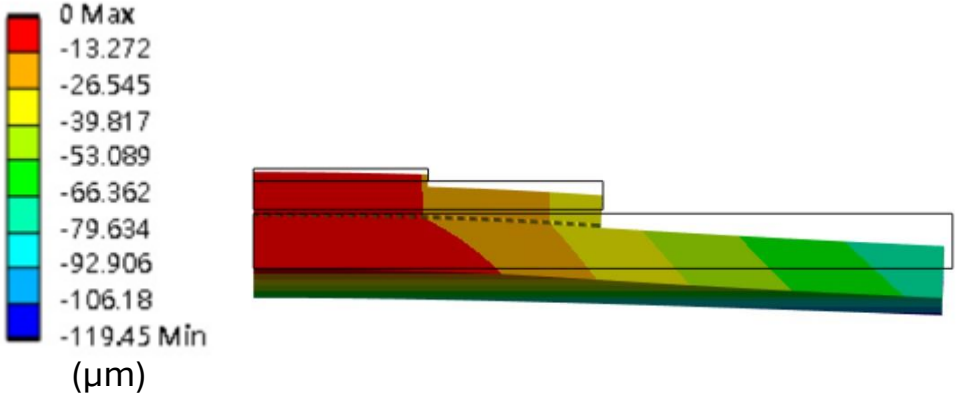
85^{O}C (450s)_Side view



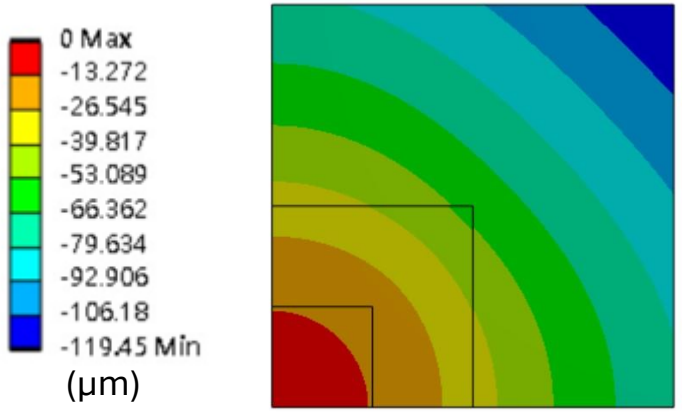
85^{O}C (450s)_Top view



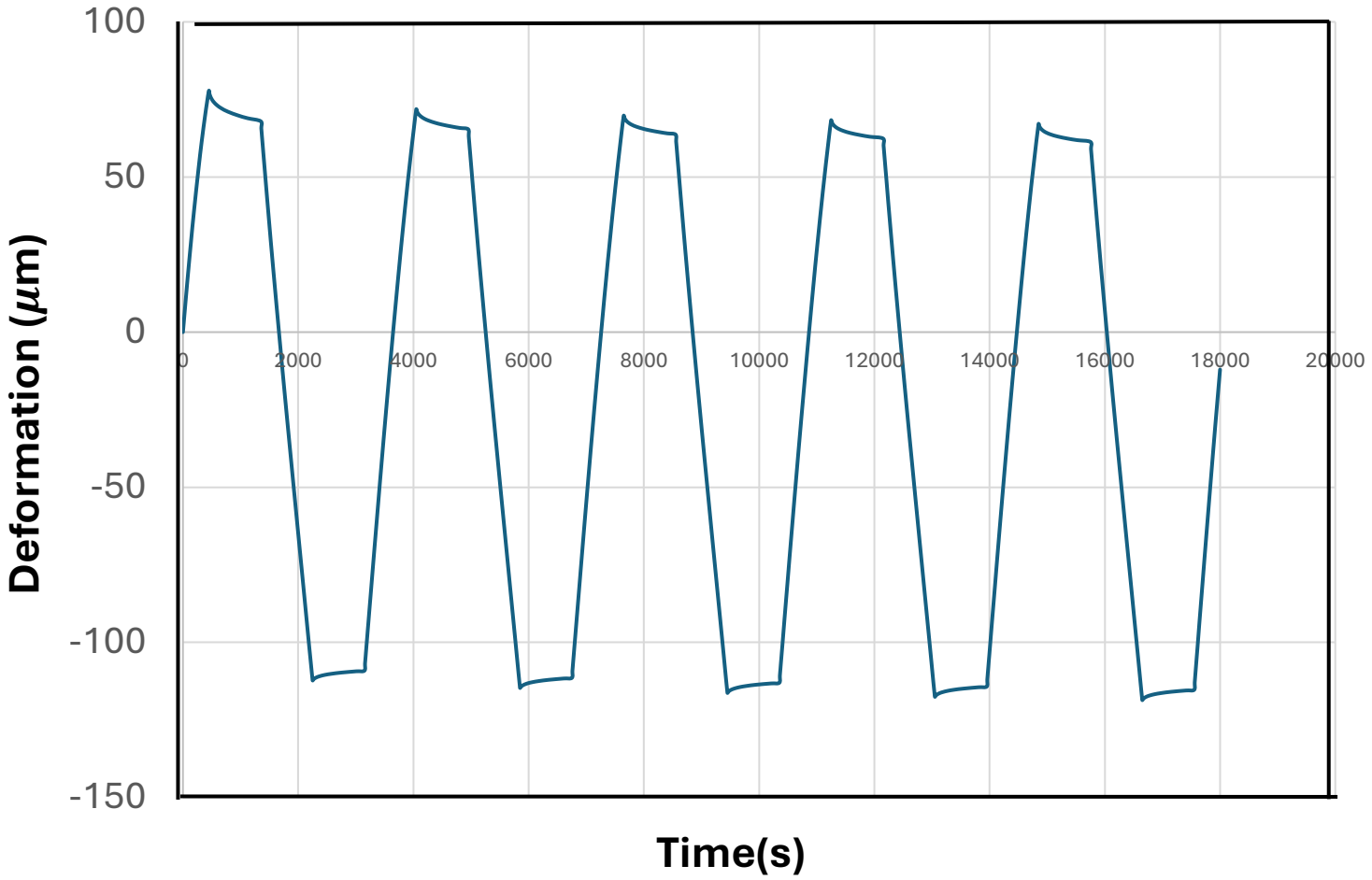
-40^{O}C (2250s)_Side view



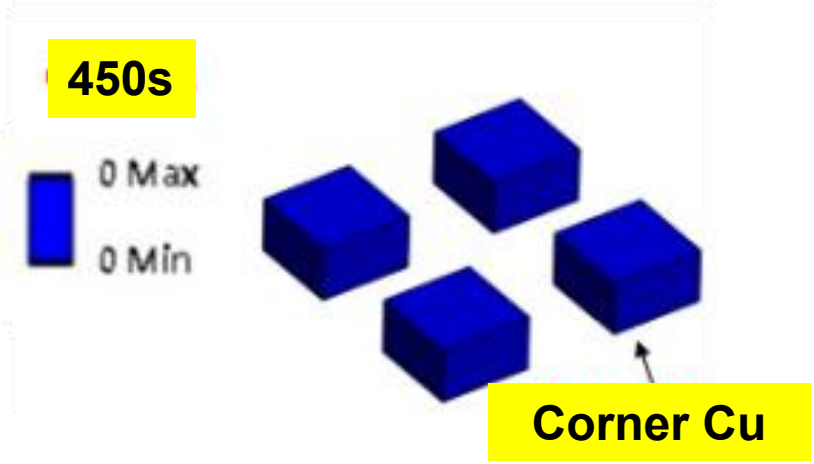
-40^{O}C (2250s)_ Top view

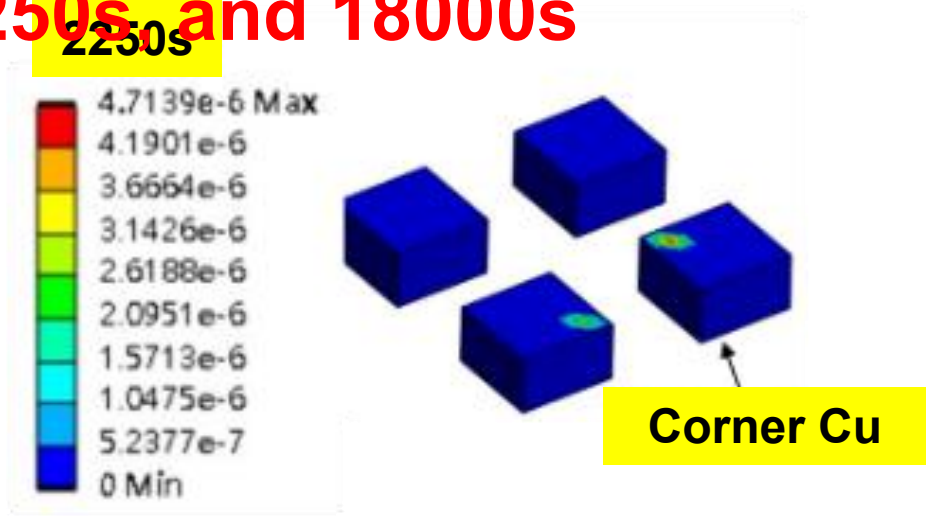


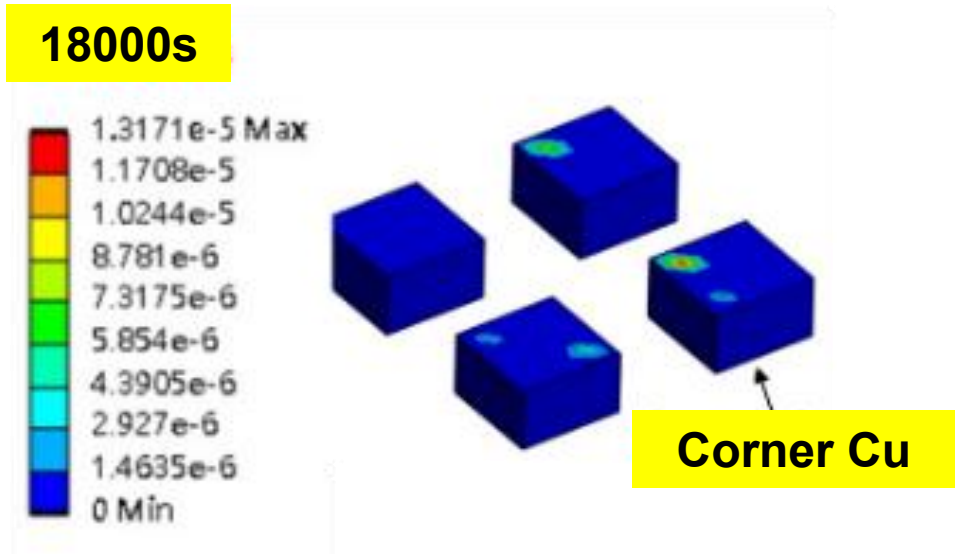
Time-history deformation of the structure



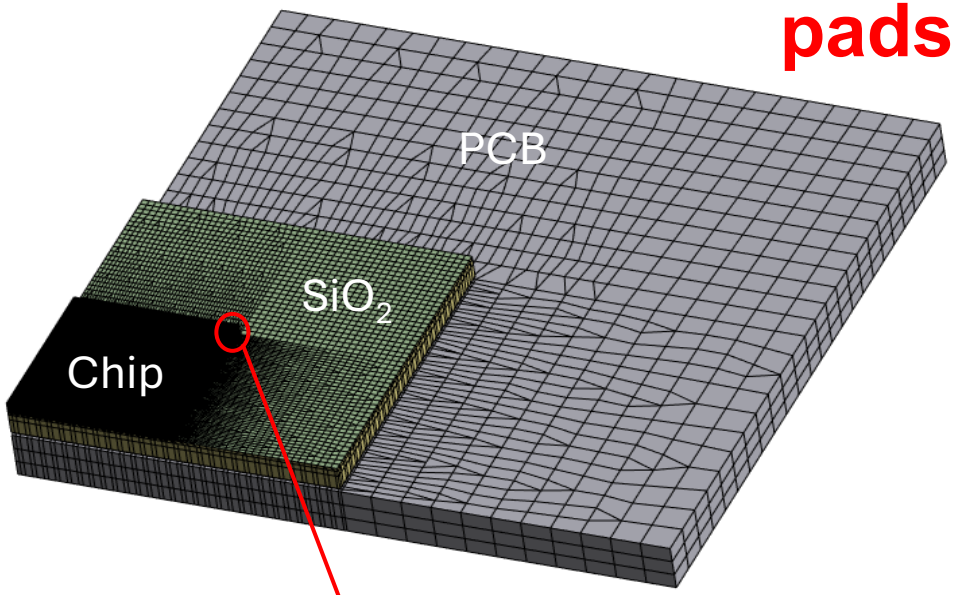
Accumulated equivalent inelastic strain contours at the corner Cu-pads at 450s, 2250s, and 18000s

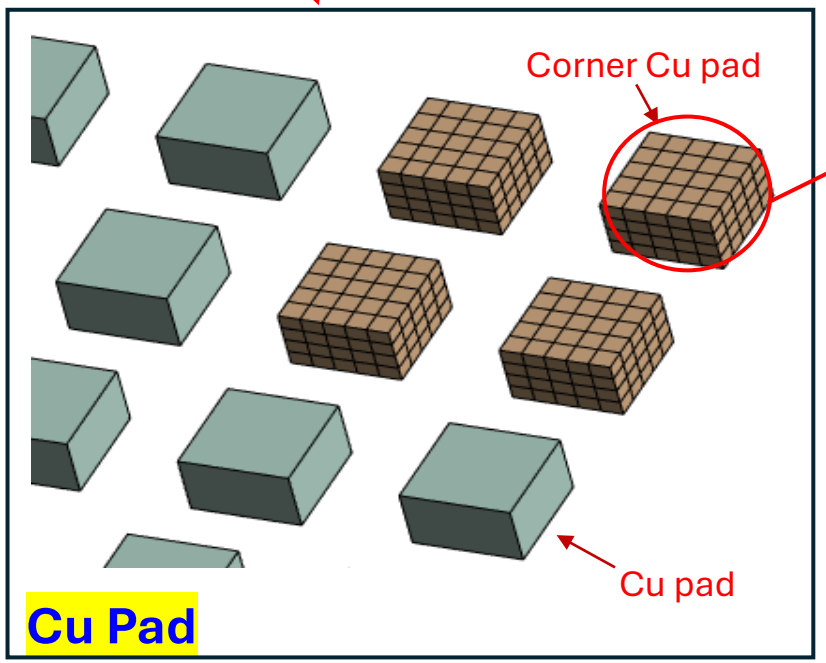




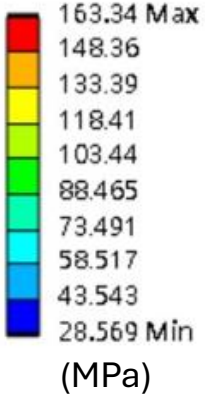


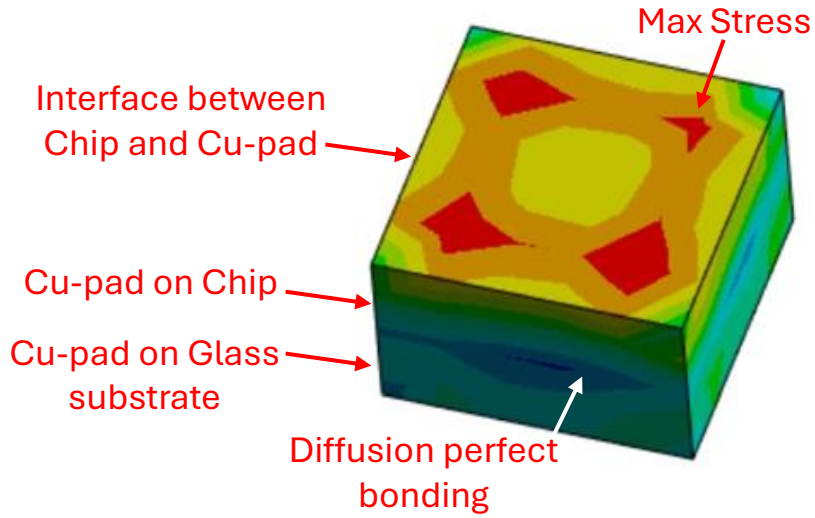
Accumulated equivalent (von Mises) stress contours at the corner Cu-pads at 450s and 2250s.



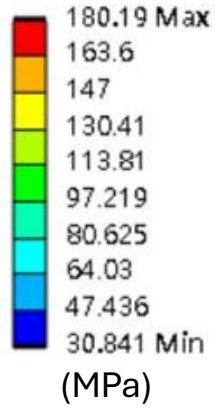


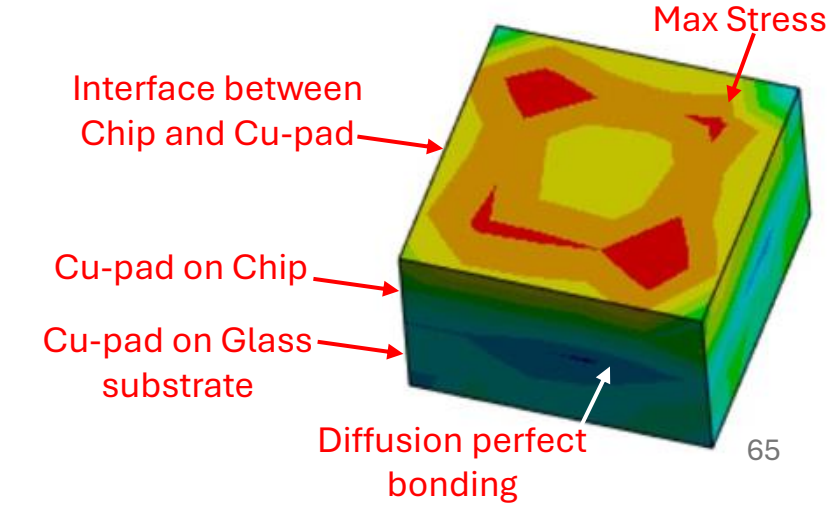
85^{O}C (450s)



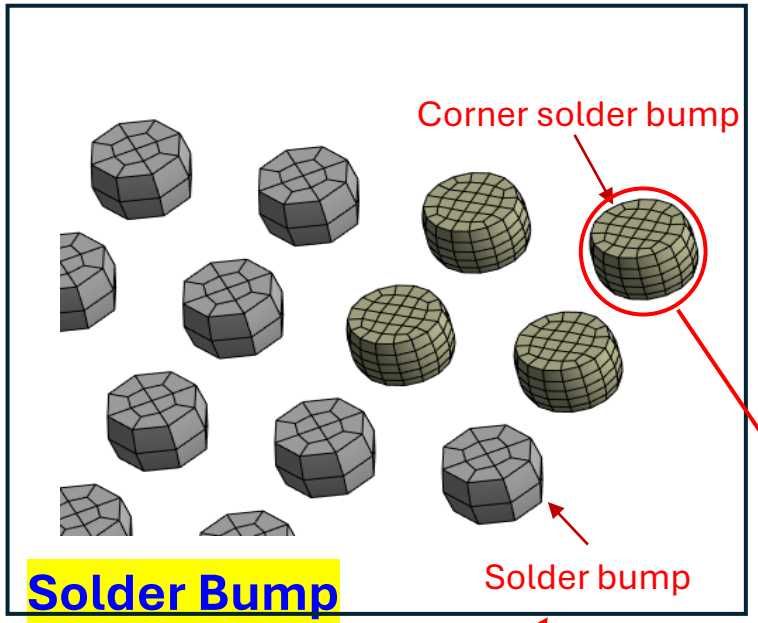


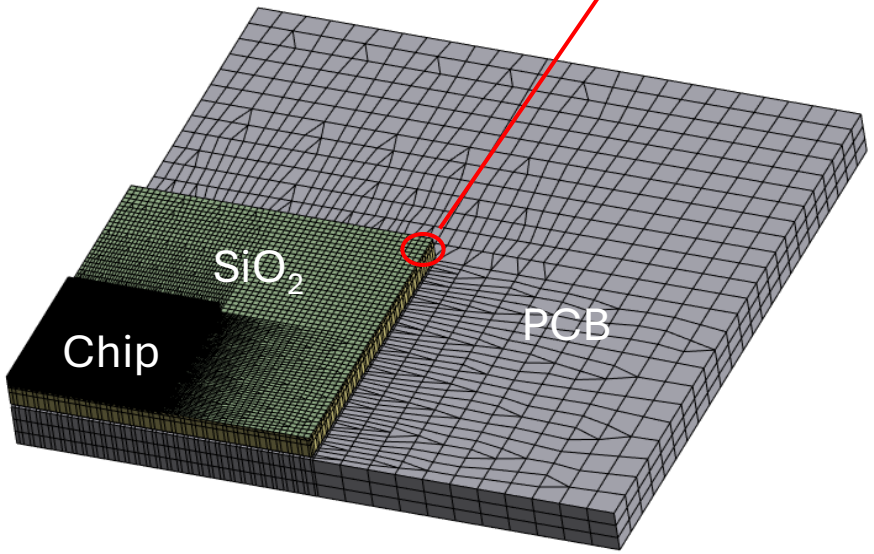
-40^{O}C (2250s)

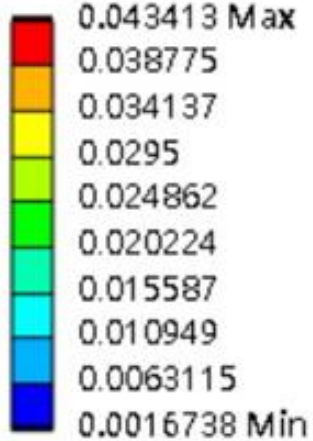




Accumulated equivalent inelastic strain contours at the corner solder ball at 450s and 2250s

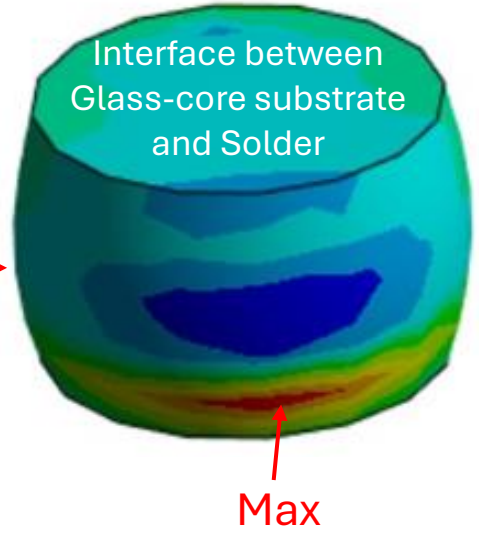


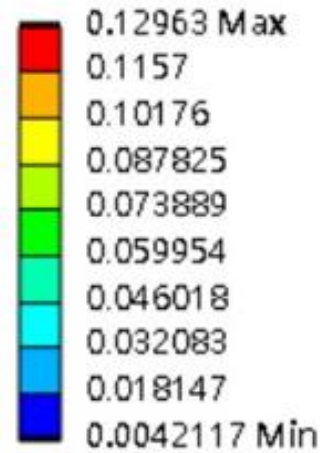




85^{O}C (450s)

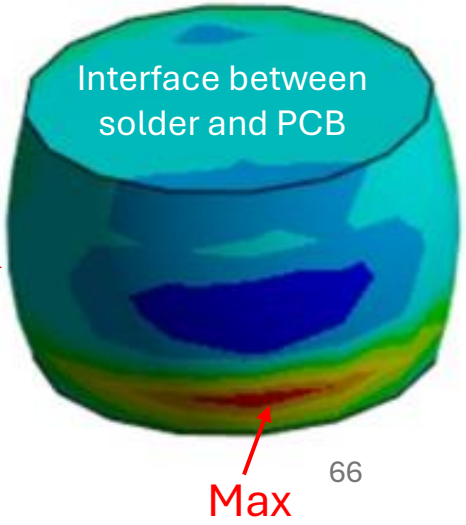
C4 Bump or Solder Ball →



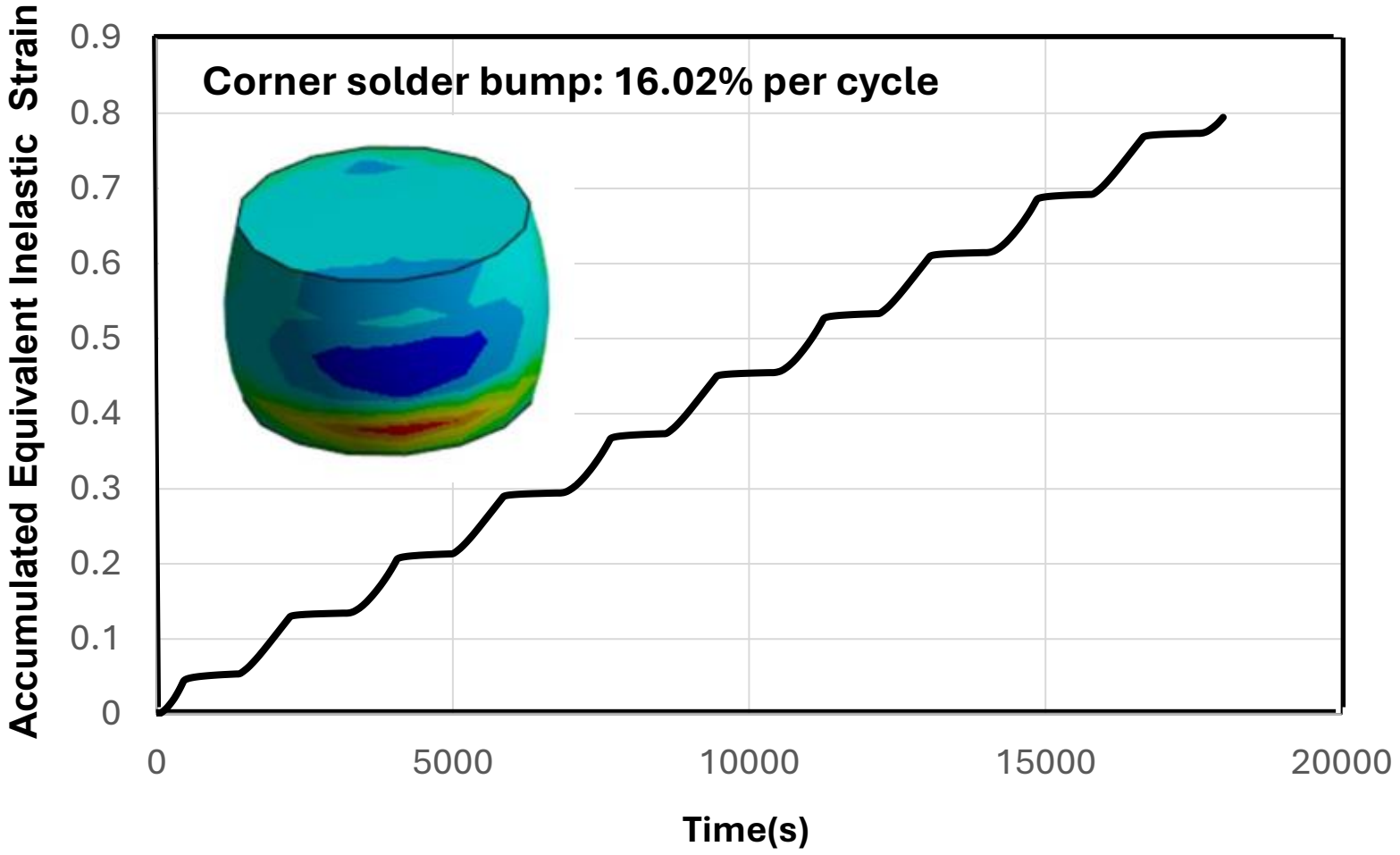


-40^{O}C (2250s)

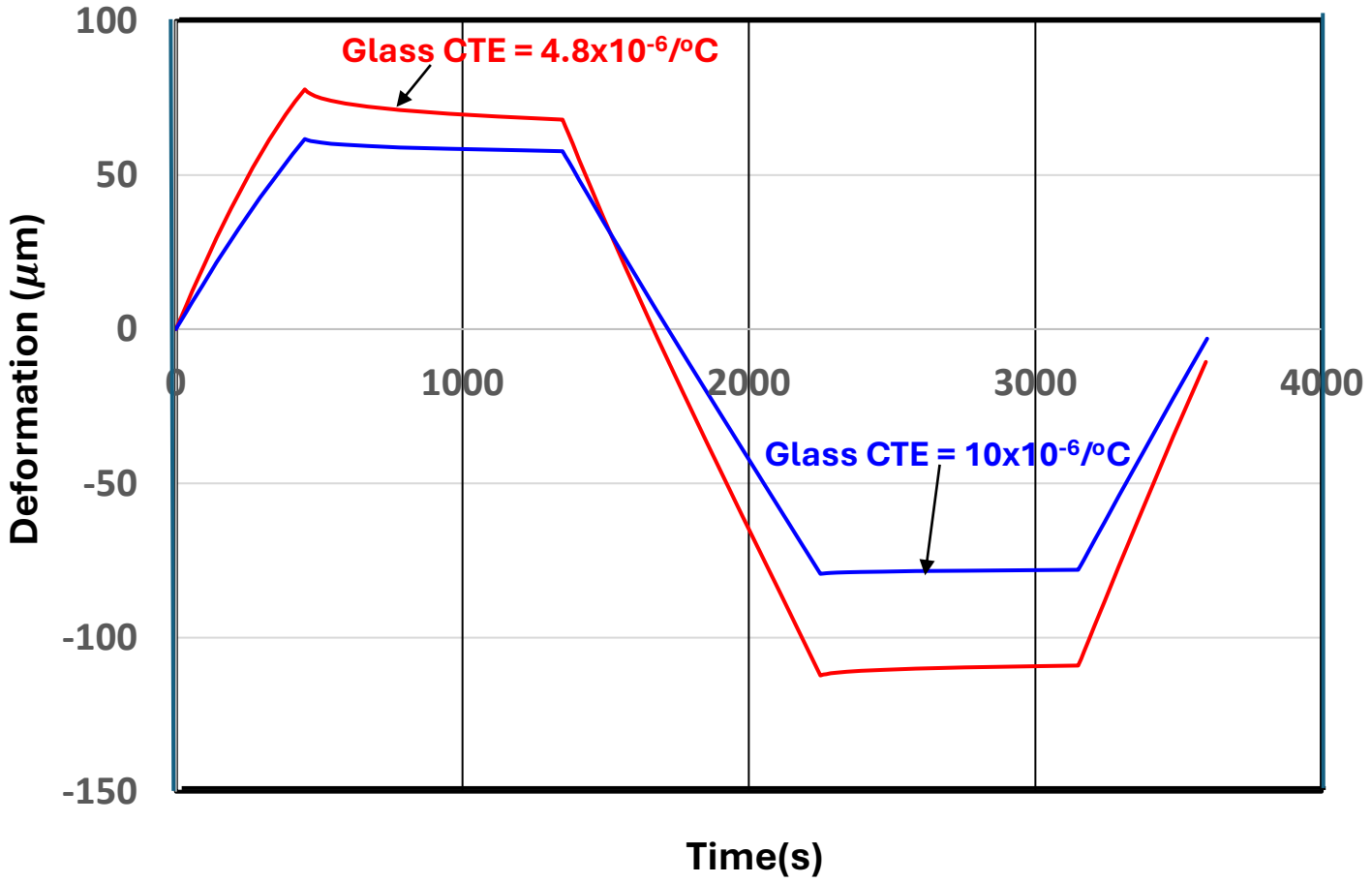
C4 Bump or Solder Ball →



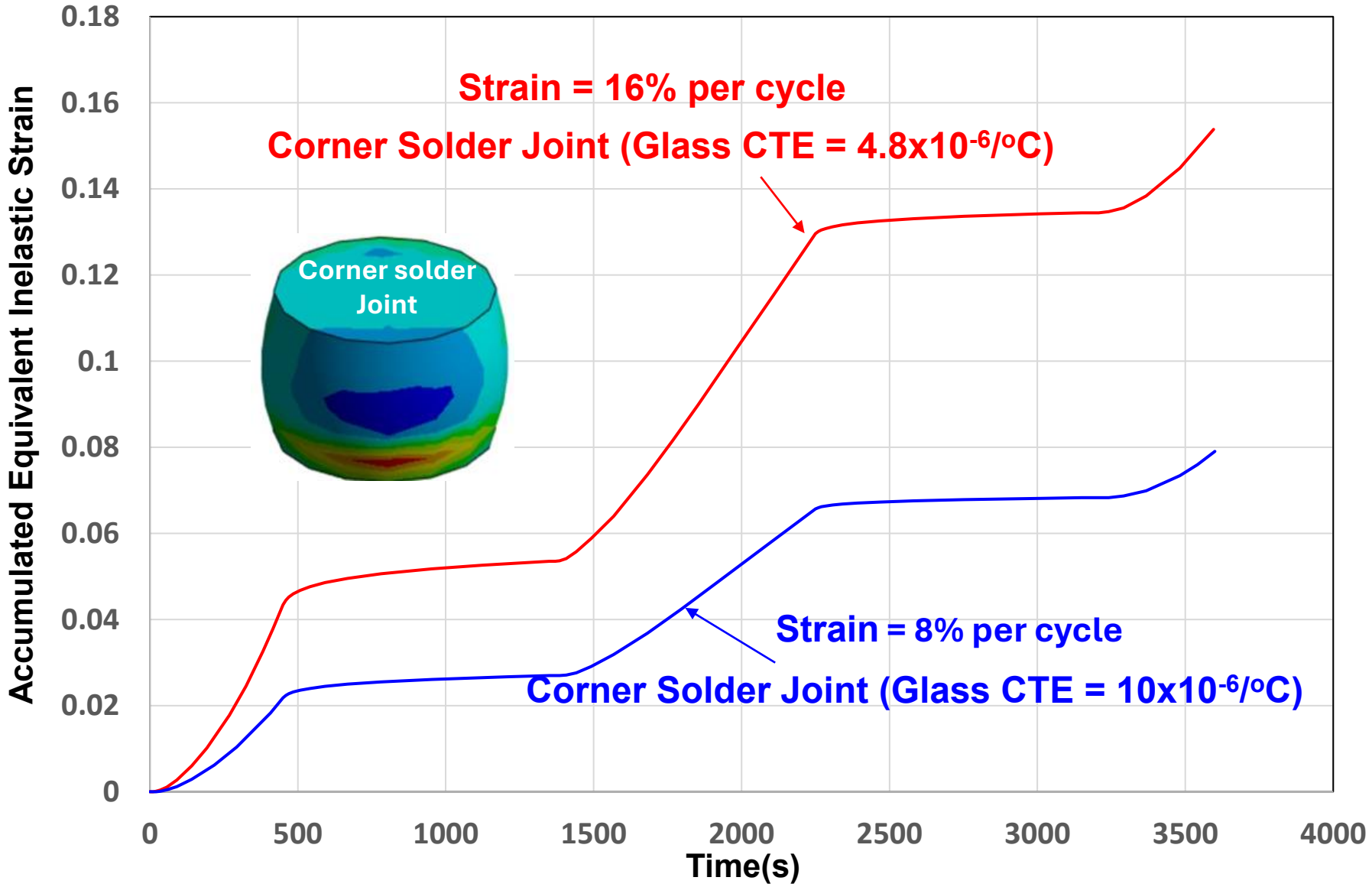
Time-history accumulated equivalent inelastic strain at the corner solder ball



Warpage for glass-core substrate with CTE = 4.8x10^{-6}/^{o}C and 10x10^{-6}/^{o}C



Accumulated equivalent inelastic strain at the corner solder joint (CTE = $4.8 \times 10^{-6}/^{o}C$ and $10 \times 10^{-6}/^{o}C$).

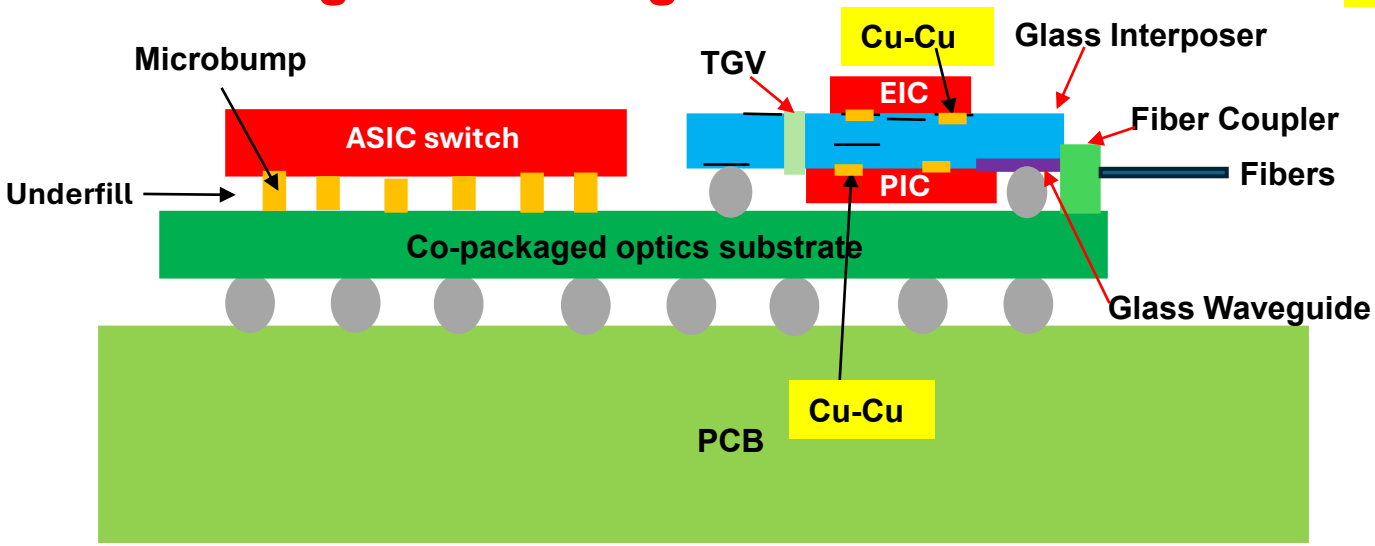


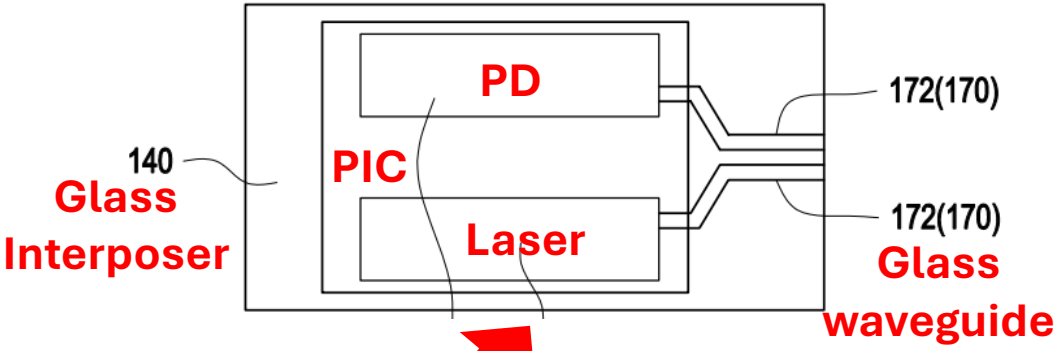
RECOMMENDATION

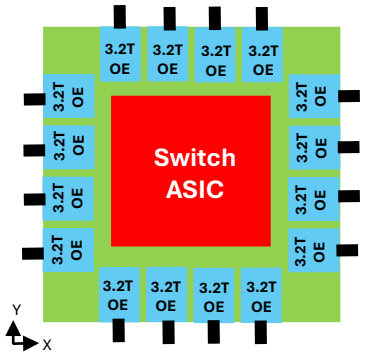
The CTE of Glass should be as close as to the PCB, instead of the Silicon chip.

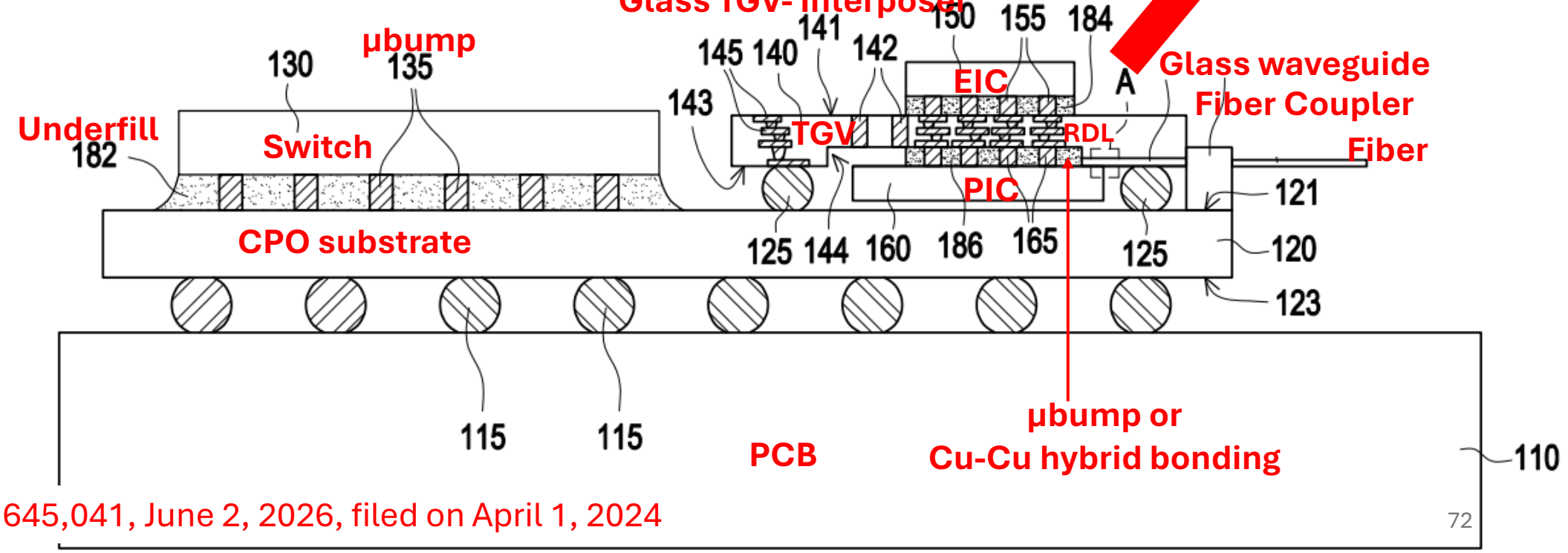
3D Heterogeneous Integration of CPO (Switch, PIC and EIC) on Glass Substrate and Glass Interposer

3D Heterogeneous Integration of PIC and EIC with Glass Interposer and Cu-Cu Hybrid Bonding



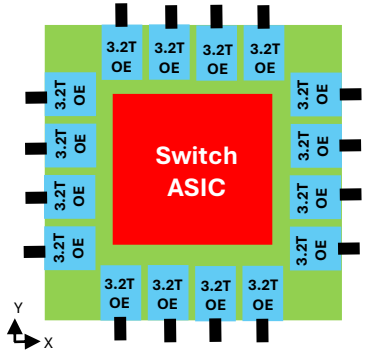


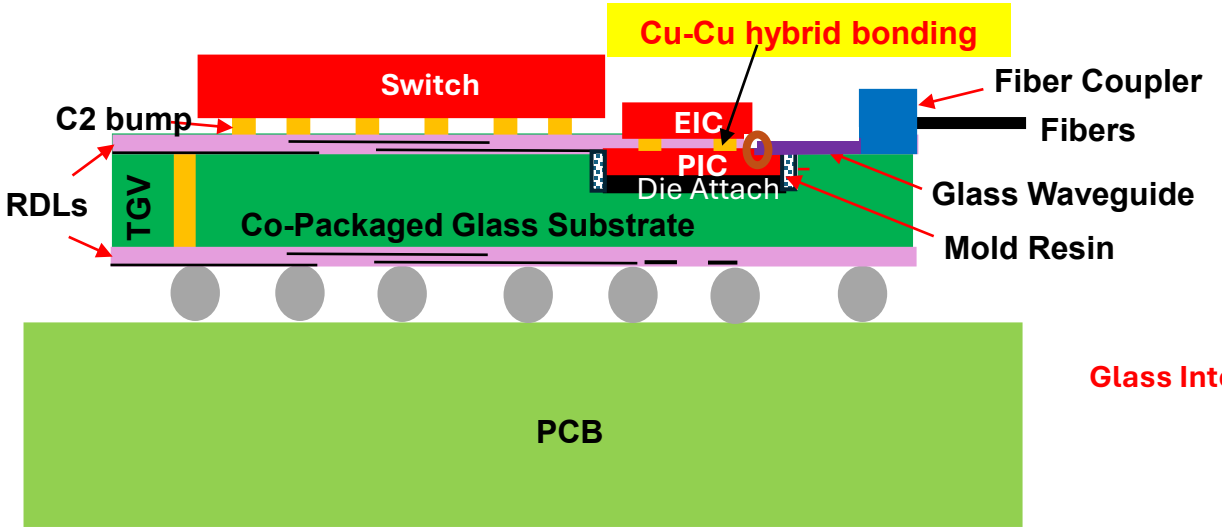


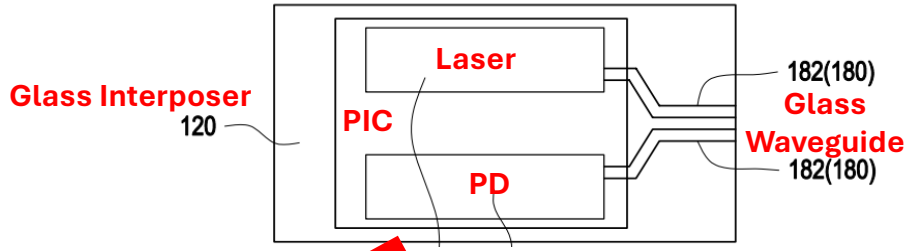


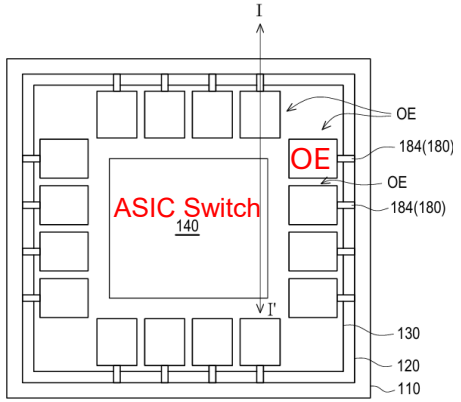
US Patent No. 12,645,041, June 2, 2026, filed on April 1, 2024

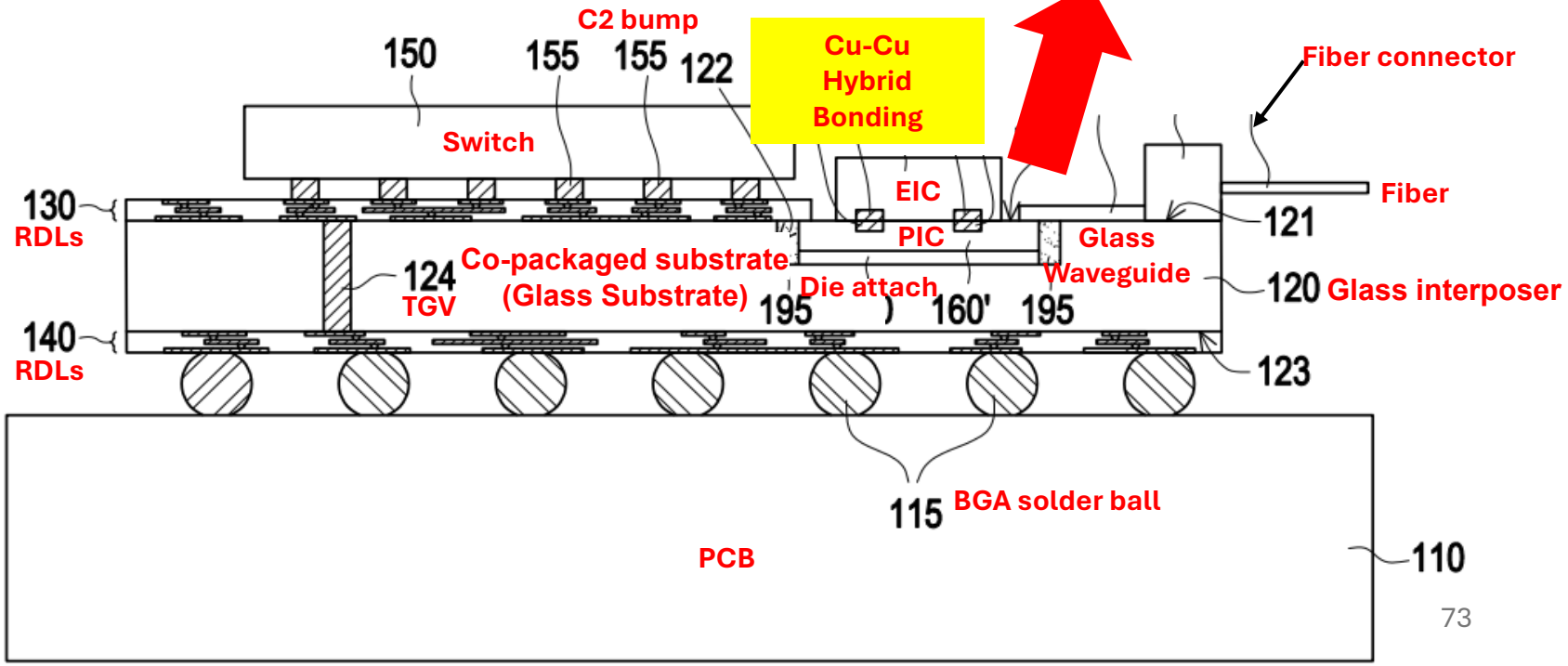
3D Heterogeneous Integration of EIC and PIC by Cu-Cu Hybrid Bonding with the PIC Embedded in a Co-Packaged Glass Substrate









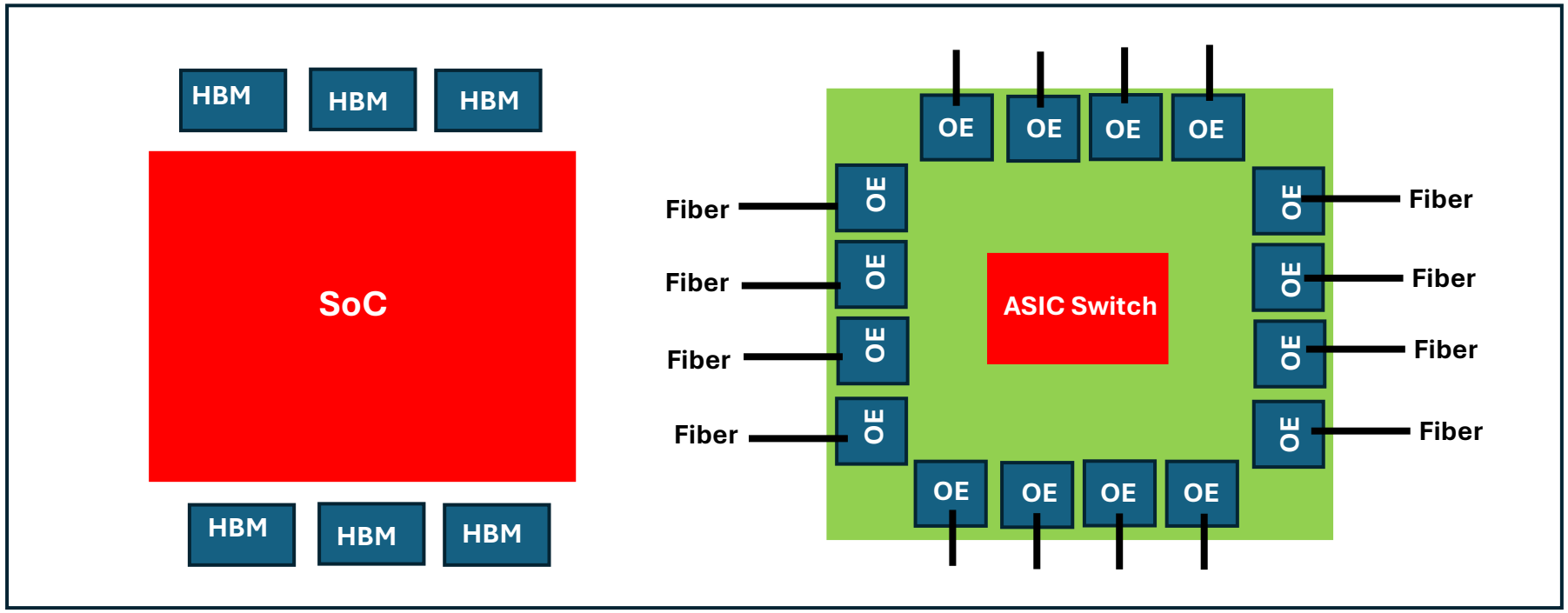


TW Patent I936450, filed on April 12, 2024

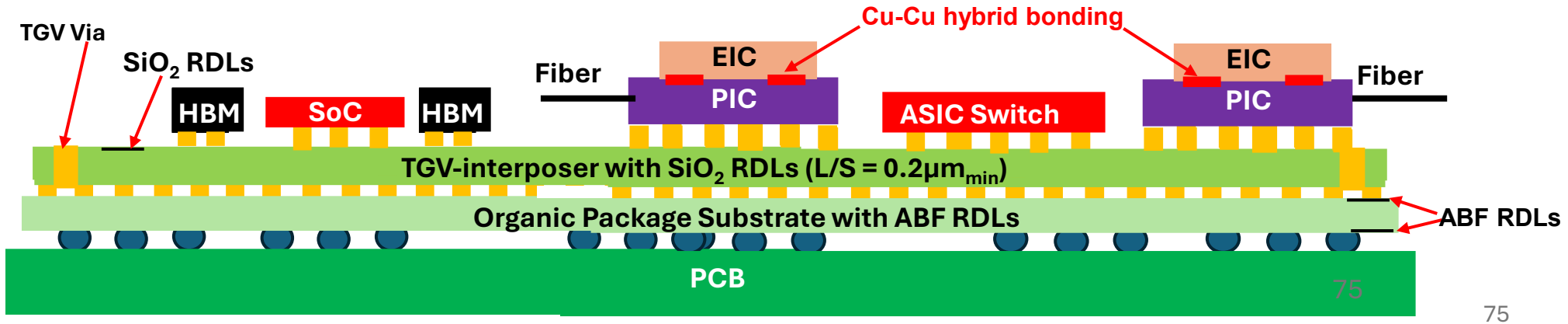
3.5D Heterogeneous Integration of Switch, PIC and EIC on Glass Interposer

3.5D Heterogeneous Integration of SoC, HBMs, Switch IC, PIC, and EIC on a TGV-Interposer in AI Era

Top-View



X-View



Patent pending

75

In General, the Challenges of Glass Packaging are:

- Micro-bubbles-free raw glass material formation
- Crack-free TGV formation
- Delamination-free seed layer formation
- Fine L/S = 0.2μm$_{min}$ SiO_2 RDLs fabrication on top of TGV interposer
- Fine 10μm < L/S ≥ 2μm ABF RDLs fabrication on both sides of glass-core substrate
- RDLs thickness uniformity
- Panel warpage for fabricating the RDLs
- Handling
- Testing
- Integration within existing manufacturing environments
- Immature technology
- etc.

SUMMARY and RECOMENDATIONS

- FOWLP and FOPLP are not glass packaging.
- Glass packaging either with a glass-core substrate or glass-core interposer is most suitable for HPC and date centers in AI era.
- 310mm × 310mm panel format strikes a critical balance: it is large enough to capture the area efficiency (cost) and small enough to maintain the processing control (yield). All the successful experience from 300mm-wafer can be adapted to 310mm x 310mm panel.
- Because there is underfill protection of the μbump solder joint on the glass substrate but there is no underfill protection for the BGA solder joints on the PCB. Thus, for flip chip applications, the CTE of glass is recommended to be as close as to that of the PCB, e.g., $10x10^{-6}/^{o}C$.

Some Recent Advanced Packaging Papers Published by the Lecturer and his Colleagues

1. Lau, J. H., "Recent Advances and Outlooks of Hybrid Bonding", *IEEE Transactions on CPMT*, 2027.
2. Lau, J. H., and N. Liu, "Silicon Bridges for Chiplets Heterogeneous Integration with Cu-Cu Hybrid Bonding" *ASME Transactions, Journal of Electronic Packaging*, 2027.
3. Lau, J. H., N. Liu, T. Tseng, "Microbump Reliability of Silicon Bridges for Chiplets Heterogeneous Integration", *Journal of Microelectronic Reliability*, Vol. 185, August 2026, pp. 116262.
4. Lau, J. H., "Current Advances and Outlook of Advanced Packaging", *ASME Transactions, Journal of Electronic Packaging*, published online: February 11, 2026.
5. Lau, J. H., "State-of-the-art and Outlooks of Cu-Cu Hybrid Bonding", *IEEE Transactions on CPMT*, Dec 2025, pp. 2575-2613.
6. Lau, J. H., "Co-Packaged Optics - Heterogeneous Integration of Chiplets (Switch, Photonic IC, and Electronic IC)", *J. of Microelectronic Packaging*, V 22, Issue 4, Dec. 2025, pp. 93-104.
7. Lau, J. H., N. Liu, M. Ma, and T. Tseng, "Flip Chip on Glass-Core Substrates with Microbump and Cu-Cu Hybrid Bonding", *J. of Microelectronic Packaging*, V. 22, I3, Sept.2025, pp. 44-60.
8. Lau, J. H., N. Liu, M. Ma, and T. Tseng, "Flip Chip on Glass-Core Substrates with Microbump and Cu-Cu Hybrid Bonding", *Journal of Microelectronic Packaging*, 3rd Quarter, 2025.
9. Lau, J. H., N. Liu, M. Ma, and T. Tseng, "Solder joint reliability - glass core substrate versus organic core substrate", *Journal of Microelectronic Reliability*, Vol. 168, May 2025, pp. 115701.
10. Lau, J. H., "Current Advances and Outlooks in Hybrid Bonding", *IEEE Transactions on CPMT*, Vol. 15, No. 3, March 2025, pp. 651-681.
11. Lau, J. H., "Co-Packaged Optics - Heterogeneous Integration of Photonic IC and Electronic IC", *ASME Transactions, J. of Electronic Packaging,* Vol. 147, March 2025, pp. 1-12.
12. Lau, J. H., "State-of-the-art of Cu-Cu Hybrid Bonding", *IEEE Transactions on CPMT*, Vol. 14, No. 3, March 2024, pp. 376-396.
13. Lau, J. H, G. Chen, et al., "Hybrid Substrates for Heterogeneous Integration" *ASME Transactions, J. of Electronic Packaging*, published online: Aug 11, 2023.
14. Lau, J. H, C. Lin, et al., "Hybrid Substrate with Ultra-Large Organic Interposer for Heterogeneous Integration", *IEEE Transactions on CPMT*, Vol. 13, No. 9, September 2023, pp. 1371-1379.
15. Lau, J. H., "Recent Advances and Trends in Chiplet Design and Heterogeneous Integration Packaging", *ASME Trans., J. of Electronic Packaging*, published online: June 23, 2023.
16. Lau, J. H., "Recent Advanced and Trends in Cu-Cu Hybrid Bonding", *IEEE Transactions on CPMT*, Vol. 13, No. 3, March 2023, pp. 399-425.
17. Lau, J. H., "Recent Advanced and Trends in Multiple system and Heterogenous Integration with TSV-Interposers", *IEEE Transactions on CPMT*, Vol. 13, No. 1, January 2023, pp. 3-25.
18. Lau, J. H., "Recent Advanced and Trends in Multiple system and Heterogenous Integration with TSV-less Interposers", *IEEE Trans. on CPMT*, Vol. 12, No. 8, August 2022, pp. 1271-1280.
19. Lau, J. H., "Recent Advances and Trends in Advanced Packaging", *IEEE Transactions on CPMT*, Vol. 12, No. 2, February 2022, pp. 228-252.
20. Lau, J. H., G. Chen, J. Huang, et al., "Hybrid Substrate by Fan-Out RDL-First Panel-Level Packaging, *IEEE Transactions on CPMT*, Vol. 11, No. 8, August 2021, pp. 1301-1309.
21. Lau, J. H., "State of the Art of Lead-Free Solder Joint Reliability", *ASME Transactions, Journal of Electronic Packaging*, Vol. 143, June 2021, pp. 1-36.
22. Lau, J. H., C. Ko, C. Lin, et al., "Fan-Out Panel-Level Packaging of Mini-LED RGB Display", *IEEE Transactions on CPMT*, Vol. 11, No. 5, May 2021, pp. 739-747.
23. Lau, J. H., C. Ko, K. Yang, et al., "Panel-Level Fan-Out RDL-first Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1125-1137.
24. Lau, J. H., C. Ko, T. Tseng, et al., "Panel-Level Chip-Scale Package with Multiple Diced Wafers", *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1110-1124.
25. Lau, J. H., "Recent Advances and Trends in Fan-Out Wafer/Panel-Level Packaging", *ASME Transactions, Journal of Electronic Packaging*, Vol. 141, December 2019, pp. 1-27.
26. Lau, J. H., M. Li, M. Li, et al., "Fan-out wafer-level packaging for heterogeneous integration," *IEEE Transactions on CPMT*, Vol. 8, Issue 9, September 2018, pp. 1544-1560.
27. Lau, J. H., M. Li, Q. Li, et al., "Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT.* Vol. 8, Issue 6, June 2018, pp. 991-1002.
28. Lau, J. H., M. Li, Y. Li, et al., "Warpage Measurements and Characterizations of FOWLP with Large Chips and Multiple RDLs", *IEEE Transactions on CPMT*, October 2018, pp. 1729-1737.
29. Lau, J. H., M. Li, D. Tian, et al., "Warpage and Thermal Characterization of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT*, Vol. 7, Issue 10, October 2017, pp. 1729-1738.
30. Lau, J. H., "Recent Advances and New Trends in Flip Chip Technology", *ASME Transactions, Journal of Electronic Packaging*, September 2016, Vol. 138, Issue 3, pp. 1-23.
31. Lau, J. H., Q. Zhang, M. Li, et al., "Stencil Printing of Underfill for Flip Chips on Organic-Panel and Si-Wafer Substrates", *IEEE Trans. on CPMT*, Vol. 5, No. 7, July 2015, pp. 1027-1035.
32. Lau, J. H., "Overview and Outlook of 3D IC Packaging, 3D IC Integration, and 3D Si Integration", *ASME Trans, Journal of Electronic Packaging*, Dec. 2014, Vol. 136, Issue 4, pp. 1-15.
33. Lau, J. H., C. Lee, C. Zhan, et al., "Low-Cost Through-Silicon Hole Interposers for 3D IC Integration", *IEEE Transactions on CPMT*, Vol. 4, No. 9, September 2014, pp. 1407-1419.
34. Peng, C., J. H. Lau, C. Ko, et al., "High-Density Hybrid Substrate for Heterogeneous Integration", *IEEE Transactions on CPMT*, Vol. 12, No.3, March 2022., pp. 469-478.
35. Lee, Z., J. H. Lau, CT Ko, et al., "Characterization of Low-Loss Dielectric Materials for High-Speed and High-Frequency Applications", *Materials Journal*, 15, 2022, pp. 1-16.
36. Ko, CT, H. Yang, Lau, J. H., et al., "Chip-First Fan-Out Panel Level Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, 2018, V 8, Issue 9, Sept. 2018, pp. 1561-1572.

Some Packaging Books Published by the Lecturer and his Colleagues

1. Lau, J. H., and K. N. Chiang, *Cu-Interconnects, Glass, and AI-Assisted Simulation for Chiplets Heterogeneous Integration,* (547 pages), Springer, New York, April 2026.
2. Lau, J. H., and X. Fan, *Hybrid Bonging, Advanced Substrates, Failure Mechanisms, and Thermal Management for Chiplets and Heterogeneous Integration,* (645 pages), Springer, New York, April 2025.
3. Lau, J. H., *Flip Chip, Hybrid Bonding, Fan-In, and Fan-Out Technology*, (501 pages), Springer, New York, 2024.
4. Lau, J. H., *Chiplet Design and Heterogeneous Integration Packaging*, (525 pages), Springer, New York, 2023.
5. Lau, J. H., *Semiconductor Advanced Packaging*, (498 pages), Springer, New York, 2021.
6. Lau, J. H., and N. C. Lee, *Assembly and Reliability of Lead-Free Solder Joints*, (527 pages), Springer, New York, 2020.
7. Lau, J. H., *Heterogeneous Integrations*, (367 pages), Springer, New York, 2019.
8. Lau, J. H., *Fan-Out Wafer-Level Packaging*, (303 pages), Springer, New York, 2018.
9. Lau, J. H., *3D IC Integration and Packaging*, (458 pages), McGraw-Hill, New York, 2016.
10. Lau, J. H., *Through-Silicon Via (TSV) for 3D Integration*, (487 pages), McGraw-Hill, New York, 2013.
11. Lau, J. H., *Reliability of RoHS compliant 2D & 3D IC Interconnects*, (606 pages), McGraw-Hill, New York, 2011.
12. Lau, J. H., C. K. Lee, C. S. Premachandran, and Yu Aibin, *Advanced MEMS Packaging*, (552 ages), McGraw-Hill, New York, 2010.
13. Lau, J. H., C. P. Wong, N. C. Lee, and R. Lee, *Electronics Manufacturing with Lead-Free, Halogen-Free, and Adhesive Materials*, (643 pages), McGraw-Hill, New York, 2003.
14. Lau, J. H., and R. Lee, *Microvias for Low Cost, High Density Interconnects*, (565 pages), McGraw-Hill, New York, 2001.
15. Lau, J. H., *Low Cost Flip Chip Technologies for DCA, WLCSP, and PBGA Assemblies*, (585 pages), McGraw-Hill, New York, 2000.
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Thank You Very Much for Your Attention!

