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Taiwan Semiconductors

AI Chip Testing - The Hidden Infrastructure Behind the Age of Advanced Packaging; Initiate on MPI at Buy/High Risk

Deep Dive

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CITI'S TAKE

Leading-edge advanced packaging has become essential for AI chips as system performance is now determined by interconnect, memory bandwidth, and power efficiency rather than transistor scaling alone. Advanced packaging enables large AI dies to overcome reticle limits, integrate multiple compute, I/O dies and HBM with minimal latency. This packaging-driven architecture allows AI accelerators to scale compute-density while managing power and thermal constraints. As AI chips become more expensive, advanced packaging directly impacts performance, yield, and cost-structure. Consequently, packaging and testing is no longer a simple backend consideration but a core-architectural decision, reshaping how AI-chips are designed, manufactured, and tested across the semiconductor value-chain. Given structural upside on AI chip, we expect TSMC's CoWoS capacity to reach 1.2-1.3m/1.8-2m wafers in 2026/27 and ASEH to reach 200k+ in 2027. We lift TP for ASEH and KYEC to NT$340 and NT$330 respectively and initiate on MPI at Buy/High Risk in probe card space.

ASEH and KYEC see more upside on testing; ASEH also sees strong growth in CoWoS – We have lifted our TSMC's CoWoS estimate in our latest TSMC report. ASEH looks to not just focus on the assembly and integration side, executing complex CoWoS processes, they are also doing wafer testing for Nvidia. We estimate ASEH's leading edge advanced packaging revenue to reach US$4bn in 2027. For KYEC, it is more directly exposed to advanced testing requirements, particularly in the final test and validation of high-performance AI packages. Both companies should benefit from TSMC's wafer testing business for AI chip, and we see GM upside for both given advanced packaging shifts value towards precision manufacturing and deeper test coverage rather than pure volume.

MPI - A unique player in probe card industry for wafer testing - As AI chips move towards costly CoWoS and chiplet-based packages, ensuring known-good-die at wafer level becomes economically essential. As a leading probe card maker in Taiwan, MPI influences yield and cost outcomes in upstream, where defects can be screened before expensive packaging steps. MPI clients include most of the ASICs players like Broadcom and Marvell. It also provides gaming, automotive and I/O die test probe card for Nvidia. With accelerating ASIC momentum and its rising role in advanced chips design, we estimate MPI to deliver a strong 48% sales CAGR through 2025-27E, in line with TSMC's guidance of its AI revenue growth at mid-40s%.

Initiate on MPI at Buy/High Risk with TP of NT$2,800 - We initiate on MPI at Buy/High Risk with TP based on the thesis that the company has transitioned from a cyclical probe card supplier to a structural beneficiary of AI-driven test complexity. Despite its premium valuation and very strong share price performance over past ~9 months, accelerating AI ASIC and specs upgrade will drive further upside in our view. We are looking for 77% and 64% earnings growth in 2026 and 2027 thanks to better product mix and more upside from MEMS probe card. The stock has traded at a PER range of 10-45x in the past 3 years. With the promising growth from AI chip, we set PER target of 37x at the high-end of its historical PER to the average of our 2026-27 EPS estimates.

See Appendix A-1 for Analyst Certification, Important Disclosures and Research Analyst Affiliations.

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Data Summary

															Current Fiscal Year		Next Fiscal Year	
						Rating		Short-Term	Target Price						EPS		EPS	
Company	Ticker	Ccy	Price	Mkt Cap (M)	Date & Time	Old	New	View	Old	New	ESPR (%)	Div Yld (%)	ETR (%)	Last Rpt Yr	Old	New	Old	New
ASE Technology Hldg	3711.TW	NT$	272.00	1,206,631	09 Jan 13:30	1	nc	Upside^	252.00	340.00	25.0	2.5	27.5	Dec-24	8.88	nc	13.92	15.15
King Yuan Electronics	2449.TW	NT$	263.50	322,193	09 Jan 13:30	1	nc	Upside	271.00	330.00	25.2	2.2	27.5	Dec-24	9.02	8.97	10.01	9.65
MPI	6223.TWO	NT$	2,230.00	211,696	09 Jan 15:00		1H	Upside	-	2,800.00	25.6	1.0	26.5	Dec-24	-	32.13	-	56.74

1 = Buy, 2 = Neutral, 3 = Sell, H = High Risk
ESPR = Expected Share Price Return, ETR = Expected Total Return, nc = no change
Source: Citi Research
^Catalyst Watch

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Reiterate our Buy ratings on ASEH and KYEC with new TP of NT$340 and NT$330 respectively – We revise up our ASEH 2026/2027 earnings projection for ASEH by 9%/32% anticipating robust GM recovery trend thanks to higher ASP and secular AI and leading-edge advanced packaging growth. With better visibility on AI demand and structural earnings trajectory, we lift our target price to NT$340 for ASEH; On KYEC, we are looking for 36% and 53% revenue growth in 2026/2027 with 7% and 57% earnings growth. Given longer testing process, we expect KYEC's GM to expand gradually with robust AI chip shipment trend. With its secular growth trend and upside from TPU other than GPU, we lift our target price to NT$330.

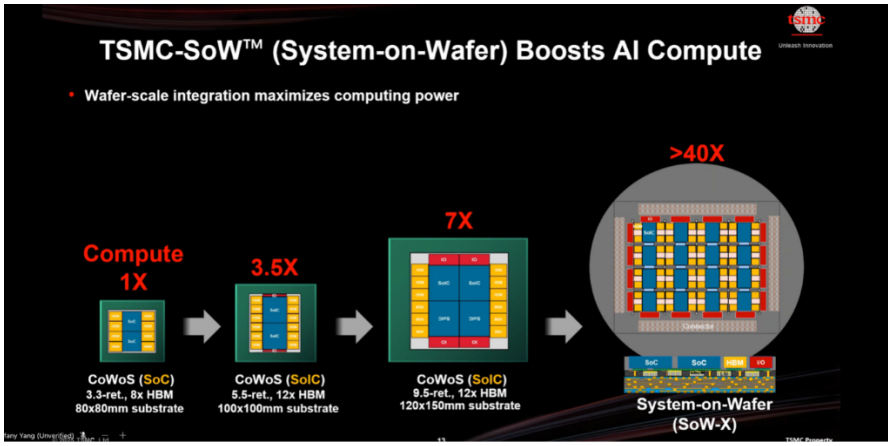
AI testing a strategic enabler

Increasing AI design complexity leads to longer testing process

The rapid ascent of AI development has not only redefined computing demand but also reshaped the semiconductor industry supply chain and technology roadmaps. Advanced packaging such as CoWoS, InFo, SoIC have moved from being specialist approaches to critical element of the AI computing system. They enable multiple dies - logic, memory, I/O and chiplets - to be combined in a single package, providing bandwidth and performance that would be impossible with monolithic scale alone. Yet as packaging complexity rises, so does the cost of the failure. As CoWoS packaging integrates logic dies and multiple HBM, a single defective die can cause the entire assembly scrapped.

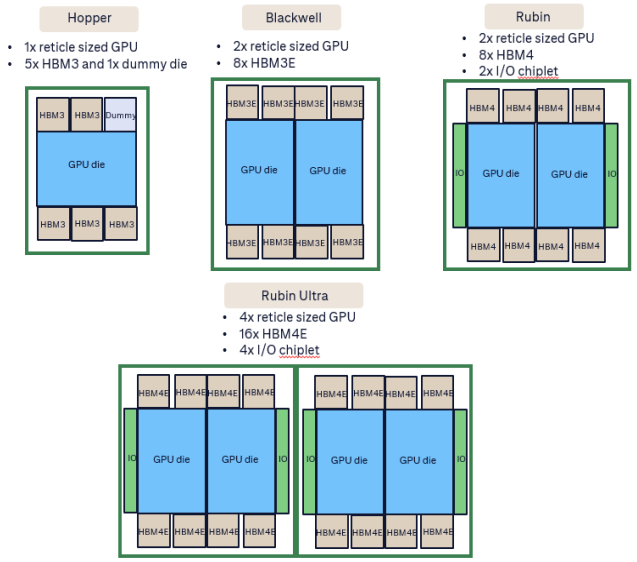
Starting from Nvidia, we see more and more AI chips now implementing chiplet design, which has logic processor packaged with HBM and I/O chips and interconnected via silicon interposers or direct die to die bond when moving to N3/N2 for their next generation AI chips.

Figure 1. Higher computing capability through TSMC's innovative packaging solutions



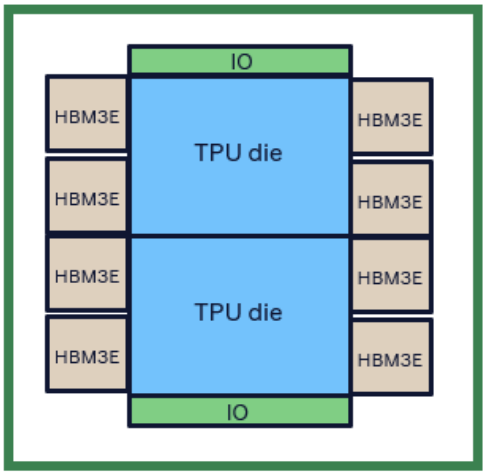
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Source: Citi Research, TSMC

Figure 2. Nvidia's AI GPU structure-from single die to multi-die chiplet



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Source: Citi Research

Figure 3. Google's TPU (Ironwood) structure – The latest chiplet design from AI ASIC



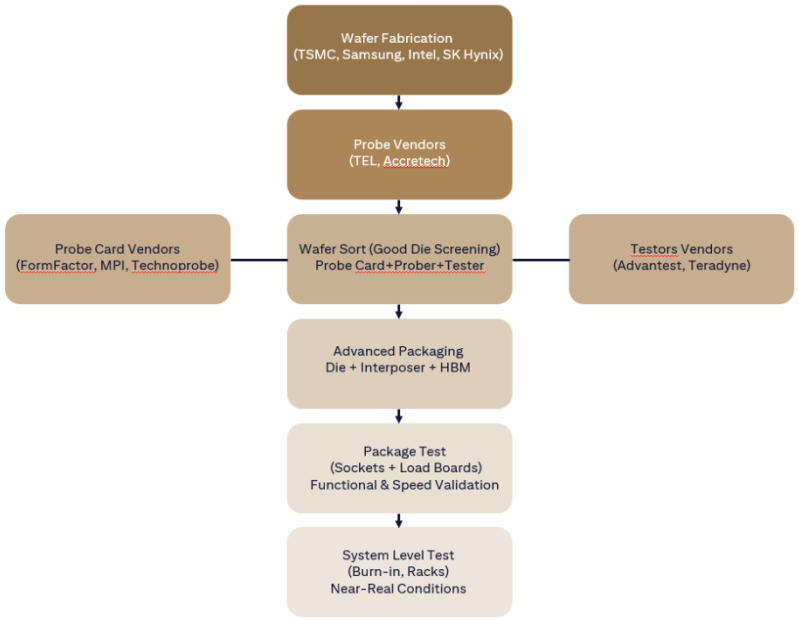
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AI Chip Testing - The Hidden Infrastructure Behind the Age of Advanced Packaging

With AI's strong growth trend which drives an exponential surge in compute demand, the hardware backbone of the AI ecosystem spanning from GPUs, ASICs and HBM has reached unprecedented complexity. As chips transits from monolithic dies to multi-chiplet system, the physical alignment and structural integrity of every micro-bump, TSV, and interposer trance determine whether downstream electrical connections can function well. If a wafer's topography drifts outside specification, electrical contact will be unreliable or be damaged. Advanced optical interferometry, white-light profilometry and 3D scanning are therefore integrated directly into wafer-sort lines, providing the geometric "map" that guides probing.

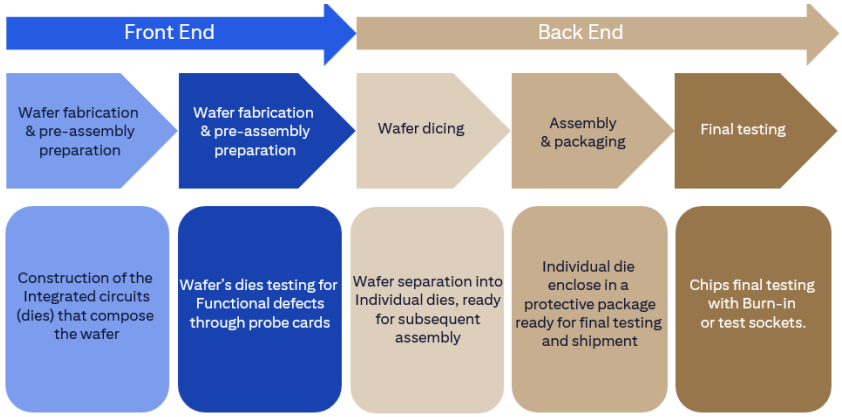
During assembly, metrology steps verify die-to-interposer alignment, TSV depth and void within underfill or bonding layers. After packaging, it inspects warpage, coplanarity and delamination, ensuring that packaged chips can sit correctly in socket for final test. Each stage feeds precise coordinate and deformation data into the test program so that probe pressure, alignment and electrical parameters can be adapted in real time.

Figure 4. Chips manufacturing and testing process flow



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Figure 5. Chips packaging and testing process



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Wafer Probing Test - The first electrical gatekeeper of known-good dies

Once physical readiness is confirmed, wafers proceed to wafer probing, the first electrical test in the AI chip lifecycle. Wafer probing serves to achieve the very important purpose: **to identify known good die (KGD)** before packaging. Dies that fail electrical, parametric or leakage tests are marked and excluded from CoWoS process. The wafer sits on a precision prober, and a customized probe card connects thousands of micro scale probes to the chips contact pad or micro-bumps. Through this interface, an automated tester applies voltage, logic vectors and timing patterns to verify functionality.

For AI accelerators, the process is extremely complex. A single GPU or ASIC may contain over 20,000 contact points at bump pitches below 45um, carrying hundreds of amps across multiple power domains. The probe card, often a MEMS fabricated array built through semiconductor processes must maintain sub-micro planarity and stable contact resistance across millions of touchdowns. Even minute mechanical drift can cause open contacts or short circuits.

Every chip that enters an AI data center today must pass through a critical test and validation stage. Current probe stations also integrate environmental temperature control. Data from wafer-level tests feeds into predictive analytics models that estimates die reliability and performance binning, which is critical for allocating HBM and logic dies during assembly. And once KGD are identified, they move into advanced packaging, these multiple logic and memory dies are combined on a silicon interposer or stacked through hybrid bonding. After this integration, the resulting chiplet module becomes an even more complex system in electrical and thermal. At this stage, final testing (FT) will be checking on packaging level test to verify system level functionality.

Final Testing - Validating performance after packaging

With AI chip getting much more powerful and advanced, each test vector is tailored to the specific AI architectures and requires massive data throughput and real-time analysis. Tester platform has thus evolved towards modular, high-parallel architectures capable of scaling channels dynamically. With the **testing socket** mounted on a load board, it will run the validation of:

- High speed I/O characterization.
- Power-delivery and current-stress verification, which ensures that the interposer rails meet design limits.
- Timing, jitter and signal integrity measurements, confirming that packaging does not degrade performance.

Final test is also the first point where mechanical and electrical domains interact at scale. Warpage or misalignment observed by metrology tools can cause contact irregularities in sockets. Hence, we see the trend that final test can provide feedback adjustment in wafer probing parameters or packaging processes and the yield optimization becomes a continuous data-driven system.

Burn-in and System-level validation - proving reliability over time

Passing functional test is not enough for AI chips running in hyperscale data centers. The final gate is burn-in and system level test, which ensures long term reliability under sustained electrical and thermal stress.

In this phase, packaged chips are mounted on burn-in board or system-emulation racks and operated at elevated temperature and voltages for hours. The objective is to accelerate early-life failure to find marginal transistors, weak interconnects or micro-void.

For AI devices consuming hundreds of watts and moving to more that 2k watt with Nvidia's next generation Rubin GPU, burn-in environments replicate real data-center workload. Dynamic power swings, temperature cycles, and real signal stream are applied to simulate months of operation in compressed time. The resulting data-failure signatures, thermal drift, leakage evolution will feedback into both packaging and wafer sorting design.

The importance of Probe Card

After the wafer is processed and goes to advanced packaging, and before the wafer is diced and enters CoWoS, every die must be tested. The testing cell consists of a few components. The tester, supplied by companies like Advantest and Teradyne, generates test vectors and measure response. The prober handles the wafer and aligns it under precise environmental conditions. **And between them stands the probe card. It is the bridge between microscopic pads on the wafer and the electronics of the tester. It carries current, transmits high frequency signals and ensures mechanical compliance across thousands of contact points.**

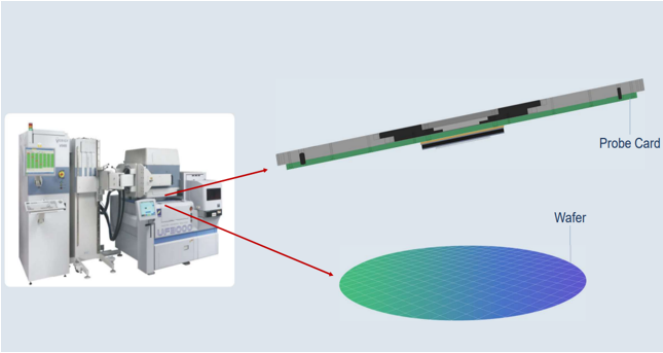
To simplify, a probe card is an electromechanical interface used to test the functionality of a chip while it is still on the wafer - before the chip is diced and individually packed. The advanced packaging has made test interfaces inseparable from system performance. The probe card has become the critical enabler, ensuring that the dies entering packaging are functional, reliable and capable of sustaining the stresses of advanced assembly and operation.

This mechanical sensitivity demands low force probing and highly compliant probe card systems, especially when contacting small micro-bumps. Also, the variability in die positional after singulation-often while still mounted on a film frame-requires sophisticated alignment and stable contact mechanics from the probe card to ensure consistent, multi-site testing. During wafer probing, the probe card physically contacts the chip's pad or micro-bumps. Once proper contact is established, the probe card provides the electrical connection between the chip and the tester, allowing the tester to verify the chip's performance and identify defects. Because every chip design has unique pad layouts and electrical requirement, each probe card is custom designed for the specific device being tested.

For high-power AI devices, transitional wafer-level probing is insufficient due to thermal limitation. High power AI chips generate substantial heat during test. Wafer level thermal control relies on passive conduction through silicon bulk, but die testing requires active thermal control to rapidly stabilize die temperature, prevent hot spot migration, and maintain consistent electrical behavior.

Physical realities such as electrical noise, contact resistance drift over time, and systematic wear or contamination on probe tips inject noise into the measurement signal before it is digitized. As a result, new solutions involving active thermal control are being deployed specifically for bare die testing, allowing manufacturers to run full, at-speed final test programs at the die level. The ability to guarantee KGD is now directly contingent upon the stability, precision, and physical compliance of the prove technology used in this critical screening step.

Figure 6. The probe card uses needles to touch the terminals (pads) of chips, thus electrically connecting to a tester



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Source: Citi Research, Technoprobe

Figure 7. The components structure inside the probe card



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As the AI boom has magnified testing process, and like we mentioned earlier, probe card is faced with unprecedented complexity as GPUs and HBM dies push through 20,000 contacts at pitches smaller than 40um. We thus see that at the package level, sockets must withstand higher power, faster I/Os and tighter tolerances to validate chips. Both probe card and the sockets, once treated as consumables, have become strategic enablers of yield-enhancement in AI manufacturing.

This risk has elevated the importance of testing, from wafer level testing to final testing. Probe card is in the most critical wafer sorting testing process in our view, as the highly sophisticated interfaces connect the test system to the microscopic pad and bumps on each die. Based on probe cards' technology, it can determine whether a die is a Know Good Die (KGD) and then is ready to enter the advanced packaging stage. Therefore, for probe card makers, it is increasingly required to engineer flexible, thermally stable probe capable of sustaining contact quality across temperature cycles without compromising die integrity.

Among advanced packaging elements, HBM is the most disruptive for probe cards. Each HBM stack contains 8-16 dies vertically connected through TSVs. These connects to GPUs or AI ASIC via ultra-wide interface of 1,024-2,048 bits at pitches of 55um/45um and approaching 36um for HBM4. More importantly, probe card are not commodities. Each card is custom designed for a specific chip. The engagement includes:

1. Jointly design-in with chipmakers and ATE vendors.
2. Long qualification cycles, usually 12-18 months
3. Volume production synchronized with wafer ramp up
4. Recurring maintenance, refurbishment and needle replacement.

Going forward, we see the trend of higher pin counts, greater electrical current handling and testing coverage for chiplet and memory stack. The evolution of packaging has redefined wafer probing as the frontline safeguard against catastrophic downstream losses.

Business model creates high switching cost and strong vendor lock-in in supply chain ecosystem

As probe card acts as the critical physical interface between the automatic test equipment and the wafer, it provides reliable electrical contact between tens of thousands of microscopic chip pad or micro bumps and the tester. It embodies a convergence of mechanical precision, material and signal integrity engineering.

Because each chip requires a custom probe card, the relationship between vendor and customer is project-based and sticky, with long qualification cycles. Once qualified, suppliers often enjoy recurring revenue from maintenance, refurbishment and next-generation integrations.

The semiconductor industry is undergoing rapid changes with advancements in AI, HPC and advanced packaging, which requires increasingly sophisticated probe card for high-density, high-power testing. ATE firms lack the deep domain expertise or agility to keep pace with these specialized requirements in-house, as probe development involves filling know-how gaps in adjacent areas like materials and interconnect. Partner with dedicated probe card specialists allows for faster innovation and shared roadmaps.

Figure 8. AI GPUs and ASIC testing supply chain

AI chip makers	Wafer testing (CP) partner	Final testing partners	Probe cards suppliers
Nvidia	*TSMC performs CP in-house for GPU using its own probe card built with Technoprobe and CHPT. *Gradually outsourcing to OSATs ASE/SPIL	KYEC	MPI, Technoprobe, CHPT
Broadcom	SPIL, KYEC, Amkor, Powertech	Amkor, ASE/SPIL, KYEC	MPI
AWS/Marvell/Alchip	Mainly on OSATs	ASE/SPIL, KYEC	MPI
AMD	Mainly on OSATs	ASE/SPIL	

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Competitive Landscape

FormFactor as global leader

FormFactor (covered by Elizabeth Sun) has long stood as the undisrupted leader in the global probe card market, a position it has maintained through deep technology investment, breadth of product portfolio, and extensive partnerships with major semiconductor manufacturers. According to TechInsights, FormFactor consistently ranks at the top of probe card vendor lists and is broadly credited with the largest share of the advanced MEMS probe card segment — often estimated at roughly 28% of global unit shipments in 2024 and leading overall revenue contributions in the space.

FormFactor's core competitive advantage centers on its development and deployment of Micro-Electro-Mechanical Systems (MEMS) probe card technology.

MEMS cards are critical for testing modern high-density logic, 3D packaging, and advanced DRAM/NAND applications used in AI accelerators, advanced CPUs, and heterogeneous chiplet designs. They provide extremely fine pitch contact solutions (often below 60 μm) with high electrical fidelity and planarity that mechanical probes cannot reliably deliver. This precision gives foundries, IDMs, and OSATs the confidence to move into advanced nodes and complex packaging, such as CoWoS, InFO, and 3D-stacked memory modules.

Technologically, FormFactor emphasizes patented MEMS design and integration with test ecosystems, enabling high reliability and scalability for sub-7nm and future nodes. FormFactor's R&D scale is also illustrated by sustained investment in next-generation probe cards with enhanced signal integrity, automated calibration, and adaptive contact control — all geared toward very large pin counts (10k+). North America is a particularly strong region for FormFactor, holding a significant portion of its revenue and strategic partnerships with Western logic designers, although its reach extends globally through localized service and engineering.

On applications, FormFactor's products find the widest adoption in foundry & logic test flows, where volume and technological barriers are highest. Although memory and automotive IC segments also consume probe cards, the primary volume and revenue contributions for FormFactor derive from logic and advanced packaging — which account for roughly 72% of the overall probe card application base.

FormFactor's dominant market position comes not just from sales volume, but also from an extensive patent portfolio and strategic co-development programs with leading fabs (e.g. TSMC and Samsung). These defensive positions make it difficult for new entrants to replicate their technology at scale — contributing to powerful entry barriers in the probe card ecosystem.

Technoprobe: European engineering with global reach

Technoprobe S.p.A. (non-rated), headquartered in Italy, is widely recognized as the second largest probe card supplier globally. Market research study (SEMI) consistently positions Technoprobe within the top two players in terms of revenue, unit shipments, and technological presence. In a recent analysis by TechInsights, Technoprobe is often shown to hold between 12%–24% share of global probe card shipments depending on the metric (units vs. revenue), underscoring a significant footprint despite formidable competition from FormFactor.

Its core strength lies in its vertical probe card solutions — which historically have been favored for a broad array of memory (DRAM/NAND) and logic test applications. Vertical probe cards use straight needle designs that excel in high-current and high compliance testing, making them well-suited for chips with a mix of dense logic and power-domain requirements. Technoprobe also invests heavily in MEMS hybrid and vertical MEMS designs that can span the requirements of both legacy and next-generation node testing.

The company's technology strategy emphasizes scalability and regional presence, with manufacturing and engineering centers positioned near major customer clusters in Europe and Asia. Technoprobe has expanded operations in Taiwan and Korea to strengthen its proximity to key foundry and OSAT customers, enabling shorter design cycles and faster turnaround for custom probe card requirements.

Application-wise, Technoprobe serves a broad spectrum: high-volume memory test flows, logic and microprocessor validation, and increasingly, advanced packages including multi-die heterogenous ICs. Its products are used by major

fabs and test houses that demand both volumetric capacity and consistent quality. In some 3D and 2.5D packaging use cases, Technoprobe's vertical designs remain competitive where ultra-fine MEMS may not yet be cost-effective.

Regionally, Technoprobe's strength has been historically strong in Europe, but its strategic facilities in Asia facilitate greater penetration in the Asia-Pacific — the world's largest semiconductor manufacturing region. This global engineering footprint is a differentiator in a market where speed of customization and local support often tip vendor selection in favor of closer partners.

Micronics Japan (MJC): Japanese Precision in a Regional Niche

Micronics Japan Co., Ltd. (MJC) (non-rated) represents one of the most important probe card vendors within the Asia-Pacific and Japanese domestic landscape, routinely ranks as the global top 3–5 players, per SEMI. MJC is consistently identified as amongst the top-three suppliers in rankings of probe card vendors, often alongside FormFactor and Technoprobe in revenue and capability.

MJC's core technological strength lies in precision engineering and materials expertise, honed through decades of supplying high-reliability vertical and MEMS probe cards. Japan's semiconductor ecosystem — with its legacy in memory manufacturing, high-reliability automotive ICs, and niches like RF/analog test — has historically favored suppliers with deep mechanical and materials know-how. MJC fills that role with solutions optimized for these segments.

Unlike FormFactor's global MEMS leadership or Technoprobe's vertical-centric broad suite, MJC has carved a regional niche that reflects Japan's domestic demand and multi-site manufacturing culture. Its probe cards often leverage proprietary substrate materials and packaging interfaces that favor high durability and contact life, aligning with long test cycles and reliability-critical applications. This specialization helps MJC maintain solid market share in segments like automotive, industrial logic, and memory test, particularly where rigorous environmental test conditions are critical.

Market research (Mordor Intelligence) indicates that MJC — as a brand — collectively with JEM (Japan Electronic Materials) and other Japanese vendors accounts for a sizeable portion of the Asia-Pacific probe card market, contributing significantly to the roughly 60–80% regional dominance of APAC in production.

However, MJC's reach outside Japan and Korea is comparatively lower than that of FormFactor and Technoprobe, limiting its penetration in North America and Europe. Nonetheless, its steady performance in regional accounts and specialization in robust, precision test cards keep it as a vital player in the oligopolistic probe card landscape.

MPI Corporation: Taiwan's rising challenger with niche focus and market share upside

MPI Corporation, based in Taiwan, has steadily risen in the competitive hierarchy of probe card vendors. According to recent rankings by TechInsights, MPI has climbed to the top five global probe card suppliers, consistently holding a position around 4th–5th globally in total probe card revenue and unit ranking over the past several years.

MPI's strategic advantage stems from flexibility, proximity to Taiwan's semiconductor ecosystem, and specialized MEMS and vertical probe design capabilities. Unlike larger peers, MPI's business has evolved to serve both

conventional logic/test flows and edge niches such as high-speed RF and mixed-signal test cards. Its Taiwan base allows for tight integration with TSMC, ASEH, and local IDMs — providing rapid customization and engineering support that many global sellers cannot match.

Technologically, MPI's probe cards are designed for high-frequency, complex packaging applications — particularly where fast turnaround and co-development are needed. The company's integration of probe stations with automation and thermal solutions positions it as a versatile provider capable of serving both wafer sort and advanced packaging test flows. These strengths are reflected in rising non-memory card rankings and regional order volumes, even as its overall share remains below the top three.

The competitive landscape shows that while MPI's absolute market share is smaller than FormFactor's and Technoprobe's, it plays a strategic role in Taiwan and surrounding regions — a critical advantage given the concentration of leading foundries and OSATs in that geography. Additionally, MPI's closer customer integration and possible collaborative efforts with other probe card and tester vendors provide growth pathways in segments where speed and custom engineering trump volume economics.

Overall Competitive Dynamics

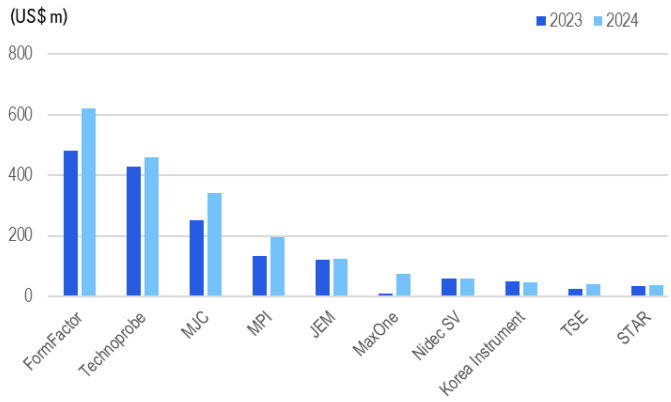
Collectively, the probe card market exhibits high concentration and significant technological barriers. The top players — FormFactor, Technoprobe, MJC, and MPI — along with a handful of others, command majority of the AI chip probe card market.

Key differentiators among these players include:

- **Technology leadership:** MEMS probe card precision at fine pitches drives testing for cutting-edge chips.
- **Application focus:** Logic and advanced packaging require high-density cards; memory and automotive rely on durability.
- **Regional reach and service:** Proximity to fabs and OSATs significantly affects adoption and support cycles.

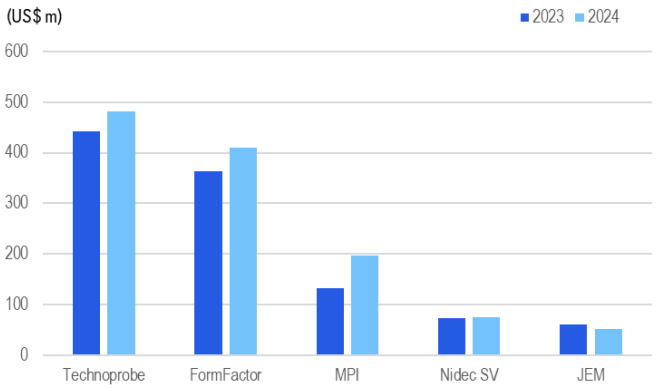
In this landscape, FormFactor leads globally with MEMS innovation and scale, Technoprobe offers broad vertical expertise with high volume, MJC holds a strong regional niche with precision materials, and MPI punches above its weight with Taiwan-centric agility and specialized test solutions.

Figure 9. Global Top 10 probe card players – revenues comparison



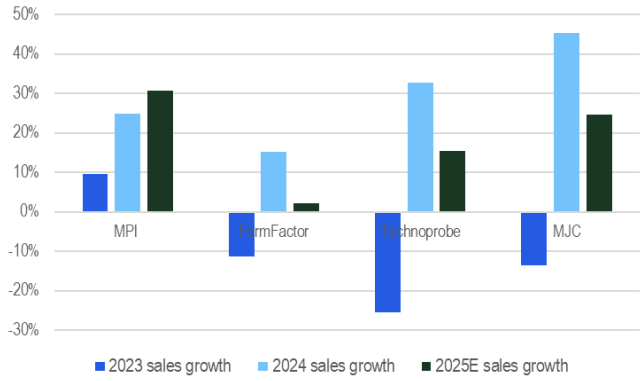
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Source: Citi Research, MPI

Figure 10. Global non-memory Top 5 probe card players - revenues comparison



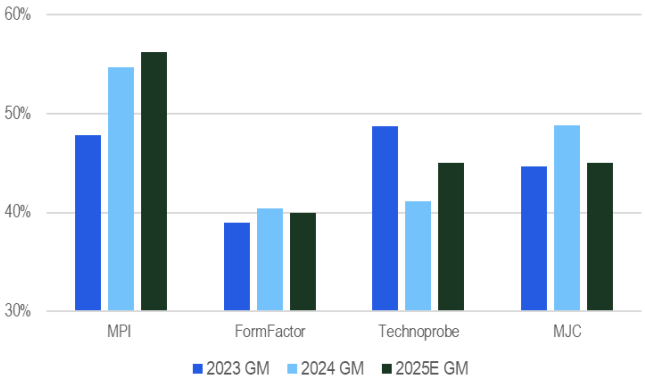
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Source: Citi Research, MPI

Figure 11. Revenues growth comparison with key global peers



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Source: Citi Research, MPI

Figure 12. Gross margin comparison with key global peers



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Source: Citi Research, MPI

Figure 13. Comparison of Taiwan probe card and test interface peers

		MPI (6223.TW)	WinWay (6515.TW)	CHPT (6510.TW)	KSMT (6683.TW)
Financial Summary	Market Cap (US$bn)	7	3	2	0.4
	2025/26E revenues (NT$m)	13,287/19,347	7,660/10,342	4,820/6,229	2,107/2,711
	2025/26E revenues growth (%)	31%/46%	32%/35%	34%/29%	21%/29%
	2025/26E GM (%)	56%/59%	46%/42%	55%/55%	45%/47%
	2025/26E EPS (NT$)	32.1/56.7	45.2/68.5	28.2/43.2	13.0/18.9
	2025/26E EPS growth (%)	31%/77%	34%/52%	82%/53%	-26%/45%
Operation Summary	**Products Mix (%) in 2025E**				
	Probe Card	71%	32%	66%	30%
	Load Board/Burn-in Board			23%	65%
	Contact Element (Pins)		10%		
	Socket		54%		
	Others	29%	4%	11%	5%
	Business Model	Providing Probe Card (insourcing Probe Head & Substrate; partially PCB insourcing)	Providing Probe Card & Socket	Mostly in-house production	Mainly providing Substrate & Load Board
	Sales mix (%) by applications	Probe Card sales breakdown: HPC 40% Consumer 25% Networking 20% DDIC 13% Auto 4% AP 3%	HPC 45% PC 30% Networking 20% Smartphone 5%	HPC 40% AP 23% Gerber 11% RF 7% PMIC 6% SSD 1% Others 12%	AP >50% RF 10-20% TV SoC 5-10%
Products Coverage	Probe Card PCB/Substrate	v		v	v
	Probe Head	v		v	
	Cantilever Probe Card	v			v
	Vertical Probe Card	v	v		v
	MEMS Probe Card	v	v	v	
	Load Board/Burn-in Board			v	v
	Test & Burn-in Socket		v	v	
Capacity	Probe Card	*CPC: 500k pins/month *VPC: 1.2m pins/month; +10% in 2026E *MEMS: 1m pins/month in 2025E; doubling in 1H26E			
	PCB/Load Board			*Fab 3 to start production in 2028 with total capacity to double	
	Test & Burn-in Socket		*3.5m pins/month in 2025E; growing to 5m/7m pins by 2Q26/4Q26E		

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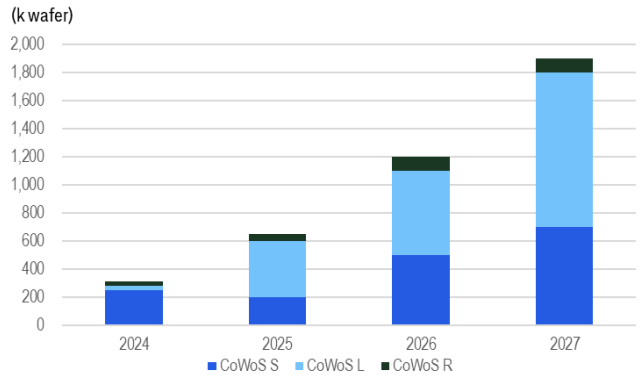
Source: Citi Research, Bloomberg estimates for WinWay, CHPT and KSMT's financial summary

AI chip growth trend - GPU growth remains strong; ASIC led by TPU

By our estimate, thanks to better ecosystem control and supply chain capacity support, Nvidia will likely continue to share over 50% of TSMC's advanced packaging capacity with total capacity to be 650k or higher wafers in 2026. Among major CSPs, AWS and Google have been working on their own chips solution for years and have their own AI framework and ecosystem internally. This trend underscores the growing appeal of ASICs, which offer lower power consumption and tailored performance for specific AI tasks, such as recommendation system.

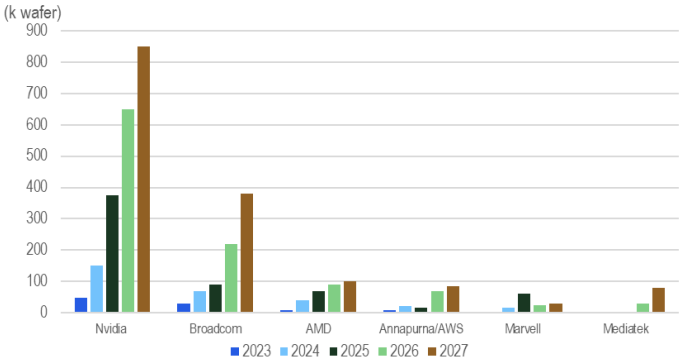
In the ASIC market, Google controls the entire vertical full stack, including data base, TPU hardware, Gemini architecture, datacenter fabric and compiler tool chain, allowing it to co-evolve algorithm and silicon in lockstep. Once a model is trained, this tight integration enables Google to evolve both training and inference within its closed loop. In Google's TPU supply chain, Broadcom continues to share the biggest market share. With Google's commercializing and expanding TPU-based GCP to outside customers, we see upside on TPU family shipment in the longer term, which will likely benefit both Broadcom and Mediatek, with Mediatek as the new entrant in TPU's chip design.

Figure 14. TSMC – CoWoS capacity by technology



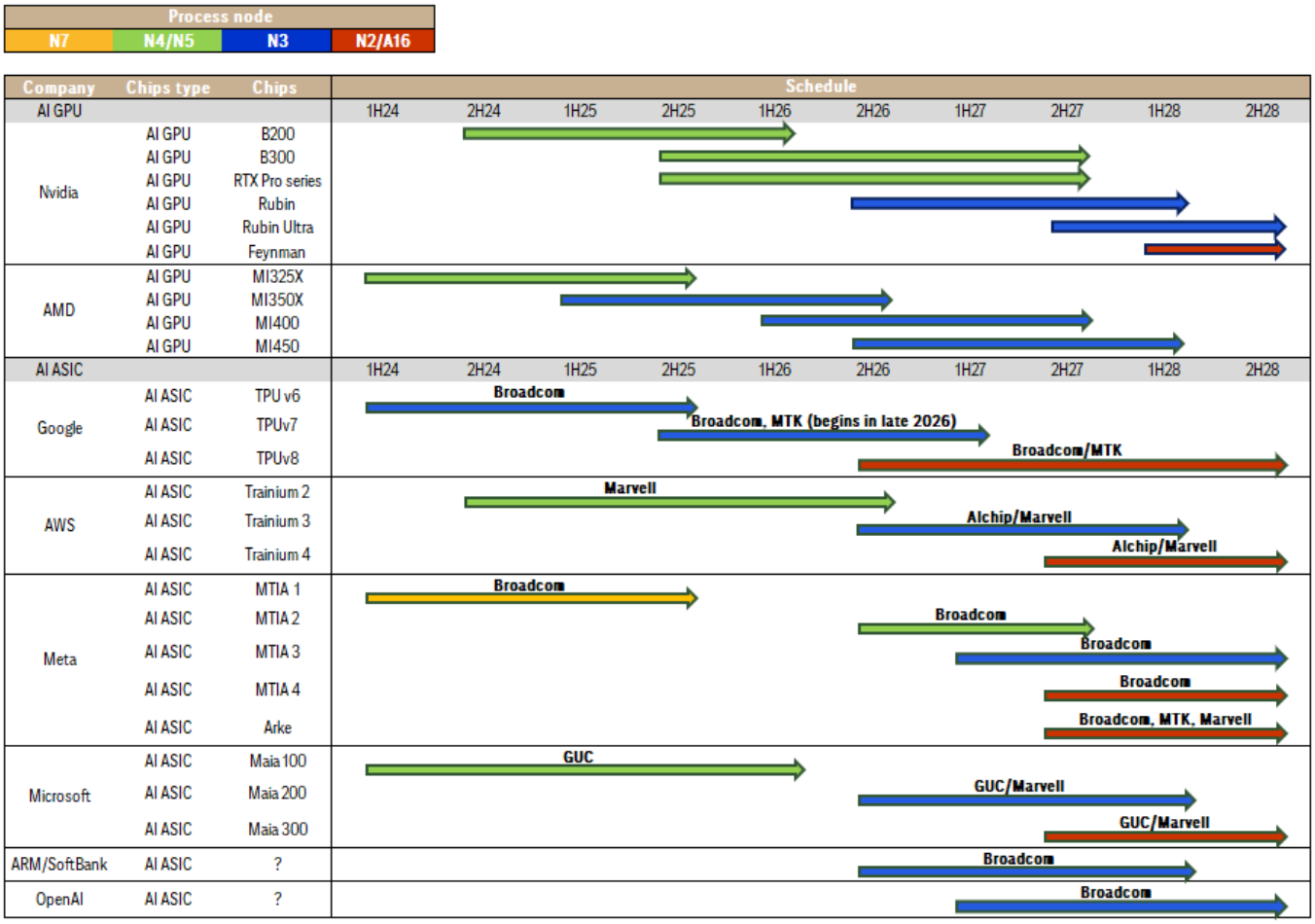
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Source: Citi Research

Figure 15. TSMC – CoWoS capacity by customer



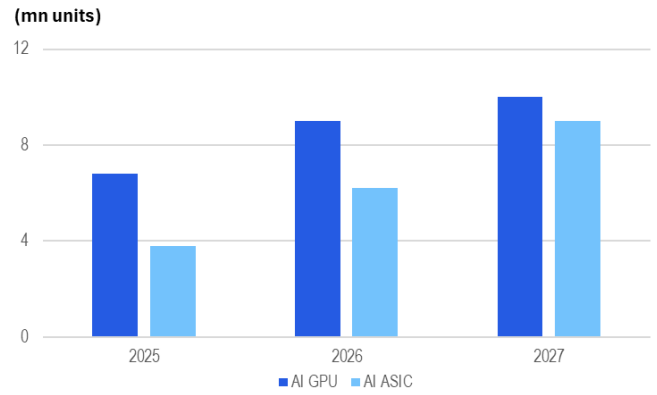
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Source: Citi Research

Figure 16. AI GPU and ASIC roadmap



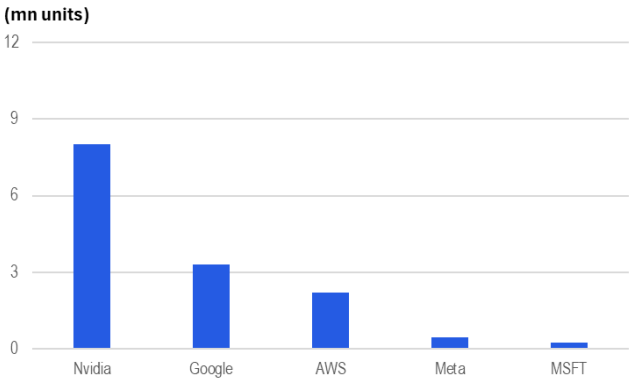
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Source: Citi Research

Figure 17. AI chips shipment trend – AI GPU vs ASIC (2025-27E)



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Source: Citi Research

Figure 18. 2026E key AI GPU/ASIC production planning shipment projection



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Source: Citi Research

Stock implications - Initiate on MPI at Buy/High Risk, reiterate Buy ratings on KYEC and ASEH in advanced packaging

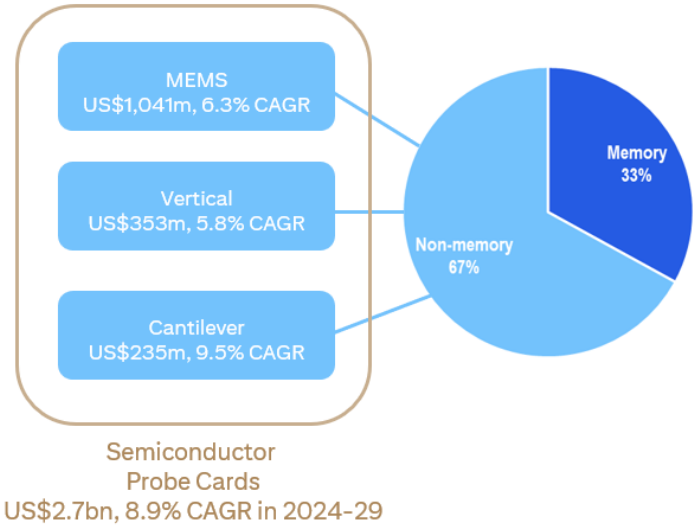
MPI- Benefitting from strong ASIC growth, Probe Card leader with upside in CPO

Company description

Founded in 1995 in Hsinchu, Taiwan, MPI Corporation is aiming to build precision probing system for Taiwan semiconductor testing market. In its early years, the company focused primarily on engineering probers for laboratory and wafer-level characterization - a niche but vital segment that supported IC design companies and research institutes. MPI's precision mechanical know-how positioned it as one of the earliest domestic suppliers capable of producing high accuracy probe stations locally rather than Japan or the US. By early 2000s, MPI had leveraged its precision machinal base to move up the value chain into vertical probe cards, targeting the testing of DRAM and logic devices. MPI also established its in-house PCB processing and substrate assembly lines to ensure quality control and shorten turnaround time. Over time, MPI has become a key local partner for leading OSATs, supporting vertical probe cards used for volume production in memory and SoC testing.

As TSMC developed its CoWoS and advanced packaging since 2010s, wafer level test complexity exploded. MPI made a decisive investment into MEMS probe-card fabrication for sub-50um pitches or multi-ampere current densities required by more advanced SoC. It developed proprietary process for micro-spring and thin-film formation and transformed MPI from a precision-mechanical manufacture into a micro-electromechanical device company- directly competing with global leaders like FormFactor and Technoprobe in the most technology-intensive segment of the testing interface market.

Figure 19. Market value of semiconductor probe card



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Source: Citi Research, MPI

MPI's MEMS production capacity will be reaching 2mn pins per month in 2026, as per the Company, from 1mn per month in 2025 and will be expanding vertical-probes by 10%+ in response of the AI chip demand - fine-pitch and high current multi-die. The company is the largest probe-card and prober supplier. Its revenue by product segments are:

- **Probe Card – 70%+ revenue, including vertical probe card (40%+ of total sales) and rapidly rising contribution from MEMS probe cards (10%+) for AI chips. We expect MEMS probe card will be the growth catalyst thanks to the strong AI chip growth trend.**
- **Engineering Probers and Automation Equipment – 20-25% of revenue; including wafer probers used in RD and engineering, automation modules, thermal chucks and environmental control systems.**
- **Thermal Solution and Others – 5-10% of revenue**

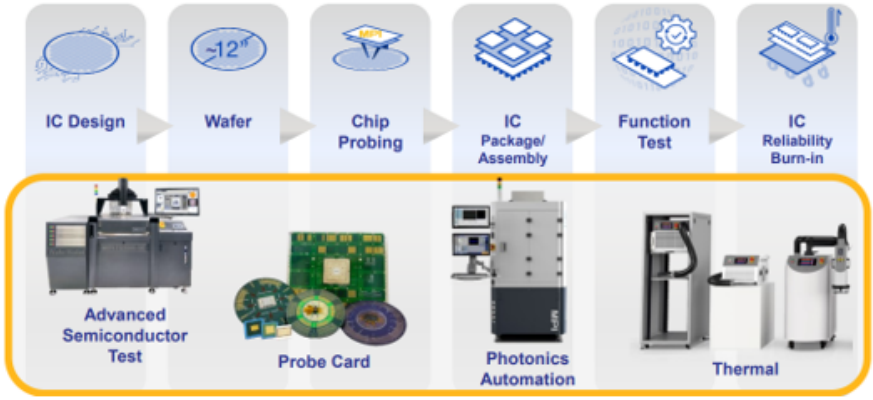
As one of the top five global probe card suppliers, MPI is the only Taiwanese manufacturer capable of producing a full range of probe cards, including Cantilever (CPC), Vertical (VPC), and MEMS-based solutions. This comprehensive technology portfolio addresses high-frequency and fine-pitch testing needs, establishing a strong competitive moat. The company holds the leading market share among Taiwanese VPC manufacturers, and its high-end MEMS probe cards are being integrated into the supply chains of major international clients, with volume production expected after validation in 2025.

In probe cards, VPC (Vertical Probe Card) describes the probe's physical orientation (vertical), while MEMS (Micro-Electro-Mechanical Systems) refers to the advanced microfabrication technology used to create the tiny, precise probes, often integrated into VPCs for high-density testing (Vertical MEMS Probe Cards) for complex logic chips, offering superior signal integrity and fine pitch compared to traditional cantilever cards. With AI chip moving to more advanced node and

complex design, we see the trend that the most advanced, high-density VPCs incorporate MEMS technology for their probes, leading to superior performance. We estimate its current MEMS probe card is about 10-15% of its probe card revenue; with its aggressive expansion and secular growth into 2026, we expect it would contribute more than 30% of its probe card revenue by 2027.

MPI has announced that it will continue expanding probe card and related equipment capacity, focusing on VPC and MEMS probe card, and strengthening its high-frequency measurement and system integration capabilities through overseas acquisition. In addition, it will continue developing its CPO equipment and thermal management devices, with CPO equipment expected to gradually contribute starting from 2026.

Figure 20. MPI's products portfolio



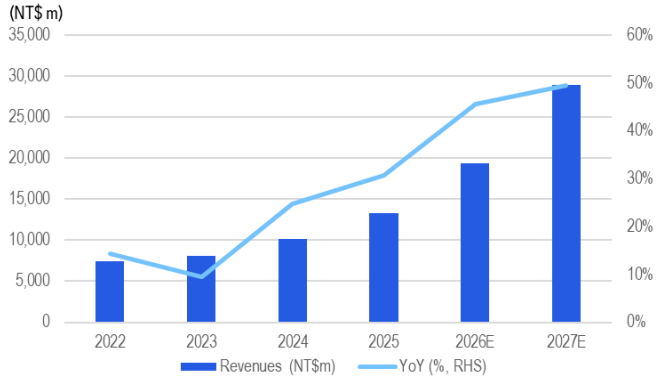
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Source: Citi Research, MPI

Financial Forecast and Outlook

This secular AI trend propelled MPI's revenue to a record NT$13bn in 2025 (30%+ YoY increase), marking the eighth consecutive year of growth. The increasing mix of high-margin VPC and MEMS products — accounting for around 75%+ of probe card revenue — is expected to drive significant profit expansion.

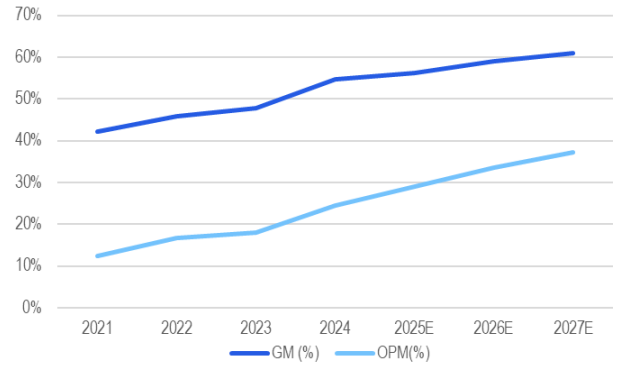
To meet soaring demand, MPI plans to increase its capacity substantially into 2026 in particular for MEMS probe card. The company currently has extended order visibility, and its robust demand is evident in its Book-to-Bill (BB) ratios: VPC is at a strong 1.4-1.5, while CPC is at 0.9-1.0 currently. Additionally, contract liabilities rose by a record 32% YoY and 3% QoQ, reaching 40% of revenue, indicating aggressive pre-payments from customers and solidifying future revenue streams.

Figure 21. MPI – revenues trend



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Source: Citi Research, MPI

Figure 22. MPI – margins trend



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Source: Citi Research, MPI

Rising entry barriers with limited competition

The migration toward heterogenous integration has turned testing into a yield critical process. As we see the trend of rising design complexity of AI accelerators, a single defective die can compromise an entire packaging. We see that the more AI packaging proliferates, the more probe card matters. Each layer of CoWoS or SoIC integration will increase the demand for precision contacts and stable resistance under high-current and frequency operation. During the testing process, the probe card's architecture combined MEMS probes, fine pitch alignment structures and high frequency interconnect substrate. Each design is customized for the target device. Thus, probe card makers need to closely work with the chip makers to ensure the precision at the micro level to ensure the yield of wafer sort stage. We see that the qualification cycle now is over 12 months, and once a probe card is qualified, switching vendors is difficult.

Since probe card design is a long process, engineers must translate the chip's pad layout into a probe architecture. For legacy devices, cantilever or vertical probes would be good enough. But AI chips and HBM demand MSMS probes, these are fabricated in cleanrooms, using lithotherapy and thin-film processes to create miniature springs and beams with micron-level accuracy.

The first technical frontier is pitch scaling. Advanced MEMS probes achieve less than 50um pitch, with roadmaps toward 36um. At this dimension, placement accuracy must be within a micron. Achieving this requires wafer-level fabrication techniques, advanced alignment and precision metrology.

The next would be pin count. A single probe card may host 20k probes. Each must be routed through the probe card substrate with controlled impedance. Electronical design becomes as complex as high speed HDI PCB layout, with crosstalk, reflections and parasitic to manage.

In addition, with data rate exceeding 100Gbps per lane for AI chip connectivity, probes must deliver clean signals. Also, current carrying capability is very critical as well. AI chips drew immerse power during test, sometimes hundreds of amps distributed across thousands of pins. Each probe must maintain low contact resistance to avoid heating, while also surviving millions of cycles without degradation. To note that wafer surfaces are never perfectly flat, and micro bumps vary in height. Probes must deflect elastically, ensuring uniform contact force and

consistent scrub across the array. Achieving this and overcome all these issues, probes require extraordinary uniformity in fabrication.

This approach allows MPI to respond quickly to customer changes in pad layout, bump pitch, or power architecture — an increasingly common occurrence in AI programs. By controlling substrate architecture at the design level, MPI can co-optimize signal routing, contact structures, and mechanical compliance without waiting for third-party redesign cycles. The reports frame this agility as a competitive advantage, particularly in Taiwan's fast-moving advanced packaging ecosystem.

Internal substrate design and manufacture capability

The relevance of substrate capability is becoming more pronounced as test flows move closer to packaging decisions. MPI's substrate expertise strengthens its position as a system-level test interface provider, rather than a component supplier. This capability supports deeper customer engagement, longer design cycles, and higher switching costs — particularly important as test interfaces become increasingly custom and program-specific. MPI has its internal substrate design and capacity, its substrate capability underpins MPI's probe card and advanced test solutions by enabling high-density, high-speed, and mechanically precise interfaces required for AI chips and advanced packaging. While not a standalone revenue driver, it is a critical enabler that enhances MPI's competitiveness, responsiveness, and strategic positioning in an increasingly complex semiconductor testing landscape.

Robust customer base

MPI's customers base is dominated by AI ASIC and CoWoS ecosystem leaders, including Broadcom, Marvell, TSMC and ASE/SPIL. MPI has the advantage of regional service networks when customers require local refurbishment within hours compared to its global peers like FormFactor and Technoprobe.

In TSMC's CoWoS and advanced packaging flow, each die must be pre-qualified before integration. Wafer sorting, which is the process that uses probe card to screen die before packaging. The probe card, prober and tester determine not only throughput but the economic viability of advanced packaging itself

Probe cards have become the essential yield gatekeepers for AI chip, in particular with a big die and expensive chip. Its function seems simple - connect a tester to a wafer - but its execution borders on the extraordinary. Every test involved thousands of synchronized micro-contacts that must press against extremely thin pads, deliver uniform force and transmit signals without distortion.

MPI is one of the only few players able to deliver the precision and scale required. MPI is not merely a probe-card vendors, it has also evolved into a strategic infrastructure partner for the AI era - integrating MEMS engineering, substrate know-how and testing system co-development with its foundry and OSAT partners. MPI has invested aggressively in MEMS technology, in house substrate manufacturing and automation. This vertical integration allowed it to shorten lead time and customize probe card for its customers and foundry/OSAT partners evolving packaging flows.

The company's strategy has relied on its early insight that advanced packaging would migrate testing closer to wafer level. Instead of treating probe card as commodity and consumables, MPI positioned itself as precision instruments co-developed with the foundry. Its portfolio covers three domains:

1. **Vertical probe card** - for memory and SoC testing
2. **MEMS probe card** - for logic and HBM AI applications
3. **Probers and thermal solution** - integrating environmental control for wafer sort.

   The transition from mechanical to MEMS-based probe represents a generational leap. Traditional cantilever probes were limited to pitches of 80um; MEMS processes allow 36-45 um, enabling contact with HBM micro bumps. These MEMS structures are fabricated using semiconductor lithography, ensuring uniform spring constraints and predictable compliance.

We see that the company's rise parallels the structural transformation, from packaging performance to testing interface precision defining competitiveness. As AI ASIC also emerges following GPUs, the demand for probe card and sockets has become a secular growth driver.

As the new AI chips are entering a new arena with more advanced node like N3/2 starting from 2026, these new chips would introduce a new topology of contacts, power rails and I/O configurations. Hence, we see probe card which once served 500-1,000 pins for consumer chips, are now facing more than 10x contacts, carrying current densities orders of higher magnitude. Socket designs at the package level must sustain 100A currents, terabit data rates and continuous thermal stress. The AI shifts have effectively elevated testing interfacing probe card, socket and load board. The trend is thus benefiting MPI as the testing ecosystem has become more demanding on precision and yield assurance.

When a semiconductor wafer is complete at the fab, the first safeguard comes at **wafer sort.** At this stage, the robe card serves as the delicate bridge between the tester and the wafer. Thousands of microscopic MEMS probes touch down simultaneously on the wafer's pad or bumps. The tester injects signals, current flows, and the prober ensure precise alignment. This process determines which dies qualify as **Known Good Dies (KGD).** Without the probe card, the risk is that defective dies slip through, leading to catastrophic losses once they enter costly CoWoS or SoIC packaging.

Once dies are packaged, the probe card steps aside. In its place, the testing socket becomes the critical interface. Unlike the probe card, which tests bare dies, the socket grips a finished package and connects it to automated test equipment. Here, the object shifts: the chip is validated for **functional performance, I/O integrity and the speed at full operating conditions.** In other words, probe card ensures die quality, socket ensure packaging reliability.

Finally, some AI chips advanced to system-level-test (SLT). In burn-in racks or emulation systems, devices are stressed under real world conditions. While sockets and load boards still act as intermediaries, the goal here is not to probe individual connections but to verify that the device behaves correctly as part of a larger system.

Equipment business - potential rising start with CPO taking off

While probe card and related interfaces account for the majority of MPI's revenue, the equipment business is a stable, technology-driven contributor, typically associated with early-stage validation, RF characterization, and advanced device development rather than high-volume manufacturing. The equipment business currently contributes roughly mid-teens percentage of its revenue; it is centered on probe station, RF/microwave test platforms and thermal control system. These tools are not positioned as direct competitors to large scale automated test equipment vendors; instead, they sit upstream and adjacent - used when devices are still being electrically, thermally and mechanically characterized at the wafer or early package level.

It is also worth noting that MPI's equipment strength lies in high-frequency and high precision environment, particularly where signal integrity, contract stability and temperature control must be tightly managed. This includes mmWave, SerDes, RF front-end and increasingly, heterogeneous integration and chiplet-based architecture. The equipment business is more tied to engineering engagement rather than procurement cycles as it allows MPI to engage its probe card customers in earlier stage.

CPO could be the new catalyst for MPI

Co-Packaged Optics (CPO) represents a structural shift in how high-speed interconnects are designed, assembled, and tested. By integrating optical engines directly alongside switch ASICs or AI processors within the same package, CPO eliminates traditional pluggable modules but introduces unprecedented challenges in electrical-optical co-validation, thermal coupling, and yield learning. Testing in this environment is no longer purely electrical, nor purely optical—it becomes a hybrid, multi-physics problem.

This shift fundamentally benefits companies with strength in RF probing, high-frequency signal integrity, precision alignment, and thermal control, rather than those focused solely on digital functional test. Traditional test flows - where optics are validated separately from logic silicon - are insufficient once optical engines and logic dies are co-located under a shared thermal and mechanical environment. As a result, testing increasingly migrates toward wafer-level and early package-level characterization, where MPI's equipment portfolio is precisely most relevant.

MPI's Opportunity in CPO: Where Equipment Matters Most

MPI's opportunity in CPO lies less in volume manufacturing and more in enabling the ecosystem during development, qualification, and early deployment. CPO systems require extremely accurate probing of high-speed electrical lanes (often >112G SerDes), alongside precise thermal control to replicate real operating conditions. MPI's RF probe stations and thermal platforms are well-suited for this task, as they allow engineers to correlate electrical performance degradation with temperature, alignment, and packaging stress.

Moreover, CPO architectures demand tight co-optimization between chip, package, and optical module. This increases demand for customized test setups, rather than standardized, high-throughput handlers. MPI's historical strength in customization - serving advanced research labs, IDMs, and leading foundries - aligns well with this need. As CPO designs remain non-standard and vendor-specific, test equipment that can adapt quickly becomes a competitive advantage.

Another important dimension is MPI's ecosystem adjacency. CPO development is driven by hyperscalers, switch ASIC vendors, and advanced packaging houses working closely with foundries. MPI's footprint in Taiwan and Asia places it close to TSMC-centric advanced packaging development, where CPO-related test challenges are being addressed in parallel with CoWoS, SoIC, and chiplet integration. This proximity increases the likelihood that MPI's equipment is specified during early validation phases, even if final volume testing later transitions to other platforms.

From a strategic perspective, MPI's equipment business provides optionality rather than immediate scale. CPO volumes will remain limited in the near term, but engineering intensity and ASP per tool are high, supporting attractive margins even at modest unit shipments. More importantly, early engagement through equipment creates technical lock-in, positioning MPI to influence downstream interface design—including probe cards, sockets, and custom interposers—as CPO moves toward broader adoption. In this sense, MPI's equipment business should be viewed as a strategic enabler of future probe card and interface demand, particularly in next-generation AI and networking architectures where testing shifts earlier, becomes more complex, and spans electrical, optical, and thermal domains simultaneously.

Valuation and Risks - Initiate on MPI at Buy/High Risk with TP NT$2,800

We initiate on MPI at Buy/High Risk and set up our MPI's valuation and target price based on the thesis that the company has transitioned from a cyclical probe card supplier to a structural beneficiary of AI-driven test complexity. We are looking for 77% and 64% earnings growth in 2026 and 2027. The company trades at a PER range of 10-45x in the past 3 years. With the promising growth from AI chip, we set our target PER target of 37x at the high-end of its historical PER to the average of our 2026-27 EPS estimates. Our target price is set at NT$2,800.

Despite its premium valuation, accelerating AI ASIC to drive further upside

MPI has currently been trading at c30x PER to 2026-27E EPS average. We acknowledge the shares have seen a very strong performance, more than quadrupling since April 2025. That said, we expect the stock to still be able to trade higher toward our TP of NT$2,800 since we believe its aggressive MEMS expansion, expanding margins on improving mix and strong development in AI ASIC probe card market should drive a strong sales CAGR of 48% and earnings CAGR of 70% in 2025-27E. While near-term volatility remains possible, the target price framework embedded in the reports assumes MPI's earnings power remains structurally higher than that in the previous cycles, supporting a valuation well above historical norms.

Key downside risks that may prevent the stock from achieving our target price

1. **Slowdown in AI demand**: any unexpected slowdown in overall AI market growth may result in a slower project development with key AI customers.
2. **Slower than expected adoption of MEMS probe cards**: slower adoption or expansion of its MEMS business may lead to a slower AI order demand and thus cap margins outlook.
3. **Intensifying competition from global and regional peers**: any unexpectedly intensified competition may lead to some downside to its market share position in its new project development with key AI customers.
4. **Slow development in CPO equipment business**: while not much contribution for MPI now, any slower development for MPI in CPO market may cap the stock from further re-rating potentials.

While MPI's premium multiple, earnings volatility or short-term order fluctuations could lead to disproportionate share price reactions, MPI's deep integration into customer test flows and its exposure to advanced packaging reduces the risk of abrupt demand collapse, even in softer macro environments.

Figure 23. MPI – Citi Estimates vs. Consensus

	2025E			2026E			2027E		
(NT$mn)	Citi	Con.	Diff.	Citi	Con.	Diff.	Citi	Con.	Diff.
Sales	13,287	13,097	1%	19,347	18,917	2%	28,910	23,458	23%
Gross profit	7,467	7,353	2%	11,404	11,047	3%	17,599	13,942	26%
Operating profit	3,849	3,807	1%	6,471	6,259	3%	10,749	8,330	29%
Net income	3,140	3,058	3%	5,526	5,311	4%	9,077	7,102	28%
EPS (NT$)	32.13	32.47	-1%	56.74	55.79	2%	93.20	75.00	24%
Gross margin	56.2%	56.1%	+0.1 ppt	58.9%	58.4%	+0.5 ppt	60.9%	59.4%	+1.4 ppt
Operating margin	29.0%	29.1%	-0.1 ppt	33.4%	33.1%	+0.4 ppt	37.2%	35.5%	+1.7 ppt
Net margin	23.6%	23.3%	+0.3 ppt	28.6%	28.1%	+0.5 ppt	31.4%	30.3%	+1.1 ppt

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Source: Citi Research, Bloomberg

Figure 24. MPI - financial forecast summary

	2024				2025				2026							
(NT$ in Mn, year-end Dec)	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4QE	1QE	2QE	3QE	4QE	2024	2025E	2026E	2027E
Revenue	2,047	2,393	2,729	3,003	2,829	3,293	3,414	3,752	3,766	4,455	5,249	5,878	10,172	13,287	19,347	28,910
COGS	-1,021	-1,093	-1,182	-1,315	-1,205	-1,374	-1,591	-1,650	-1,563	-1,795	-2,191	-2,395	-4,611	-5,820	-7,943	-11,311
Depreciation costs	-76	-78	-80	-85	-90	-103	-122	-153	-169	-187	-212	-243	-319	-468	-812	-1,175
Gross Profit	1,026	1,300	1,547	1,688	1,623	1,919	1,822	2,102	2,203	2,660	3,058	3,483	5,561	7,467	11,404	17,599
Operating Expense	-639	-702	-802	-935	-783	-840	-927	-1,068	-972	-1,059	-1,334	-1,568	-3,078	-3,617	-4,933	-6,849
SG&A expenses	-423	-458	-492	-600	-508	-530	-605	-694	-620	-650	-852	-999	-1,973	-2,337	-3,121	-4,225
R&D expenses	-217	-250	-286	-336	-269	-318	-328	-375	-346	-417	-489	-570	-1,089	-1,290	-1,822	-2,634
EBIT	387	598	745	753	840	1,079	896	1,034	1,231	1,601	1,724	1,915	2,483	3,849	6,471	10,749
Net Interest Income	1	5	-1	4	-6	7	-9	4	-6	7	-9	4	9	-4	-4	-4
Net Other Income	95	82	27	99	54	-330	166	48	46	47	47	48	303	-62	188	188
Pre-Tax Profit	482	684	772	856	888	756	1,053	1,086	1,270	1,655	1,762	1,967	2,795	3,783	6,655	10,933
Tax	-86	-142	-121	-142	-162	-126	-176	-180	-232	-276	-294	-327	-490	-644	-1,129	-1,856
Net Profit	398	543	651	714	727	631	877	906	1,039	1,379	1,468	1,641	2,306	3,140	5,526	9,077
EPS (NT$)	4.22	5.76	6.91	7.58	7.71	6.69	9.30	9.61	11.02	14.62	15.57	17.40	24.44	32.13	56.74	93.20
Revenue breakdown																
Probe card	57%	56%	59%	58%	65%	74%	72%	71%	72%	74%	75%	77%	57%	71%	75%	79%
Equipment	32%	30%	30%	33%	25%	23%	21%	23%	23%	21%	20%	19%	31%	23%	20%	18%
Others	11%	14%	11%	9%	10%	3%	7%	6%	5%	5%	5%	4%	11%	6%	5%	3%
Margins (%)																
Gross Margin	50.1%	54.3%	56.7%	56.2%	57.4%	58.3%	53.4%	56.0%	58.5%	59.7%	58.3%	59.3%	54.7%	56.2%	58.9%	60.9%
Operating Margin	18.9%	25.0%	27.3%	25.1%	29.7%	32.8%	26.2%	27.6%	32.7%	35.9%	32.9%	32.6%	24.4%	29.0%	33.4%	37.2%
Net Margin	19.4%	22.7%	23.9%	23.8%	25.7%	19.2%	25.7%	24.1%	27.6%	30.9%	28.0%	27.9%	22.7%	23.6%	28.6%	31.4%
Sequential Growth (%)																
Revenue	-7%	17%	14%	10%	-6%	16%	4%	10%	0%	18%	18%	12%	25%	31%	46%	49%
Gross Profit	-2%	27%	19%	9%	-4%	18%	-5%	15%	5%	21%	15%	14%	43%	34%	53%	54%
EBIT	10%	55%	25%	1%	12%	28%	-17%	15%	19%	30%	8%	11%	69%	55%	68%	66%
Net Profit	43%	37%	20%	10%	2%	-13%	39%	3%	15%	33%	6%	12%	75%	36%	76%	64%
EPS	43%	37%	20%	10%	2%	-13%	39%	3%	15%	33%	6%	12%	76%	31%	77%	64%

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Source: Citi Research, Bloomberg

Figure 25. MPI – valuation comparison with peers

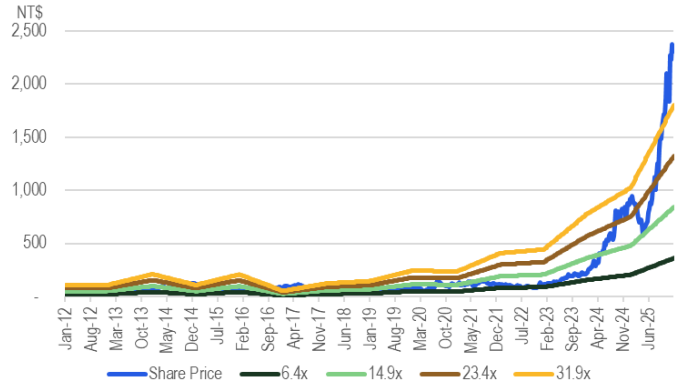
Ticker	Company	Rating	Price 2026/1/8		Mkt Cap (US$m)	EPS (local Currency) 2026	EPS (local Currency) 2027	P/E (x) 2026	P/E (x) 2027	P/B (x) 2026	P/B (x) 2027	ROE (%) 2026	ROE (%) 2027	Dividend Yield(%) 2026	Dividend Yield(%) 2027	EPS Growth (%) 2026	EPS Growth (%) 2027
6223.TW	**MPI**	**1H**	**TWD**	**2,120**	**6,391**	**56.7**	**93.2**	**37.4**	**22.7**	**11.6**	**7.6**	**37.9**	**41.5**	**1.6**	**2.1**	**76.6**	**64.3**
6515.TW	WinWay	NR	TWD	3,175	3,623	68.5	91.4	46.3	34.7	15.7	12.3	37.2	38.3	1.6	3.0	51.7	33.4
6510.TW	CHPT	NR	TWD	2,190	2,274	43.2	72.1	50.7	30.4	7.1	4.6	15.4	18.8	0.9	1.7	53.2	66.8
2360.TW	Chroma	1	TWD	925	12,491	25.1	32.2	36.8	28.7	10.9	22.5	31.7	35.1	2.0	1.0	35.8	2.2
7769.TW	Hon Precision	NR	TWD	3,130	17,832	99.1	127.8	31.6	24.5	11.7	9.2	50.5	45.7	2.1	2.8	34.1	29.0
3131.TW	GPTC	NR	TWD	1,830	1,693	57.6	74.9	31.8	24.4	9.0	7.4	32.6	34.0	2.2	2.7	49.6	30.1
FORM.US	Formfactor	1	USD	63	4,862	1.8	n.m.	35.5	n.m.	4.3	7.5	8.1	n.m.	-	-	51.5	n.m.
TPRO.IM	Technoprobe	NR	EUR	14	10,483	0.3	0.3	54.7	40.5	6.1	5.4	11.5	13.8	0.1	0.2	74.3	35.1
Peers average								**39.1**	**27.6**	**11.0**	**10.6**	**34.2**	**35.6**	**1.7**	**2.2**	**50.2**	**37.6**

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Note – Bloomberg consensus for non-rated (NR) stocks

Source: Citi Research, Bloomberg

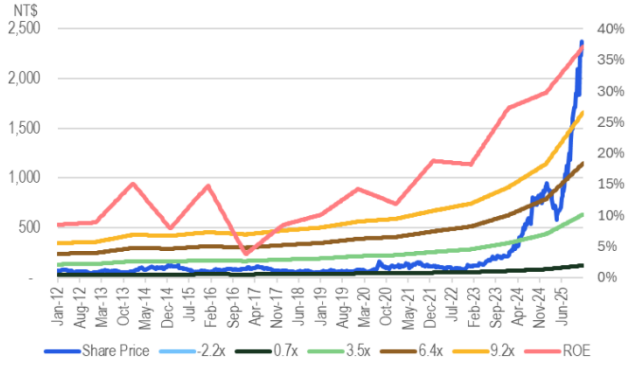
Figure 26. MPI – PE band



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Source: Citi Research

Figure 27. MPI – PB band & ROE trend



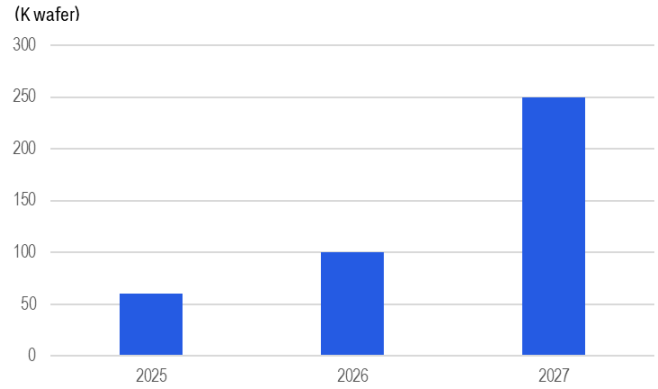
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Source: Citi Research

ASEH- Leading edge advanced packaging and wafer testing lead more earnings upside

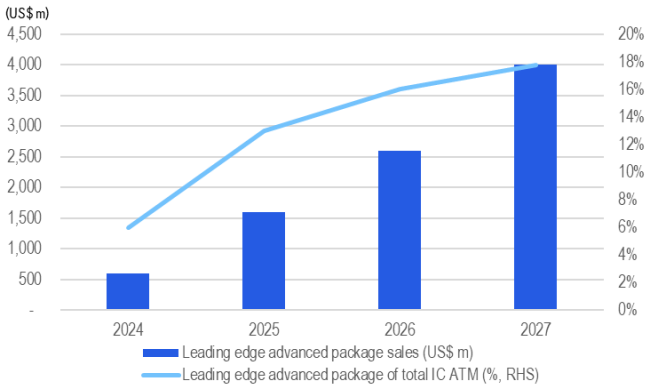
ASEH guided US$1.6bn revenue from leading edge advanced packaging in 2025 and expect it to reach US$2.6bn in 2026. With TSMC's continuous oS process outsourcing and more of the wafer sorting/probing testing service, we expect there is a higher chance that the company's leading edge advanced packaging revenue can be over US$4bn in 2027.

Figure 28. ASEH – CoWoS capacity (oS) and FoCoS capacity



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Source: Citi Research

Figure 29. ASEH – leading edge advanced package revenues



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Source: Citi Research

While leading edge advanced packaging provides higher ASP and margin accretive upside, we also note that its overall UTR has been supported due to much larger die size. Other than AI chip, ASEH also benefits from better pricing environment and remaining resilient demand outlook. We thus expect ASEH to provide positive guidance during its earnings call in late-Jan 2026.

We revise up our 2026/2027 earnings projection for ASEH by 9%/32% anticipating robust GM recovery trend thanks to higher ASP and secular AI and leading edge advanced packaging growth. Its EMS business would also be supported by resilient order flow from Apple in the near term. With better visibility on AI demand and structural earnings trajectory, we lift our target price to NT$340 which is derived using a DCF methodology. Our target price implies 23x and 16x to our 2026 and 2027 EPS; reiterate Buy.

Figure 30. ASEH – Estimates Revisions

	2025E			2026E			2027E		
(NT$mn)	New	Old	Chg.	New	Old	Chg.	New	Old	Chg.
Sales	642,022	642,022	0%	701,929	738,738	-5%	908,869	825,542	10%
YoY growth	8%	8%		9%	15%		29%	12%	
Gross profit	110,880	110,880	0%	139,569	136,439	2%	191,311	155,676	23%
Opex	62,974	62,974	0%	64,741	68,145	-5%	85,168	77,359	10%
Operating profit	47,906	47,906	0%	74,829	68,293	10%	106,143	78,318	36%
Pre-tax profit	49,056	49,056	0%	82,594	75,970	9%	117,748	89,807	31%
Net income	38,457	38,457	0%	65,641	60,308	9%	94,128	71,532	32%
EPS (NT$)	8.88	8.88	0%	15.15	13.92	9%	21.72	16.51	32%
Gross margin	17.3%	17.3%	0.0 ppt	19.9%	18.5%	+1.4 ppt	21.0%	18.9%	+2.2 ppt
Opex ratio	9.8%	9.8%	0.0 ppt	9.2%	9.2%	-0.0 ppt	9.4%	9.4%	+0.0 ppt
Operating margin	7.5%	7.5%	0.0 ppt	10.7%	9.2%	+1.4 ppt	11.7%	9.5%	+2.2 ppt
Net margin	6.0%	6.0%	0.0 ppt	9.4%	8.2%	+1.2 ppt	10.4%	8.7%	+1.7 ppt

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Source: Citi Research

Figure 31. ASEH – Citi Estimates vs. Consensus

	2025E			2026E			2027E		
(NT$mn)	Citi	Con.	Diff.	Citi	Con.	Diff.	Citi	Con.	Diff.
Sales	642,022	639,844	0%	701,929	728,755	-4%	908,869	823,189	10%
Gross profit	110,880	110,015	1%	139,569	139,666	0%	191,311	168,466	14%
Operating profit	47,906	47,922	0%	74,829	72,591	3%	106,143	91,904	15%
Net income	38,457	38,396	0%	65,641	58,346	13%	94,128	73,718	28%
EPS (NT$)	8.88	8.72	2%	15.15	13.18	15%	21.72	16.62	31%
Gross margin	17.3%	17.2%	+0.1 ppt	19.9%	19.2%	+0.7 ppt	21.0%	20.5%	+0.6 ppt
Operating margin	7.5%	7.5%	-0.0 ppt	10.7%	10.0%	+0.7 ppt	11.7%	11.2%	+0.5 ppt
Net margin	6.0%	6.0%	-0.0 ppt	9.4%	8.0%	+1.3 ppt	10.4%	9.0%	+1.4 ppt

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Source: Citi Research, Bloomberg estimates

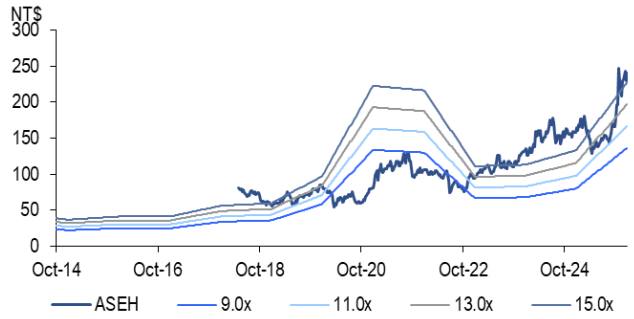
Figure 32. ASEH - financial forecast summary

	2024				2025				2026							
(NT$ in Mn, year-end Dec)	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4QE	1QE	2QE	3QE	4QE	2024	2025E	2026E	2027E
Revenue	132,803	140,238	160,105	162,264	148,153	150,750	168,569	174,550	155,165	162,531	177,104	207,129	595,410	642,022	701,929	908,869
COGS	-111,982	-117,184	-133,673	-135,639	-123,261	-125,063	-139,692	-143,127	-125,733	-130,207	-140,765	-165,655	-498,478	-531,142	-562,360	-717,557
Gross Profit	20,821	23,054	26,432	26,625	24,893	25,688	28,877	31,423	29,432	32,324	36,339	41,474	96,932	110,880	139,569	191,311
Operating Expense	-13,344	-14,046	-14,956	-15,420	-15,221	-15,494	-15,676	-16,582	-13,965	-14,628	-16,471	-19,677	-57,765	-62,974	-64,741	-85,168
SG&A expenses	-6,998	-7,203	-7,780	-8,007	-7,905	-7,750	-8,112	-8,108	-7,235	-7,567	-8,223	-9,574	-29,988	-31,876	-32,599	-43,970
R&D expenses	-6,609	-7,106	-7,439	-7,676	-7,579	-8,004	-7,826	-8,727	-6,982	-7,314	-8,501	-10,356	-28,830	-32,137	-33,154	-42,209
EBIT	7,477	9,008	11,476	11,205	9,671	10,193	13,201	14,841	15,467	17,696	19,869	21,797	39,166	47,906	74,829	106,143
Net Interest Income	-1,115	-1,172	-1,336	-1,342	-1,309	-1,310	-670	-1,074	-1,222	-1,196	-1,199	-1,198	-4,965	-4,363	-4,816	-5,255
Net Other Income	1,450	2,269	2,120	1,644	1,448	371	1,446	2,248	2,514	3,366	3,621	3,080	7,482	5,513	12,581	16,860
Pre-Tax Profit	7,812	10,105	12,260	11,506	9,810	9,254	13,976	16,015	16,759	19,866	22,290	23,679	41,683	49,056	82,594	117,748
Tax	1,893	1,950	2,054	1,861	2,022	1,576	2,615	3,203	2,514	4,172	4,458	4,736	-7,758	-9,416	-15,880	-22,535
Net Profit to Parent	5,660	7,778	9,666	9,378	7,554	7,521	10,870	12,512	13,992	15,432	17,566	18,651	32,482	38,457	65,641	94,128
EPS (NT$)	1.31	1.80	2.24	2.17	1.75	1.74	2.51	2.89	3.23	3.56	4.05	4.30	7.52	8.88	15.15	21.72
Margins (%)																
Gross Margin	15.7	16.4	16.5	16.4	16.8	17.0	17.1	18.0	19.0	19.9	20.5	20.0	16.3	17.3	19.9	21.0
Operating Margin	5.6	6.4	7.2	6.9	6.5	6.8	7.8	8.5	10.0	10.9	11.2	10.5	6.6	7.5	10.7	11.7
Net Margin	4.3	5.5	6.0	5.8	5.1	5.0	6.4	7.2	9.0	9.5	9.9	9.0	5.5	6.0	9.4	10.4
Sequential Growth (%)																
Revenue	-17.3	5.6	14.2	1.3	-8.7	1.8	11.8	3.5	-11.1	4.7	9.0	17.0	2.3	7.8	9.3	29.5
Gross Profit	-19.2	10.7	14.7	0.7	-6.5	3.2	12.4	8.8	-6.3	9.8	12.4	14.1	5.6	14.4	25.9	37.1
EBIT	-36.7	20.5	27.4	-2.4	-13.7	5.4	29.5	12.4	4.2	14.4	12.3	9.7	-2.9	22.3	56.2	41.8
Net Profit	-39.7	37.4	24.3	-3.0	-19.5	-0.4	44.5	15.1	11.8	10.3	13.8	6.2	2.4	18.4	70.7	43.4
EPS	-40.0	37.3	24.2	-2.9	-19.6	-0.5	44.5	15.1	11.8	10.3	13.8	6.2	1.8	18.0	70.6	43.4

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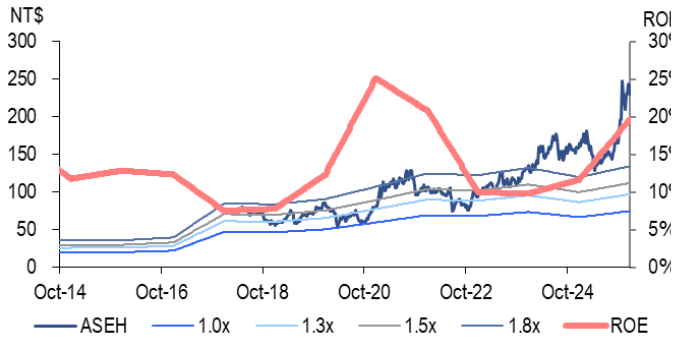
Source: Citi Research, Bloomberg

Figure 33. ASEH – Forward P/E band



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Source: Citi Research, company data

Figure 34. ASEH – Forward P/B band & ROE



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Source: Citi Research, company data

KYEC- Longer testing time + wafer testing opportunity provides more upside

Given KYEC's expertise in final testing and burn-in process, the company has successfully secured Nvidia, Broadcom and Mediatek as its key customers in AI GPU/ASIC. With AI chip continuously migrating to more advanced node with chiplet design and bigger die size, we believe the testing time will be getting longer thus supporting KYEC's better ASP and revenue growth. We expect Nvidia's revenue at KYEC to grow more than 60% and nearly double growth at Broadcom due to low base. With wafer sorting outsourcing from TSMC, we believe it would be able to contribute an incremental c3% increase to its overall revenue.

KYEC has seen substantial capex growth in 2025 and we expect the company to continue to expand more capacity reflecting its customers' strong long term demand outlook. We are looking for 36% and 53% revenue growth in 2026/2027 with 7% and 57% earnings growth. Given longer testing process, we expect KYEC's GM to expand gradually with robust AI chip shipment trend. With its secular growth trend and upside from TPU other than GPU, we lift our target price to NT$330, which is derived using a DCF methodology. Our target price implies 34x and 22x to our 2026 and 2027 EPS; reiterate Buy.

Figure 35. KYEC – Estimates Revisions

	2025E			2026E			2027E		
(NT$mn)	New	Old	Chg.	New	Old	Chg.	New	Old	Chg.
Sales	34,808	35,066	-1%	47,214	49,915	-5%	72,195	70,065	3%
YoY growth	30%	31%		36%	42%		53%	40%	
Gross profit	12,491	12,592	-1%	18,167	19,078	-5%	28,237	27,145	4%
Opex	-3,562	-3,588	-1%	-3,937	-4,300	-8%	-5,645	-5,991	-6%
Operating profit	8,929	9,004	-1%	14,230	14,779	-4%	22,592	21,154	7%
Pre-tax profit	10,448	10,523	-1%	14,668	15,217	-4%	23,030	21,592	7%
Net income	11,039	11,101	-1%	11,862	12,304	-4%	18,631	17,459	7%
EPS (NT$)	8.97	9.02	-1%	9.65	10.01	-4%	15.15	14.20	7%
Gross margin	35.9%	35.9%	-0.0 ppt	38.5%	38.2%	+0.3 ppt	39.1%	38.7%	+0.4 ppt
Opex ratio	-10.2%	-10.2%	-0.0 ppt	-8.3%	-8.6%	+0.3 ppt	-7.8%	-8.6%	+0.7 ppt
Operating margin	25.7%	25.7%	-0.0 ppt	30.1%	29.6%	+0.5 ppt	31.3%	30.2%	+1.1 ppt
Net margin	31.7%	31.7%	+0.1 ppt	25.1%	24.6%	+0.5 ppt	25.8%	24.9%	+0.9 ppt

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Source: Citi Research

Figure 36. KYEC – Citi Estimates vs. Consensus

	2025E			2026E			2027E		
(NT$mn)	Citi	Con.	Diff.	Citi	Con.	Diff.	Citi	Con.	Diff.
Sales	34,808	34,967	0%	47,214	47,954	-2%	72,195	62,841	15%
Gross profit	12,491	12,491	0%	18,167	18,568	-2%	28,237	25,423	11%
Operating profit	8,929	8,986	-1%	14,230	14,262	0%	22,592	19,267	17%
Net income	11,039	11,101	-1%	11,862	11,904	0%	18,631	16,023	16%
EPS (NT$)	8.97	8.85	1%	9.65	9.70	0%	15.15	13.07	16%
Gross margin	35.9%	35.7%	+0.2 ppt	38.5%	38.7%	-0.2 ppt	39.1%	40.5%	-1.3 ppt
Operating margin	25.7%	25.7%	-0.0 ppt	30.1%	29.7%	+0.4 ppt	31.3%	30.7%	+0.6 ppt
Net margin	31.7%	31.7%	-0.0 ppt	25.1%	24.8%	+0.3 ppt	25.8%	25.5%	+0.3 ppt

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Source: Citi Research, Bloomberg estimates

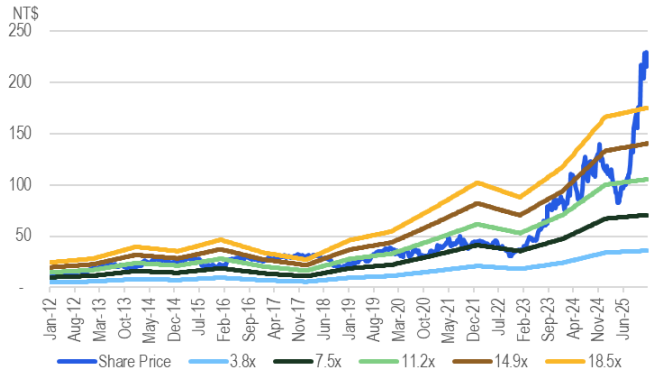
Figure 37. KYEC – financial forecast summary

KYEC	2024				2025				2026							
(NT$ in Mn, year-end Dec)	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4QE	1QE	2QE	3QE	4QE	2024	2025E	2026E	2027E
Revenue	5,977	6,543	7,039	7,297	7,315	8,362	9,291	9,840	9,508	10,649	12,573	14,484	26,856	34,808	47,214	72,195
COGS	-4,004	-4,236	-4,512	-4,760	-4,865	-5,390	-5,944	-6,118	-5,909	-6,616	-7,727	-8,794	-17,512	-22,317	-29,047	-43,958
Depreciation costs	-2,093	-892	-1,423	-1,456	-1,506	-1,621	-1,746	-2,085	-2,310	-2,503	-2,662	-2,885	-5,865	-6,958	-10,360	-12,720
Gross Profit	1,973	2,307	2,527	2,537	2,450	2,972	3,347	3,722	3,599	4,033	4,846	5,689	9,344	12,491	18,167	28,237
Operating Expense	-669	-711	-759	-1,033	-928	-795	-855	-984	-903	-903	-1,001	-1,130	-3,172	-3,562	-3,937	-5,645
SG&A expenses	-463	-508	-536	-810	-685	-583	-619	-689	-666	-636	-712	-797	-2,316	-2,576	-2,811	-3,941
R&D expenses	-206	-203	-223	-223	-243	-212	-236	-295	-238	-266	-289	-333	-855	-986	-1,126	-1,704
EBIT	1,304	1,596	1,768	1,504	1,523	2,176	2,492	2,738	2,696	3,130	3,845	4,560	6,172	8,929	14,230	22,592
Net Interest Income	-112	-76	-95	-80	-11	144	-11	-11	25	25	24	24	-362	111	98	98
Net Other Income	78	-144	162	65	618	338	405	48	84	85	85	86	162	1,408	340	340
Pre-Tax Profit	1,271	1,377	1,835	1,489	2,129	2,658	2,886	2,775	2,805	3,240	3,954	4,670	5,972	10,448	14,668	23,030
Tax	-257	-214	-379	-361	-850	-483	-584	-499	-561	-589	-800	-841	-1,211	-2,416	-2,790	-4,383
Net Profit	1,369	1,903	2,478	2,030	4,290	2,175	2,302	2,271	2,240	2,648	3,150	3,825	7,779	11,039	11,862	18,631
EPS (NT$)	1.11	1.55	2.02	1.65	3.48	1.77	1.87	1.85	1.82	2.15	2.56	3.11	6.34	8.97	9.65	15.15
Margins (%)																
Gross Margin	33.0%	35.3%	35.9%	34.8%	33.5%	35.5%	36.0%	37.8%	37.9%	37.9%	38.5%	39.3%	34.8%	35.9%	38.5%	39.1%
Operating Margin	21.8%	24.4%	25.1%	20.6%	20.8%	26.0%	26.8%	27.8%	28.4%	29.4%	30.6%	31.5%	23.0%	25.7%	30.1%	31.3%
Net Margin	22.9%	29.1%	35.2%	27.8%	58.6%	26.0%	24.8%	23.1%	23.6%	24.9%	25.1%	26.4%	29.0%	31.7%	25.1%	25.8%
Sequential Growth (%)																
Revenue	-30%	9%	8%	4%	0%	14%	11%	6%	-3%	12%	18%	15%	-19%	30%	36%	53%
Gross Profit	-31%	17%	10%	0%	-3%	21%	13%	11%	-3%	12%	20%	17%	-16%	34%	45%	55%
EBIT	-33%	22%	11%	-15%	1%	43%	15%	10%	-2%	16%	23%	19%	-16%	45%	59%	59%
Net Profit	-13%	39%	30%	-18%	111%	-49%	6%	-1%	-1%	18%	19%	21%	33%	42%	7%	57%
EPS	-13%	39%	30%	-18%	111%	-49%	6%	-1%	-1%	18%	19%	21%	34%	42%	8%	57%

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Source: Citi Research, Bloomberg

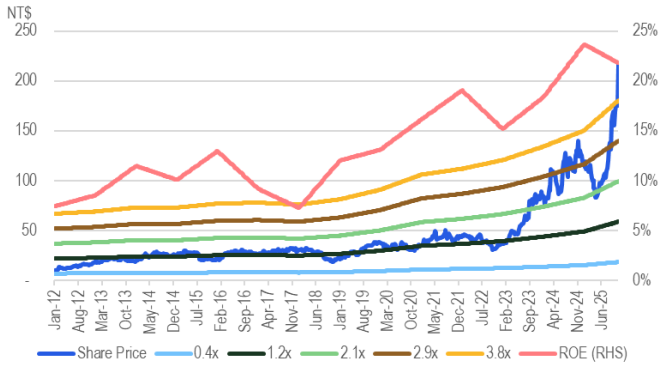
Figure 38. KYEC – Forward P/E band



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Source: Citi Research, company data

Figure 39. KYEC – Forward P/B band & ROE



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Source: Citi Research, company data

Companies Mentioned:
King Yuan Electronics Co (2449.TW; NT$263.5; 1; 09 Jan 26; 13:30)
MPI (6223.TWO; NT$2230.0; 1H; 09 Jan 26; 15:00)
ASE Technology Holding (3711.TW; NT$272.0; 1; 09 Jan 26; 13:30)
Advanced Micro Devices (AMD.O; US$204.68; 2; 08 Jan 26; 16:00)
Advantest (6857.T; ¥20255.0; 1; 09 Jan 26; 15:30)
Alchip (3661.TW; NT$3570.0; 1; 09 Jan 26; 13:30)
Alphabet Inc (GOOGL.O; US$325.44; 1; 08 Jan 26; 16:00)
Amazon.com, Inc. (AMZN.O; US$246.29; 1; 08 Jan 26; 16:00)
Apple, Inc. (AAPL.O; US$259.04; 1; 08 Jan 26; 16:00)
Arm Holdings PLC (ARM.O; US$113.08; 1; 08 Jan 26; 16:00)
Broadcom Inc (AVGO.O; US$332.48; 1; 08 Jan 26; 16:00)
Chroma ATE (2360.TW; NT$923.0; 1; 09 Jan 26; 13:30)
FormFactor Inc (FORM.O; US$64.52; 1; 08 Jan 26; 16:00)
GUC (3443.TW; NT$2365.0; 1H; 09 Jan 26; 13:30)
Marvell Technology Inc (MRVL.O; US$83.45; 1; 08 Jan 26; 16:00)
Mediatek (2454.TW; NT$1420.0; 1; 09 Jan 26; 13:30)
Meta Platforms Inc (META.O; US$646.06; 1; 08 Jan 26; 16:00)
Microsoft Corp. (MSFT.O; US$478.11; 1; 08 Jan 26; 16:00)
NVIDIA Corp (NVDA.O; US$185.04; 1; 08 Jan 26; 16:00)
Powertech Technology (6239.TW; NT$200.0; 1; 09 Jan 26; 13:30)
Samsung Electronics (005930.KS; W139000.0; 1; 09 Jan 26; 15:45)
SK Hynix (000660.KS; W744000.0; 1; 09 Jan 26; 15:45)
SoftBank Corp. (9434.T; ¥214.5; 1; 09 Jan 26; 15:30)
SoftBank Group (9984.T; ¥4263.0; 1H; 09 Jan 26; 15:30)
TE Connectivity Ltd. (TEL.N; US$228.03; 1; 08 Jan 26; 16:00)
Teradyne Inc (TER.O; US$216.31; 1; 08 Jan 26; 16:00)
Tokyo Electron (8035.T; ¥37910.0; 1; 09 Jan 26; 15:30)
TSMC (2330.TW; NT$1680.0; 1; 09 Jan 26; 13:30)

6223.TWO: Fiscal year end 31-Dec — **Price: NT$2,230.00; TP: NT$2,800.00; Market Cap: NT$211,696m; Recomm: Buy/High Risk**

Profit & Loss (NT$m)	2023	2024	2025E	2026E	2027E
Sales revenue	8,147	10,172	13,287	19,347	28,910
Cost of sales	-4,250	-4,611	-5,820	-7,943	-11,311
Gross profit	3,897	5,561	7,467	11,404	17,599
Gross Margin (%)	47.8	54.7	56.2	58.9	60.9
EBITDA (Adj)	**2,008**	**3,039**	**4,532**	**7,641**	**12,442**
EBITDA Margin (Adj) (%)	24.6	29.9	34.1	39.5	43.0
Depreciation	-462	-474	-683	-1,169	-1,692
Amortisation	-75	-83	0	0	0
EBIT (Adj)	**1,471**	**2,483**	**3,849**	**6,471**	**10,749**
EBIT Margin (Adj) (%)	18.1	24.4	29.0	33.4	37.2
Net interest	4	9	-4	-4	-4
Associates	-4	-1	-1	-28	-28
Non-Op/Except/Other Adj	111	304	-61	216	216
Pre-tax profit	**1,582**	**2,795**	**3,783**	**6,655**	**10,933**
Tax	-264	-490	-644	-1,129	-1,856
Extraord./Min.Int./Pref.div.	2	1	1	0	0
Reported net profit	**1,321**	**2,306**	**3,140**	**5,526**	**9,077**
Net Margin (%)	16.2	22.7	23.6	28.6	31.4
Core NPAT	1,321	2,306	3,140	5,526	9,077
Per share data	**2023**	**2024**	**2025E**	**2026E**	**2027E**
Reported EPS ($)	13.91	24.44	32.13	56.74	93.20
Core EPS ($)	13.91	24.44	32.13	56.74	93.20
DPS ($)	7.00	7.50	15.88	21.63	38.06
CFPS ($)	11.01	22.23	48.26	58.51	98.32
FCFPS ($)	7.05	9.20	11.11	19.36	57.22
BVPS ($)	80.81	98.72	124.41	182.62	278.24
Wtd avg ord shares (m)	94.2	94.2	94.3	94.3	94.3
Wtd avg diluted shares (m)	94.9	94.3	97.7	97.4	97.4
Growth rates	**2023**	**2024**	**2025E**	**2026E**	**2027E**
Sales revenue (%)	9.5	24.9	30.6	45.6	49.4
EBIT (Adj) (%)	18.4	68.7	55.0	68.1	66.1
Core NPAT (%)	8.8	74.6	36.2	76.0	64.3
Core EPS (%)	8.4	75.7	31.5	76.6	64.3
Balance Sheet (NT$m)	**2023**	**2024**	**2025E**	**2026E**	**2027E**
Cash & cash equiv.	2,579	3,695	7,843	10,986	17,768
Accounts receivables	1,338	2,050	2,031	3,427	4,944
Inventory	2,752	3,477	4,142	6,358	8,423
Net fixed & other tangibles	4,966	6,319	7,509	10,152	12,463
Goodwill & intangibles	296	318	302	302	302
Financial & other assets	508	618	833	1,151	1,496
Total assets	**12,440**	**16,479**	**22,660**	**32,375**	**45,395**
Accounts payable	564	766	926	1,433	1,906
Short-term debt	170	858	1,106	1,106	1,106
Long-term debt	1,511	1,305	2,930	4,220	5,461
Provisions & other liab	2,575	4,243	5,886	8,279	10,509
Total liabilities	**4,819**	**7,172**	**10,849**	**15,038**	**18,982**
Shareholders' equity	7,614	9,303	11,810	17,337	26,413
Minority interests	6	4	0	0	0
Total equity	**7,620**	**9,307**	**11,810**	**17,337**	**26,413**
Net debt (Adj)	**-898**	**-1,532**	**-3,806**	**-5,660**	**-11,200**
Net debt to equity (Adj) (%)	-11.8	-16.5	-32.2	-32.6	-42.4

Valuation ratios	2023	2024	2025E	2026E	2027E
PE (x)	na	91.2	69.4	39.3	23.9
PB (x)	27.6	22.6	17.9	12.2	8.0
EV/EBITDA (x)	na	69.2	46.0	27.0	16.3
FCF yield (%)	0.3	0.4	0.5	0.9	2.6
Dividend yield (%)	0.3	0.3	0.7	1.0	1.7
Payout ratio (%)	50	31	49	38	41
ROE (%)	18.2	27.3	29.7	37.9	41.5
Cashflow (NT$m)	**2023**	**2024**	**2025E**	**2026E**	**2027E**
EBITDA	2,008	3,039	4,532	7,641	12,442
Working capital	-814	-767	893	-997	-1,194
Other	-148	-175	-708	-945	-1,673
Operating cashflow	**1,046**	**2,097**	**4,717**	**5,698**	**9,575**
Capex	-377	-1,229	-3,631	-3,813	-4,003
Net acq/disposals	-1,066	-288	1,547	0	0
Other	174	174	0	0	0
Investing cashflow	**-1,269**	**-1,343**	**-2,084**	**-3,813**	**-4,003**
Dividends paid	-660	-707	-1,508	-2,053	-3,614
Financing cashflow	**434**	**357**	**1,387**	**1,289**	**1,242**
Net change in cash	**202**	**1,125**	**4,020**	**3,175**	**6,814**
Free cashflow to s/holders	**669**	**868**	**1,086**	**1,885**	**5,572**

For definitions of the items in this table, please click here.

Adding Upside 30-Day Catalyst Watch on ASE Technology Holding (3711.TW)

Direction:	**Upside**
Duration:	Within 30 Days
Catalyst:	Earnings

ASEH will host its earning call in late Jan, and we expect the company to provide a positive growth outlook driven by its strong development in leading edge advanced packaging business with support from its strong capex planning. With improving mix in more advanced packaging sales and more outsourcing opportunity from TSMC's oS process and wafer sorting/probing testing service, we foresee a solid margin expansion for ASEH in the coming years.

Adding Upside 90-Day Short-Term View on King Yuan Electronics Co (2449.TW)

Direction:	**Upside**
Duration:	Within 90 Days
Category:	Thematic driven

We expect strong earnings growth for KYEC in the near-to-medium term supported by robust Nvidia's GPU and AI ASIC shipments and longer testing time for AI chips when migrating to more advanced node with chiplet design and bigger die size. We are also seeing new opportunity from TSMC's outsourcing CP business to provide upside to its growth momentum.

Adding Upside 90-Day Short-Term View on MPI (6223.TWO)

Direction:	**Upside**
Duration:	Within 90 Days
Category:	Thematic driven

We see an accelerating earning growth outlook for MPI as we view it as a key beneficiary of the increasing demand and complexity for probe cards with AI chips migrating to more advanced node. With strong demand for AI chips, especially for ASIC, and improving sales mix on strong MEMS expansion, we are positive over MPI growth outlook.

Bull/Bear: ASE Technology Holding (3711.TW)

NT$350.00	NT$340.00	NT$250.00
▲29% Upside	▲25% Upside	▼8.1% Downside



Spread 37pp
Current Price and expected returns (upside/downside) as of 09 Jan 2026

BULL Assumptions

- Stonger-than-expected margin expansion
- Higher-than-expected utilization rate
- Bull case TP to be based on our DCF valuation on the assumption of a terminal sales growth of 6%

BASE Assumptions

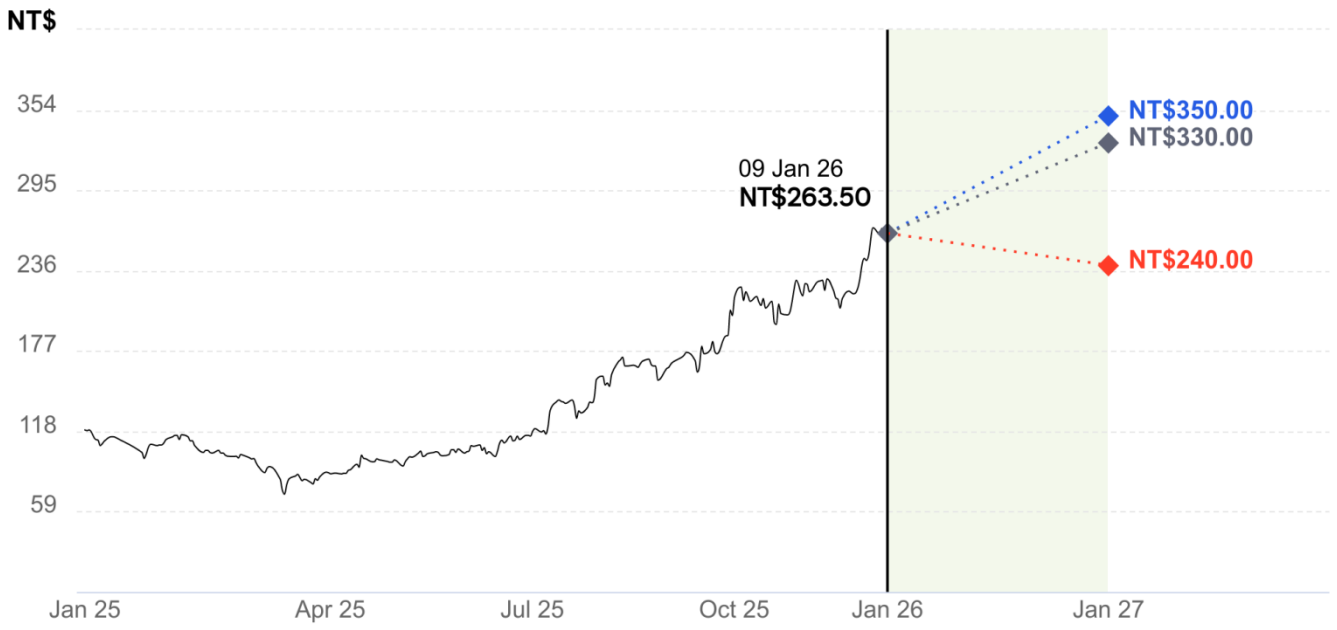
- 5% long-term revenue growth
- Long-term operating margin maintained at >12%

BEAR Assumptions

- Muted revenue growth with margin contraction
- Lower-than-expected utilization rate
- Bear case TP to be based on our DCF valuation on the assumption of a terminal sales growth of 4%

Bull/Bear: King Yuan Electronics Co (2449.TW)

NT$ 350.00 ▲33% Upside | NT$ 330.00 ▲25% Upside | NT$ 240.00 ▼8.9% Downside



Spread 42pp
Current Price and expected returns (upside/downside) as of 09 Jan 2026

BULL Assumptions

- Stronger than expected demand outlook from global consumer electronic products
- Better than expected demand from automotive and base station sector
- Bull case TP to be based on our DCF valuation on the assumption of a terminal sales growth of 18%

BASE Assumptions

- Smooth products transition schedule for AI GPU and ASIC
- Ongoing GM expansion from 2023's 34% to >38% in 2026-2027E

BEAR Assumptions

- Weaker than expected end-demand for global smartphone/consumer electronic products
- Pricing pressure from increasing competition
- Bear case TP to be based on our DCF valuation on the assumption of a terminal sales growth of 10%

Bull/Bear: MPI (6223.TWO)

NT$3,000.00	NT$2,800.00	NT$1,800.00
▲35% Upside	▲26% Upside	▼19% Downside



Spread 54pp
Current Price and expected returns (upside/downside) as of 09 Jan 2026

BULL Assumptions

- Stronger than expected demand from AI customers
- New project wins from AI customers
- Smooth development in CPO business

BASE Assumptions

- Sales growth of >40% in 2026/27
- GM >55% in 2026/27

BEAR Assumptions

- Slowdown in AI customers demand
- Intensifying competition from peers
- Slower development in CPO business

ASE Technology Holding

Company description

Advanced Semiconductor Engineering (ASE), incorporated in 1984 and listed at the TWSE in 1989, is one of the world's leading companies in the semiconductor packaging and testing sector. In June 2016, ASE entered into a Joint Share Exchange Agreement with SPIL under which ASE Industrial was eventually to be formed as a holding company with 100% equity interests in both ASE and SPIL. ASE Industrial was listed on Taiwan's main board on April 30, 2018, the same day on which ASE and SPIL were delisted.

Investment strategy

We have a Buy rating on ASE Holding. The combined ASE-SPIL entity is the highest-quality OSAT worldwide, in our view, with its market share leadership, superior operations, economies of scale, and customer/product diversification. Conditions imposed by the Chinese government on the ASE-SPIL merger, which required them to operate independently, were lifted in 2020. Consequently, we believe ASE Holding will benefit from further revenue and operating synergies as well as the trend for advanced packaging.

Valuation

Our target price of NT$340 is derived using a DCF methodology. Using Bloomberg data, we apply a risk-free rate of 2.5%, a risk premium of 6%, and a beta of 1.34x for a 10.5% cost of equity. With a 20% corporate tax and a 3.0% interest rate on its debt, our WACC for ASE Holding is 8.5%. We assume terminal sales growth of 5%. We model its adjusted EBIT margin to gradually improve from 7.3% in 2024 to 12.5% in 2035E. At our target price, the shares would trade at a 2026/27E P/B of 5x/4x and a 2026/27E P/E of 22x/16x which is inline with its global peers.

Risks

Key downside risks that could prevent ASE shares from reaching our target price include: 1) poor efficiency and less synergy created from merger with SPIL; 2) failure to gain market share in advanced packaging; 3) industry oversupply due to aggressive capacity expansion; 4) severe pricing erosion due to competition; and 5) a longer-than-expected semiconductor inventory correction.

King Yuan Electronics Co

Company description

Founded in 1987, King Yuan Electronics Corp. (KYEC) mainly provides testing services for the back-end process of semiconductor production globally. With more than 30 years of industry experience, KYEC has built up firm relationships with several leading global IC design/IDM customers. Its headquarters and production facilities are both located in Taiwan, with sales offices in North America, Japan, and Singapore.

Investment strategy

We rate KYEC as Buy. As a key testing service provider for AI GPU and ASIC products, KYEC is well positioned to benefit from the significant AI growth opportunity in the years to come. Currently, KYEC is the major final testing service provider for its major customer's AI GPU, and we expect KYEC to continue to secure its dominant share in its customer's upcoming AI GPU product lines due to its specialty in burn-in testing, smooth product delivery capability, and its strong business partnership with its customer. We are also positive over the growth outlook of its smartphone business thanks to the integration of AI functionality, leading to a better replacement cycle. We believe KYEC's major customer in smartphone will benefit from an improved product mix, which will result in longer testing times for the flagship SoC.

Valuation

Our target price for KYEC of NT$330 is derived using a DCF methodology. Using Bloomberg data, we apply a risk-free rate of 3%, a risk premium of 6% and a beta of 1.20x for a 9.7% cost of equity. With 20% corporate tax and a 3.0% interest rate on its debt, our WACC for KYEC is 9.2%. We assume terminal sales growth of 15%. We model its adjusted EBIT margin to gradually improve from 23% in 2024 to 30% in 2035E. At our target price, the shares would trade at a 2026/27E P/B of 7x/5x and a 2026/27E P/E of 34x/22x which is inline with its global peers.

Risks

Key downside risks that could prevent KYEC shares from reaching our target price include: 1) weaker-than-expected end-demand for global smartphone/consumer electronic products; 2) slower ramp for AI-related products; 3) slower-than-expected demand recovery in the automotive and base station sector; and 4) pricing pressure on increasing competition.

MPI

Company description

Founded in 1995 in Hsinchu, Taiwan, MPI Corporation is aiming to build precision probing system for Taiwan semiconductor testing market. In its early years, the company focused primarily on engineering probers for laboratory and wafer-level characterization. By early 2000s, MPI had leveraged its precision machinal base to move up the value chain into vertical probe cards, targeting the testing of DRAM and logic devices. MPI also established its in-house PCB processing and substrate assembly lines to ensure quality control and shorten turnaround time. Over time, MPI has become a key local partner for leading OSATs, supporting vertical probe cards used for volume production in memory and SoC testing. With development in MEMS probe-card fabrication for sub-50um pitches, MPI has developed proprietary process for micro-spring and thin-film formation which has transformed MPI from a precision-mechanical manufacturer into a micro-electromechanical device company- directly competing with global leaders like FormFactor and Technophobe in the most technology-intensive segment of the testing interface market.

Investment strategy

We have a Buy/High Risk rating on MPI as we view it as a key beneficiary of the increasing demand and complexity for probe cards with AI chips migrating to

more advanced node with chiplet design and bigger die size. We have seen the company transitioning from a cyclical probe card supplier to a structural beneficiary of AI-driven test complexity. With the promising growth from AI chips, we expect MPI to deliver sustainable earnings growth and improving sales mix, supported by its rising competitive moats.

Valuation

Our target price for MPI is set at NT$2,800 based on our target PE multiple of 37x to our 2026-2027 EPS average. We believe our PER, at the high-end of its 3-year forward PER range, is justified given MPI's earnings power remains structurally higher than that in the previous cycles. We expect MPI to see an accelerating earnings growth ahead supported by its sustainable sales growth and improving mix. At our target price, the shares would trade at a 2026/27E P/B of 15x/10x

Risks

Our quant risk rating system rates the MPI stock as High Risk for its share-price volatility. Key downside risks that could prevent MPI shares from reaching our target price include 1) Slowdown in AI ASIC demand; 2) Slower than expected adoption of MEMS probe cards; 3) intensifying competition from global and regional peers; 4) Slow development in CPO equipment business.

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Appendix A-1

ANALYST CERTIFICATION

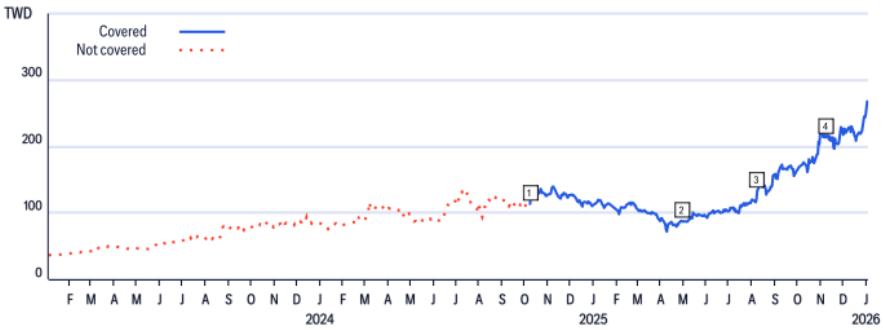
The research analysts primarily responsible for the preparation and content of this research report are either (i) designated by "AC" in the author block or (ii) listed in bold alongside content which is attributable to that analyst. If multiple AC analysts are designated in the author block, each analyst is certifying with respect to the entire research report other than (a) content attributable to another AC certifying analyst listed in bold alongside the content and (b) views expressed solely with respect to a specific issuer which are attributable to another AC certifying analyst identified in the price charts or rating history tables for that issuer shown below. Each of these analysts certify, with respect to the sections of the report for which they are responsible: (1) that the views expressed therein accurately reflect their personal views about each issuer and security referenced and were prepared in an independent manner, including with respect to Citigroup Global Markets Inc. and its affiliates; and (2) no part of the research analyst's compensation was, is, or will be, directly or indirectly, related to the specific recommendations or views expressed by that research analyst in this report.

IMPORTANT DISCLOSURES

King Yuan Electronics Co (2449.TW)

Ratings and Target Price History
Fundamental Research

Analyst: Laura (Chia Yi) Chen



	Date	Rating	Target Price	Closing Price
1	08-Oct-24 05:00:00	*1	*140.00	113.50
2	01-May-25 14:24:22	1	*110.00	86.80
3	08-Aug-25 12:54:06	1	*164.00	133.50
4	07-Nov-25 11:10:57	1	*271.00	213.50

*Indicates Change

Rating/target price changes above reflect Eastern Time

ASE Technology Holding (3711.TW)

Ratings and Target Price History
Fundamental Research

Analyst: Laura (Chia Yi) Chen



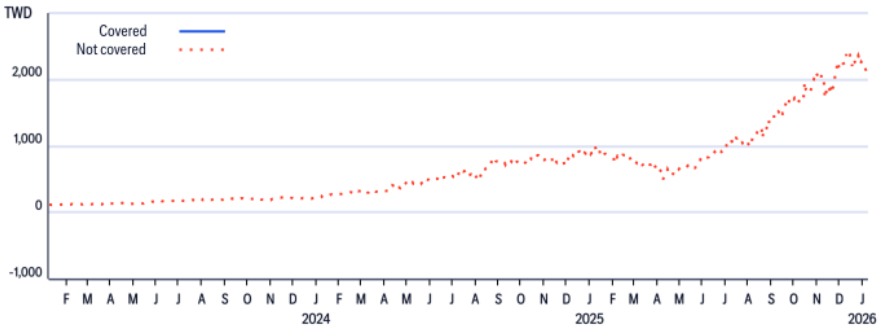
	Date	Rating	Target Price	Closing Price
1	09-Feb-23 12:56:07	1	*115.00	106.00
2	27-Apr-23 10:33:31	1	*108.00	101.00
3	05-Jul-23 07:06:55	1	*123.00	111.50
4	20-Oct-23 13:15:26	1	*135.00	118.50
5	25-Jan-24 18:23:32	1	*154.00	137.00
6	25-Apr-24 11:44:24	1	*166.00	145.00
7	26-Jul-24 06:04:37	1	*183.00	155.50
8	01-Jan-25 09:57:18	1	*192.00	162.00
9	30-Apr-25 11:07:48	1	*162.00	135.50
10	31-Jul-25 10:02:40	1	*186.00	152.50
11	30-Oct-25 10:53:07	1	*252.00	225.00

*Indicates Change

Rating/target price changes above reflect Eastern Time

MPI (6223.TWO)

Ratings and Target Price History
Fundamental Research



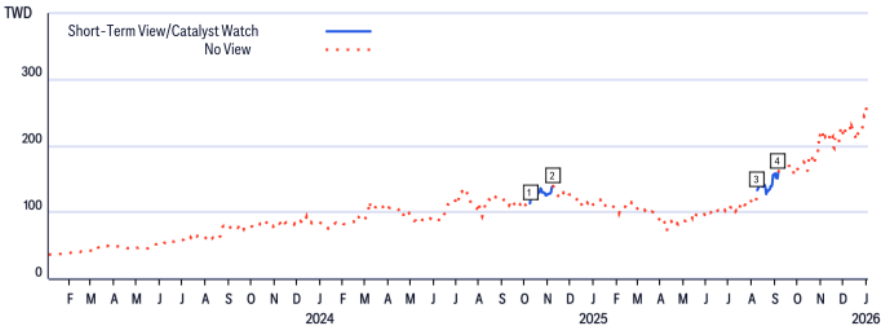
*Indicates Change

Rating/target price changes above reflect Eastern Time

King Yuan Electronics Co (2449.TW)

Short-Term View/Catalyst Watch Research

Analyst: Laura (Chia Yi) Chen



	Date	Action	Expected Direction	Duration	Closing Price
1	08-Oct-24 01:00:00	Add CW	Upside	30 Days	113.50
2	07-Nov-24 19:58:33	Remove CW	Upside	30 Days	139.00

	Date	Action	Expected Direction	Duration	Closing Price
3	08-Aug-25 08:54:06	Add STV	Upside	30 Days	133.50
4	07-Sep-25 21:32:02	Remove STV	Upside	30 Days	160.00

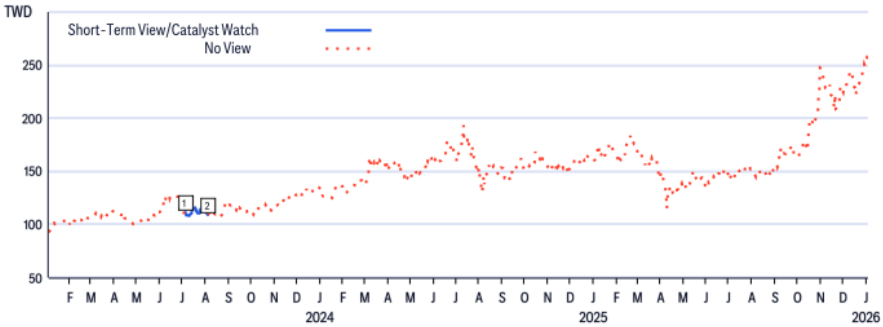
CW - Catalyst Watch , STV - Short-Term View

Rating/target price changes above reflect Eastern Time

ASE Technology Holding (3711.TW)

Short-Term View/Catalyst Watch Research

Analyst: Laura (Chia Yi) Chen



	Date	Action	Expected Direction	Duration	Closing Price
1	05-Jul-23 03:06:55	Add CW	Downside	30 Days	111.50

	Date	Action	Expected Direction	Duration	Closing Price
2	04-Aug-23 11:33:55	Remove CW	Downside	30 Days	109.00

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	12 Month Rating			Catalyst Watch		
Data current as of 01 Jan 2026	**Buy**	**Hold**	**Sell**	**Buy**	**Hold**	**Sell**
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