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TSMC (2330.TW)

Competitive Landscape Holding Steady

CITI'S TAKE

We note that there is rising concern on long term competition for TSMC as its customers are considering other alternatives in foundry and advanced packaging. While Intel's EMIB-T presents an alternative packaging strategy, the technology is dependent on the readiness of the ABF substrate ecosystem, a critical factor for next-generation AI scaling. TSMC's predictable yields, cycle times, and cost control at high volumes provide a significant advantage, giving it an edge over competitors. In this note, we provide more detailed comparison from advanced node and design rule differences between EMIB-T and CoWoS.

TSMC's Advanced Node and Packaging Strategy — During TSMC's latest technology symposium, TSMC elaborated on its N2 platform, including N2P and N2X, and the AI-focused A16 node with Super Power Rail, underscoring a shift towards system-level scaling over pure transistor shrink. Separately, advanced packaging, through CoWoS, SolC, and SoW, is central to AI compute scaling, with expanded roadmaps enabling larger, more integrated AI systems. The chip reticle cycle is moving from current 5.5-reticle CoWoS toward 9.5-reticle and eventually beyond 14-reticle package integration by 2028–2029. We estimate CoWoS capacity could continue growing at nearly 85% YoY and 60% YoY into 2026/2027 on continued strong hyperscaler AI demand, and SolC will see substantial increase in 2027/2028 with CoPoS to follow in 2029/2030. We believe TSMC's comprehensive AI manufacturing ecosystem provides a significant competitive advantage.

Competitive Landscape and Intel's EMIB-T — We see no significant change in TSMC's competitive landscape. Major AI and HPC companies have long-term foundry platform decisions locked in. Intel's EMIB-T packaging ecosystem presents a different approach to heterogeneous integration compared to TSMC's CoWoS-L, with the former having a greater reliance on advanced ABF substrate technology. While we believe AI chipmakers may try to diversify their sources and explore Intel's EMIB-T technology, the compute logic of an AI die may remain identical, and the packaging interface often cannot use the same design.

ABF technology readiness is critical for EMIB-T Adoption — Given EMIB-T's design methodology, the readiness of the ABF substrate ecosystem for ultra-high-density routing, precise bridge embedding, and advanced power delivery is critical for EMIB-T adoption. We believe the capacity and technology readiness will be key checkpoint for EMIB-T penetration in the next 2–3 years.

Earnings Summary

Year to 31 Dec	Net Profit (NT\$M)	Diluted EPS (NT\$)	EPS growth (%)	P/E (x)	P/B (x)	ROE (%)	Yield (%)
2024A	1,173,268	45.24	39.9	49.1	13.4	30.3	0.6
2025A	1,717,883	66.24	46.4	33.5	10.6	35.4	0.8
2026E	2,563,456	98.85	49.2	22.5	7.9	40.4	1.2
2027E	3,410,850	131.52	33.1	16.9	6.0	40.6	2.0
2028E	4,263,281	164.39	25.0	13.5	4.6	38.9	2.5

Source: Powered by dataCentral

Buy

Short-Term View: Upside, expires 26-JUN-26

Price (13 May 26 13:30)	NT\$2,220.00
Target price	NT\$2,875.00
Expected share price return	29.5%
Expected dividend yield	1.2%
Expected total return	30.7%
Market Cap	NT\$57,570,203M US\$1,826,002M

Price Performance

(RIC: 2330.TW, BB: 2330 TT)


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See Appendix A-1 for Analyst Certification, Important Disclosures and Research Analyst Affiliations.

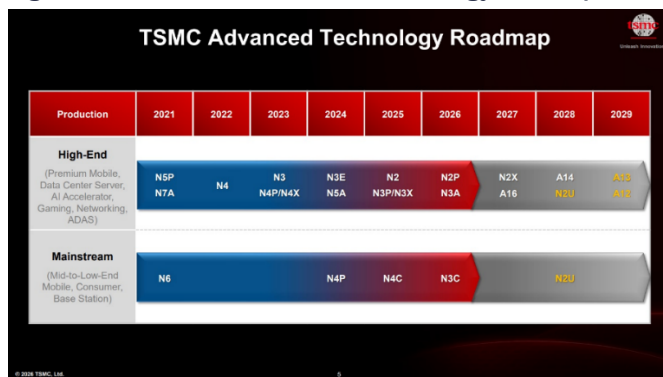
2330.TW: Fiscal year end 31-Dec						Price: NT\$2,220.00; TP: NT\$2,875.00; Market Cap: NT\$57,570,203m; Recomm: Buy					
Profit & Loss (NT\$m)	2024	2025	2026E	2027E	2028E	Valuation ratios	2024	2025	2026E	2027E	2028E
Sales revenue	2,894,308	3,809,054	5,253,452	7,071,349	8,762,189	PE (x)	49.1	33.5	22.5	16.9	13.5
Cost of sales	-1,269,954	-1,527,760	-1,811,170	-2,505,095	-3,075,722	PB (x)	13.4	10.6	7.9	6.0	4.6
Gross profit	1,624,354	2,281,294	3,442,282	4,566,254	5,686,467	EV/EBITDA (x)	28.4	21.3	14.0	10.5	8.3
Gross Margin (%)	56.1	59.9	65.5	64.6	64.9	FCF yield (%)	1.6	2.0	2.3	4.2	5.7
EBITDA (Adj)	1,984,850	2,624,188	3,931,270	5,150,214	6,401,563	Dividend yield (%)	0.6	0.8	1.2	2.0	2.5
EBITDA Margin (Adj) (%)	68.6	68.9	74.8	72.8	73.1	Payout ratio (%)	31	27	28	33	33
Depreciation	-662,797	-688,096	-946,363	-1,203,501	-1,483,358	ROE (%)	30.3	35.4	40.4	40.6	38.9
Amortisation	0	0	0	0	0	Cashflow (NT\$m)	2024	2025	2026E	2027E	2028E
EBIT (Adj)	1,322,053	1,936,092	2,984,907	3,946,713	4,918,205	EBITDA	1,984,850	2,624,188	3,931,270	5,150,214	6,401,563
EBIT Margin (Adj) (%)	45.7	50.8	56.8	55.8	56.1	Working capital	68,257	27,877	-455,087	-30,215	-60,205
Net interest	67,781	86,206	99,885	160,216	215,053	Other	-147,949	-215,723	-421,452	-535,863	-654,923
Associates	828	2,546	2,000	2,000	2,000	Operating cashflow	1,905,157	2,436,342	3,054,732	4,584,136	5,686,435
Non-Op/Except/Other Adj	15,176	16,819	25,166	35,357	43,811	Capex	-956,007	-1,272,411	-1,725,763	-2,150,000	-2,400,000
Pre-tax profit	1,405,839	2,041,663	3,111,959	4,144,285	5,179,068	Net acq/disposals	74,369	122,881	140,206	88,926	-330,102
Tax	-233,407	-326,266	-549,476	-735,652	-918,557	Other	0	0	0	0	0
Extraord./Min.Int./Pref.div.	836	2,486	973	2,217	2,770	Investing cashflow	-881,638	-1,149,530	-1,585,557	-2,061,074	-2,730,102
Reported net profit	1,173,268	1,717,883	2,563,456	3,410,850	4,263,281	Dividends paid	-363,055	-466,779	-716,556	-1,127,769	-1,417,854
Net Margin (%)	40.5	45.1	48.8	48.2	48.7	Financing cashflow	-313,242	-590,737	-668,609	-1,083,140	-1,355,192
Core NPAT	1,173,268	1,717,883	2,563,456	3,410,850	4,263,281	Net change in cash	627,147	615,273	709,637	1,348,993	1,510,211
Per share data	2024	2025	2026E	2027E	2028E	Free cashflow to s/holders	949,151	1,163,931	1,328,969	2,434,136	3,286,435
Reported EPS (\$)	45.24	66.24	98.85	131.52	164.39	Rev breakdown by node	2024	2025	2026E	2027E	2028E
Core EPS (\$)	45.24	66.24	98.85	131.52	164.39	FinSumm - Time Series data item 3	na	na	na	na	na
DPS (\$)	14.00	18.00	27.63	43.49	54.67	2nm (%)	0	0	14	29	na
CFPS (\$)	73.46	93.95	117.79	176.77	219.27	3nm (%)	20	25	29	30	na
FCFPS (\$)	36.60	44.88	51.25	93.86	126.73	5nm (%)	33	37	28	23	na
BVPS (\$)	165.37	208.98	280.20	368.24	477.96	10/7nm (%)	18	15	13	9	na
Wtd avg ord shares (m)	25,934	25,933	25,933	25,933	25,933	16/20nm (%)	8	7	5	3	na
Wtd avg diluted shares (m)	25,934	25,933	25,933	25,933	25,933	21nm to 32nm (%)	8	7	5	3	na
Growth rates	2024	2025	2026E	2027E	2028E	33nm to 45nm (%)	3	2	2	1	na
Sales revenue (%)	33.9	31.6	37.9	34.6	23.9	46nm to 65nm (%)	3	2	2	1	na
EBIT (Adj) (%)	43.5	46.4	54.2	32.2	24.6	66nm to 90nm (%)	1	1	1	0	na
Core NPAT (%)	39.9	46.4	49.2	33.1	25.0	0.10u to 0.13u (%)	1	1	0	0	na
Core EPS (%)	39.9	46.4	49.2	33.1	25.0						
Balance Sheet (NT\$m)	2024	2025	2026E	2027E	2028E	Rev brkdn by geography	2024	2025	2026E	2027E	2028E
Cash & cash equiv.	2,127,627	2,767,856	3,370,288	4,567,293	5,868,991	N. America (%)	70	na	na	na	na
Accounts receivables	272,088	281,791	582,266	691,824	879,972	Asia-Pacific (%)	10	na	na	na	na
Inventory	287,869	288,109	428,376	507,275	643,042	China (%)	11	na	na	na	na
Net fixed & other tangibles	3,235,771	3,691,841	4,524,195	5,618,469	7,157,885	EMEA (%)	3	na	na	na	na
Goodwill & intangibles	0	0	0	0	0	Japan (%)	5	na	na	na	na
Financial & other assets	769,374	903,426	1,126,006	1,261,332	1,490,863						
Total assets	6,692,729	7,933,024	10,031,132	12,646,193	16,040,753						
Accounts payable	74,227	84,330	113,188	137,050	169,985						
Short-term debt	59,858	136,926	182,927	223,123	280,244						
Long-term debt	958,429	896,062	896,062	896,062	896,062						
Provisions & other liab	1,275,849	1,354,911	1,530,287	1,795,993	2,252,299						
Total liabilities	2,368,362	2,472,229	2,722,464	3,052,228	3,598,590						
Shareholders' equity	4,288,545	5,419,596	7,266,496	9,549,576	12,395,003						
Minority interests	35,031	41,199	42,172	44,389	47,159						
Total equity	4,323,576	5,460,795	7,308,668	9,593,965	12,442,162						
Net debt (Adj)	-1,109,340	-1,734,869	-2,291,299	-3,448,108	-4,692,685						
Net debt to equity (Adj) (%)	-25.7	-31.8	-31.4	-35.9	-37.7						

For definitions of the items in this table, please click [here](#).

Leading position in the most advanced node and packaging remains intact

At the latest TSMC Technology Symposium, the company made it amply clear that its future competitiveness is no longer based purely on transistor shrink, but on building a long-duration process ecosystem spanning multiple optimized node variants. The most important message was that N2 is becoming an entire platform family rather than a one-time technology transition. TSMC reiterated that N2 entered risk production trajectory successfully for second-half of 2025, followed by N2P in 2H26 and N2X afterward for higher-performance HPC applications. More importantly, TSMC emphasized A16 as the key AI/HPC-oriented node that introduces its backside power delivery architecture called Super Power Rail (SPR). **TSMC highlighted direct backside contact architecture to reduce IR drop and improve routing efficiency. From an industry perspective, this is strategically critical because AI accelerators are increasingly constrained by power delivery and routing congestion rather than transistor density alone.** TSMC claims A16 can deliver roughly 8–10% performance improvement or 15–20% lower power versus N2P, alongside modest density gains. It is also worth noting that TSMC stated that it does not urgently require High-NA EUV through at least 2029, reflecting confidence in its existing EUV optimization capability and cost structure advantage versus competitors aggressively pursuing High-NA insertion.

Figure 1. TSMC – Advanced node technology roadmap



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Source: Citi Research, TSMC

Figure 2. TSMC – Advanced node performance comparison

N2P PPA (vs. N3E)			
Speed Improvement at Same Power	Power Reduction at Same Speed	Logic Density	Chip Density
~18%	~36%	~1.2X	>= 1.15X

TSMC A16™ PPA*			
Technology	Speed Improvement at Same Vdd	Power Reduction at Same Speed	Chip Density
A16 (Ref: N2P)	8~10%	15~20%	1.07~1.10X

*Datacenter AI products

A14 PPA (vs. N2)			
Speed Improvement at Same Power	Power Reduction at Same Speed	Logic Density	Chip Density
10~15%	25~30%	~1.23X	~1.2X

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Source: Citi Research, TSMC

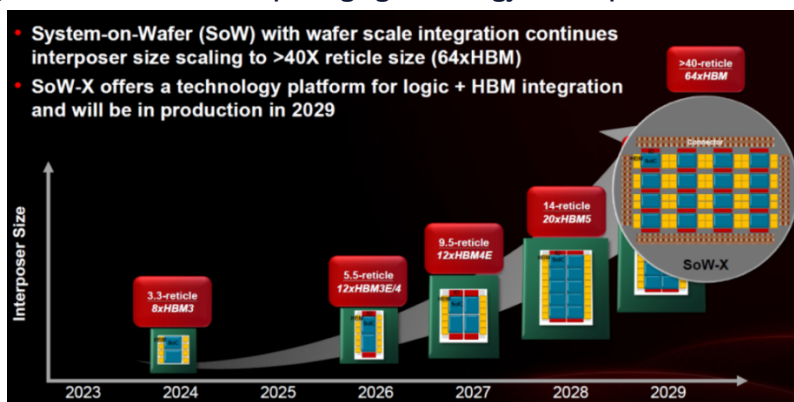
Advanced Packaging has been the Core of AI Scaling Strategy

In the symposium, TSMC also reinforced that advanced packaging is now central to AI compute scaling. It presented an expanded roadmap for CoWoS, SoIC, and System-on-Wafer (SoW) technologies under its 3DFabric strategy with bigger reticle cycle **from current 5.5-reticle CoWoS configurations toward 9.5-reticle and eventually beyond 14-reticle package integration by 2028–2029.** This is extremely significant because it enables far larger AI systems to integrate more compute dies and HBM stacks into single packages. TSMC also highlighted SoW-X, a future wafer-scale integration platform potentially capable of integrating up to 64 HBM stacks and delivering compute capability approaching an entire server rack within a single integrated system. It shows that the industry is now entering

an era where package size, memory integration, optical connectivity, and power delivery architecture determine AI system competitiveness more than transistor shrink alone.

Once again, the important strategic takeaway from the symposium was that **TSMC is shifting the industry narrative away from traditional node naming competition toward full-system scaling capability**. Instead of focusing purely on whether A16 competes with Intel 18A or Samsung SF2, TSMC is emphasizing total AI infrastructure optimization across compute, memory bandwidth, interconnect, optics, packaging, and power efficiency. We estimate CoWoS capacity could continue growing at nearly 85% YoY and 60% YoY into 2026/2027 on continued strong hyperscaler AI demand, and SoIC will see substantial increase in 2027/2028 with CoPoS to follow in 2029/2030.

Figure 3. TSMC – Advanced packaging technology roadmap



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Source: Citi Research, TSMC

It is also worth noting that TSMC's roadmap increasingly separates client/mobile optimization from HPC/AI optimization. Nodes such as A16 and future A12 are clearly positioned for high-power AI systems requiring backside power delivery and extreme routing density, while variants such as A13 appear more cost and area optimized. This indicates that smartphone scaling and AI datacenter scaling are diverging technologically. This is also the key that TSMC's greatest competitive advantage is not transistor leadership alone but its advanced-node ecosystem, advanced packaging infrastructure, and AI supply-chain integration capability. Competitors may narrow transistor gaps, but replicating TSMC's entire AI manufacturing ecosystem will likely be much more difficult over the next few years.

Competitive landscape not changing much

While we see the positives about Intel's (covered by Atif; latest report: [Intel Corp \(INTC.O\) - AI CPU Cycle + Terafab Foundry Opportunity = U/G to Buy](#)) progress in 18A and rising expectation on 14A as Intel has already tied 18A to commercial products including Intel Panther Lake for notebooks and Intel Clearwater Forest for servers, key customers of TSMC such as Apple, NVIDIA and Broadcom, and others may evaluate Intel 18A/14A. This may need to be monitored closely in our view, but evaluation tape-outs are standard industry practice and do not imply big volume mass production. As a result, we don't see competitive landscape changing much for TSMC as of now. In our view, the key debate is no longer just about transistor

performance, but manufacturing stability and economic scalability. **Other than technology leadership, TSMC's advantage has always been on predictable yields, cycle times, defect density control, and acceptable wafer costs at high volume.** Fabless companies require foundries that can perform reliably over years.

More importantly, major AI and HPC companies have already locked in their 2026/2027, or even 2028, platform decisions years ago, particularly around packaging ecosystems, IP portability, software compatibility, and supply-chain predictability. As a result, Intel's initial foundry opportunity is more likely to come from strategic diversification programs, US-government-aligned projects, networking ASICs, or second-source manufacturing strategies rather than displacement of TSMC.

Intel EMIB-T vs TSMC CoWoS-L; Different Philosophy of Advanced Integration

As AI accelerator complexity continues to rise, hyperscalers and leading ASIC vendors are beginning to explore whether the same AI chip architecture could be deployed using either TSMC's CoWoS-L platform or another alternative, such as Intel's EMIB-T packaging ecosystem. The motivation is largely strategic: reducing dependency on a single packaging supply chain, mitigating CoWoS capacity constraints, improving negotiating leverage, and diversifying manufacturing risk.

It is becoming increasingly important that advanced packaging evolves from a backend assembly process into a critical system-level performance differentiator. Also worthy to note AI packaging architecture directly impacts bandwidth density, power efficiency, thermal behavior, scalability, and ultimately total system cost, and Intel EMIB-T and TSMC CoWoS-L basically represent two fundamentally different approaches to heterogeneous integration.

CoWoS-L extends TSMC's CoWoS family by combining local silicon interconnect structures with RDL-based large-area routing, allowing very high bandwidth connectivity across large package footprints. Much of the fine-pitch routing burden is absorbed by silicon interposer-like structures and redistribution layers. This architecture is particularly well suited for large AI accelerators with multiple HBM stacks, where extremely wide memory interfaces and dense chip-to-chip interconnects are required.

By contrast, Intel EMIB-T relies on localized embedded silicon bridges rather than a full-size silicon interposer. The high-density interconnect is concentrated only where necessary, while a much larger portion of package-level routing responsibility is pushed into the ABF substrate itself. This significantly changes the substrate complexity, as the package substrate must now handle more power distribution, signal breakout, high-speed routing, via structures, and embedded trace management.

As a result, EMIB-T generally imposes greater demands on substrate technology, including:

- ultra-fine line/space routing
- advanced laser via structures
- higher layer counts

- tighter warpage control
- lower-loss ABF materials
- and more sophisticated embedded routing architectures

Intel remains heavily dependent on advanced substrate vendors such as Ibiden, Shinko, and Unimicron for its next-generation AI packaging roadmap. And substrate makers' capacity and technology progress will be key checking points whether EMIB-T is ready to pick up in big scale in next one year or two.

Dual Packaging challenge

We see a growing possibility that AI chipmakers may try to diversify their sources and try Intel's EMIB-T technology, and while the compute logic of an AI die may remain identical, **the packaging interface often cannot use the same CoWoS design.**

The first challenge lies in bump architecture and pad layout. A die originally optimized for CoWoS-L may place its HBM PHYs, die-edge interfaces, micro bump arrays, and power pads according to the routing assumptions of TSMC's silicon interconnect architecture. EMIB-T, however, may require different bridge landing zones, alternative bump pitch optimization, and distinct signal escape topologies.

Another key consideration would be power delivery integrity. As AI accelerators move toward multi-kilowatt rack-scale systems, package-level power distribution becomes a limiting factor. CoWoS-L and EMIB-T distribute current differently across the package hierarchy. EMIB-T often places heavier reliance on substrate-side power routing, while CoWoS-L can leverage larger silicon routing regions to assist in power and signal balancing.

In addition, the signal integrity and HBM routing become increasingly difficult at higher bandwidth generations. HBM4 and future memory architecture require massive parallel interfaces operating at extremely high speeds. CoWoS-L's large-area routing capability may offer advantages in scaling memory connectivity, while EMIB-T must carefully optimize bridge placement and substrate escape routing to achieve similar bandwidth efficiency.

Given the different design rules, we expect the ecosystem support across validation and reliability complexity rise dramatically when supporting two packaging ecosystems simultaneously. **And we believe Mediatek's TPU progress at EMIB-T will be an important indicator to watch out.**

ABF Substrate technology readiness is key for EMIB-T take-off

Compared to TSMC's CoWoS approach, Intel's EMIB-T may place even greater importance on substrate engineering because more routing and system integration responsibility shifts from the silicon interposer toward the package substrate itself. The ABF substrate is responsible not only for structural support, but also for ultra-high-density redistribution routing, power delivery integrity, signal integrity management, thermal stability, and integration of embedded bridge structures. It must accommodate extremely fine-line routing, precise bridge embedding, ultra-low-loss high-speed signaling, and increasingly complex power distribution networks supporting AI accelerators consuming well above 1,000W package-level

power. This significantly raises substrate complexity compared with traditional server CPUs.

Suppliers capable of advanced ABF substrate manufacturing, fine-line build-up films, precision drilling, embedded bridge integration, and low-warpage control therefore become strategically important in the EMIB-T supply chain. In practice, this means substrate technology is no longer a secondary consideration; it is becoming one of the primary enablers determining whether next-generation AI racks can scale bandwidth, power, and thermal performance economically. In our view, the ABF substrate ecosystem's readiness for EMIB-T is also an important check point for EMIB-T's penetration in next 2-3 years.

Figure 4. Comparison of Intel's EMIB-T and TSMC's CoWoS/SoIC

Category	Intel EMIB-T	TSMC CoWoS / SoIC
Core Architecture Philosophy	Modular bridge-based architecture using embedded silicon bridges within substrate	Large silicon interposer-centric architecture with highly integrated routing
Main Objective	Reduce cost and improve scalability of very large AI packages while maintaining high bandwidth	Maximize routing density and bandwidth for large AI accelerators
Interconnect Method	Embedded Multi-die Interconnect Bridges integrated into substrate	Full or partial silicon interposer underneath compute and HBM dies
Packaging Scalability	Potentially more flexible chiplet partitioning and modular scaling	Very mature scaling for massive GPU and HBM integration
Dependence on Large Silicon Interposer	Lower	Higher
Reticle Limit Exposure	Potentially reduced through modular bridge design	More exposed as package sizes continue increasing
Manufacturing Complexity	High substrate integration complexity	High interposer manufacturing complexity
Ecosystem Maturity	Earlier stage, still proving scalability and customer adoption	Industry-leading maturity with years of production learning
AI Customer Adoption	Limited but strategically important	Dominant in AI GPU and ASIC ecosystem
Thermal Challenges	Complex due to modular bridge distribution and high package power	Complex due to very large integrated package footprint
Cost Structure Potential	Potentially lower at very large package sizes	Higher silicon interposer cost but highly optimized production flow
Key Competitive Advantage	Advanced modular chiplet flexibility with strong packaging integration	Proven manufacturing scale, reliability, and ecosystem trust
Key Commercial Risk	Ecosystem readiness and production consistency	Capacity constraints and rising manufacturing complexity

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Source: Citi Research

Reiterate Buy with TP NT\$2,875

We remain positive over TSMC's growth outlook as we are looking for a strong +30% sales CAGR in the next three years, supported by secular AI demand growth and its technology leadership in advanced node and packaging. We reiterate Buy and our target price for TSMC is at NT\$2,875 based on 25x the average of our 2026-27E EPS, slightly higher than its 3-year average, which we believe is justified by TSMC's leading and robust AI demand growth outlook. Our target price equates to 2026E/27E P/E of 29x/22x and 2026E/27E P/B of 10x/8x.

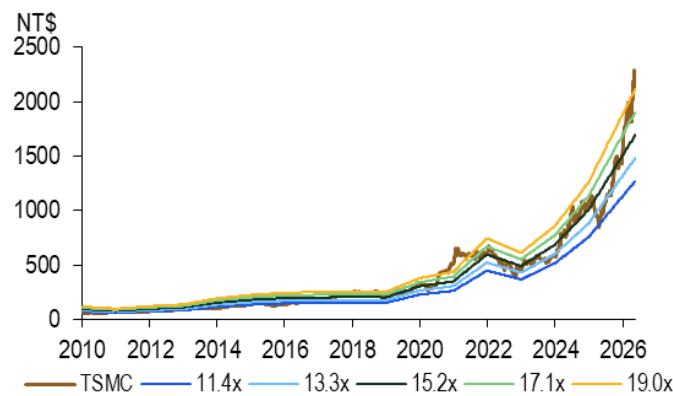
Figure 5. TSMC – Citi Estimates vs Consensus

(NT\$m)	2026E			2027E			2028E		
	Citi	Cons.	Diff.	Citi	Cons.	Diff.	Citi	Cons.	Diff.
Sales	5,253,452	5,191,110	1.2%	7,071,349	6,558,133	7.8%	8,762,189	7,898,797	10.9%
Gross profit	3,442,282	3,406,874	1.0%	4,566,254	4,261,672	7.1%	5,686,467	5,067,631	12.2%
Operating profit	2,984,907	2,972,041	0.4%	3,946,713	3,718,829	6.1%	4,918,205	4,383,234	12.2%
Net income	2,563,456	2,542,290	0.8%	3,410,850	3,177,832	7.3%	4,263,281	3,824,660	11.5%
EPS (NT\$)	98.85	97.97	0.9%	131.52	122.62	7.3%	164.39	146.83	12.0%
Gross margin	65.5%	65.6%	-0.1 ppt	64.6%	65.0%	-0.4 ppt	64.9%	64.2%	+0.7 ppt
Operating margin	56.8%	57.3%	-0.4 ppt	55.8%	56.7%	-0.9 ppt	56.1%	55.5%	+0.6 ppt
Net margin	48.8%	49.0%	-0.2 ppt	48.2%	48.5%	-0.2 ppt	48.7%	48.4%	+0.2 ppt

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Source: Citi Research, Bloomberg

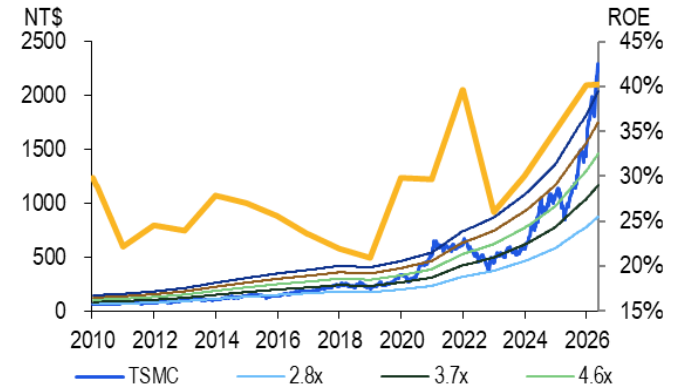
Figure 6. TSMC – Forward P/E band



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Source: Citi Research, company data

Figure 7. TSMC – Forward P/B band & ROE



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Source: Citi Research, company data

Figure 8. TSMC – Forecast Summary

Unit: NT\$bn	2025				2026				2027				2028			
	1Q	2Q	3Q	4Q	1Q	2QE	3QE	4QE	1QE	2QE	3QE	4QE	2025	2026E	2027E	2028E
Revenue	839.3	933.8	989.9	1,046.1	1,134.1	1,239.6	1,361.7	1,518.0	1,681.4	1,768.2	1,818.1	1,803.7	3,809.1	5,253.5	7,071.3	8,762.2
COGS	-345.9	-386.4	-401.4	-394.1	-382.8	-412.0	-476.7	-539.6	-587.5	-623.0	-639.0	-655.6	-1,527.8	-1,811.2	-2,505.1	-3,075.7
Gross Profit	493.4	547.4	588.5	652.0	751.3	827.6	884.9	978.5	1,093.8	1,145.2	1,179.0	1,148.1	2,281.3	3,442.3	4,566.3	5,686.5
Operating Expense	-85.2	-84.5	-87.8	-88.2	-94.0	-111.6	-124.4	-129.0	-139.8	-155.6	-161.8	-162.3	-345.2	-457.4	-619.5	-768.3
SG&A expenses	-28.6	-23.2	-24.0	-23.3	-26.2	-34.7	-36.8	-38.0	-38.9	-49.5	-49.1	-45.1	-99.2	-135.7	-182.6	-226.4
R&D expenses	-56.5	-61.3	-63.7	-64.9	-67.8	-76.9	-87.7	-91.1	-100.9	-106.1	-112.7	-117.2	-246.4	-323.4	-436.9	-541.8
EBIT	407.1	463.4	500.7	564.9	659.0	716.0	760.5	849.4	954.0	989.6	1,017.2	985.8	1,936.1	2,984.9	3,946.7	4,918.2
Net Interest Income	19.8	20.3	21.3	24.8	23.8	22.9	25.3	27.9	34.5	38.5	41.6	45.6	86.2	99.9	160.2	215.1
Net Other Income	4.0	9.4	3.4	2.6	5.1	6.7	7.3	8.1	8.9	9.3	9.6	9.5	19.4	27.2	37.4	45.8
Pre Tax Profit	430.9	493.0	525.4	592.4	687.8	745.7	793.0	885.4	997.5	1,037.5	1,068.4	1,040.9	2,041.7	3,112.0	4,144.3	5,179.1
Tax Expense/(Credit)	70.2	95.5	73.6	86.9	115.0	149.1	134.8	150.5	169.6	207.5	181.6	177.0	-326.3	-549.5	-735.7	-918.6
Net Profit	361.6	398.3	452.3	505.7	572.5	596.9	658.7	735.4	828.4	830.5	887.4	864.5	1,717.9	2,563.5	3,410.8	4,263.3
EPS (NT\$)	13.94	15.36	17.44	19.50	22.08	23.02	25.40	28.36	31.95	32.02	34.22	33.34	66.24	98.85	131.52	164.39
Margins (%)																
Gross Margin	58.8	58.6	59.5	62.3	66.2	66.8	65.0	64.5	65.1	64.8	64.9	63.7	59.9	65.5	64.6	64.9
Operating Margin	48.5	49.6	50.6	54.0	58.1	57.8	55.8	56.0	56.7	56.0	56.0	54.7	50.8	56.8	55.8	56.1
Net Margin	43.1	42.7	45.7	48.3	50.5	48.2	48.4	48.4	49.3	47.0	48.8	47.9	45.1	48.8	48.2	48.7
Sequential Growth (%)																
Revenue	-3	11	6	6	8	9	10	11	11	5	3	-1	32	38	35	24
Gross Profit	-4	11	8	11	15	10	7	11	12	5	3	-3	40	51	33	25
EBIT	-4	14	8	13	17	9	6	12	12	4	3	-3	46	54	32	25
Net Profit	-4	10	14	12	13	4	10	12	13	0	7	-3	46	49	33	25
EPS	-4	10	14	12	13	4	10	12	13	0	7	-3	46	49	33	25

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Source: Citi Research, company data

TSMC

Company description

TSMC is the founder and leader of the dedicated IC foundry segment. The company has built its reputation by offering advanced and "more-than-Moore" wafer production processes and unparalleled manufacturing efficiency. From its inception in 1987, TSMC has consistently offered the foundry segment's leading technologies and TSMC-compatible design services.

Investment strategy

We rate TSMC shares as Buy. We expect TSMC to deliver sales growth of >30% in recent years thanks to strong growth from HPC/AI as well as stable demand growth from smartphone, IoT, and automotive on tech migration and a shortened replacement cycle. CPU outsourcing to TSMC offers further growth upside potential. A rising cash dividend should also support the share price. While TSMC has been increasing capex meaningfully since 2009, its cost structure is maintained through continuous product mix improvements, efficiency enhancements, and cost reductions.

Valuation

Our target price for TSMC shares of NT\$2,875 is based on 25x the average of our 2026-27E EPS, higher than its three-year average forward PER, versus global peers' average of 15-23x. We believe our PER target is justified by TSMC's leading position in advanced process node and robust AI demand growth outlook. Given its continuing leadership in the semiconductor foundry industry, we believe TSMC's stable order visibility and earnings outlook make it less vulnerable than peers to a potential global economic downturn. Our target price equates to 2026E/27E P/E of 29x/22x and 2026E/27E P/B of 10x/8x.

Risks

Key downside risks that could impede the shares from achieving our target price include: 1) weakness in the global semiconductor market; 2) larger-than-expected margin contractions due to depreciation cost hikes and strong NTD; 3) competitors entering the foundry business; 4) longer-than-expected digestion of inventory in the supply chain; and 5) a slowdown in demand either from a global economic downturn or a global trade disruption triggered by tariffs.

Intel Corp

(INTC.O; US\$120.61; 1; 12 May 26; 16:00)

Company description

Intel is a semiconductor company that specializes in microprocessors and is the #1 supplier of microprocessors for desktop PCs, notebook PCs, and

servers with approximately 60% total market share. Intel also has a foundry business. Based in Santa Clara, CA, Intel has roughly 83,200 employees worldwide. Intel derives approximately 90% of its total revenue and 90% of total profits from the PC and Datacenter segments. Intel is a vertically integrated device manufacturer (IDM) with front-end wafer fabrication facilities in Oregon, Arizona, New Mexico, China, Ireland, and Israel and back-end assembly and test operations in Malaysia, China, Costa Rica, and Vietnam.

Investment strategy

We are Buy rated on Intel shares given the AI-driven CPU cycle and we're more positive on Intel foundry given better execution by Intel management.

Valuation

We value INTC based on our SOTP valuation, our price target is \$95. We apply a SOTP valuation framework to each of Intel's reportable segments and to highlight our growth expectations for Intel Foundry.

Risks

PC end-market: Intel derives roughly 90% of sales from the PC and server segments, which are highly dependent on IT spending. Therefore, any major uptick/downtick in IT spending could result in upside/downside to our estimates and cause us to reassess our rating on INTC.

M&A: If Intel engages in a substantial accretive acquisition, it could result in upside to our estimates.

Competition: Intel competes directly with AMD in the microprocessor market. Consequently, any fluctuations in market share between Intel and AMD could result in risk to our estimates.

Customer risk: Intel's largest PC OEM customers collectively represent roughly 45% Intel's revenue. As a result, any major declines in orders from PC OEMs could have a negative effect on our estimates for Intel.

Macroeconomic: Intel's geographic exposure spans multiple geographies including the U.S., Europe, and Asia. As a result, any prolonged macroeconomic downturn/upturn could result in downside/upside to our estimates and rating.

If the impact from the above risks turns out to be greater/less than we anticipate, the shares could fail to achieve or could exceed our target price.

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Appendix A-1

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IMPORTANT DISCLOSURES

Intel Corp (INTC)
Ratings and Target Price History
Fundamental Research

Analyst: Atif Malik



Date	Rating	Target Price	Closing Price
17-Jul-23 07:11:15	2	*\$34.00	34.37
12-Jan-24 06:06:09	2	*47.50	47.12
15-Apr-24 06:04:21	2	*40.00	36.31
26-Apr-24 03:00:00	2	*35.00	31.88

Date	Rating	Target Price	Closing Price
02-Aug-24 08:05:49	2	*25.00	21.48
01-Nov-24 03:17:08	2	*22.00	23.20
21-Jan-25 03:00:00	2	*21.00	21.77
07-Jul-25 03:00:00	2	*24.00	22.00

Date	Rating	Target Price	Closing Price
19-Sep-25 02:10:39	*3	*29.00	29.58
15-Jan-26 07:24:43	*2	*50.00	48.32
23-Jan-26 01:48:19	2	*48.00	45.07
24-Apr-26 06:29:21	*1	*95.00	82.54

*Indicates Change

Rating/target price changes above reflect Eastern Time

TSMC (2330.TW)
Ratings and Target Price History
Fundamental Research

Analyst: Laura (Chia Yi) Chen



Date	Rating	Target Price	Closing Price
28-Jun-23 11:09:56	1	*660.00	574.00
22-Nov-23 00:43:24	1	*720.00	577.00
18-Jan-24 10:40:18	1	*740.00	588.00
09-Apr-24 10:09:45	1	*950.00	819.00
18-Apr-24 09:00:06	1	*1,030.00	804.00
17-Jun-24 04:51:05	1	*1,150.00	921.00
18-Jul-24 08:21:47	1	*1,500.00	1,005.00

Date	Rating	Target Price	Closing Price
17-Oct-24 09:15:17	1	*1,540.00	1,035.00
21-Mar-25 15:53:47	1	*1,400.00	972.00
09-Apr-25 07:55:10	1	*1,050.00	785.00
17-Apr-25 10:33:27	1	*1,100.00	847.00
26-Jun-25 02:57:46	1	*1,280.00	1,075.00
17-Jul-25 09:46:31	1	*1,400.00	1,130.00
25-Sep-25 09:04:47	1	*1,600.00	1,320.00

Date	Rating	Target Price	Closing Price
16-Oct-25 10:32:46	1	*1,800.00	1,485.00
09-Jan-26 04:15:15	1	*2,450.00	1,680.00
15-Jan-26 10:05:29	1	*2,600.00	1,690.00
27-Mar-26 10:38:33	1	*2,800.00	1,820.00
16-Apr-26 08:25:24	1	*2,875.00	2,085.00

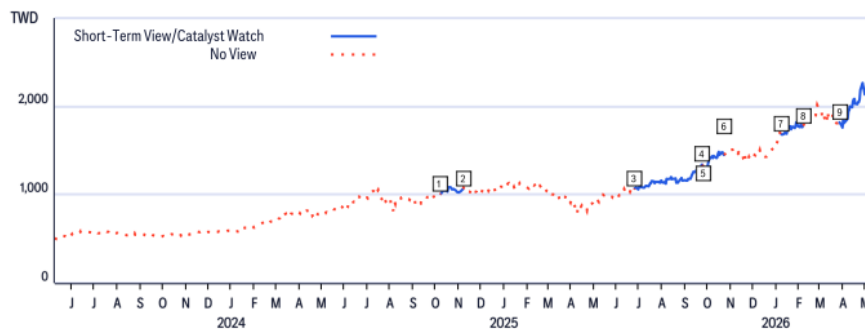
*Indicates Change

Rating/target price changes above reflect Eastern Time

TSMC (2330.TW)

Short-Term View/Catalyst Watch Research

Analyst: Laura (Chia Yi) Chen



	Date	Action	Expected Direction	Duration	Closing Price		Date	Action	Expected Direction	Duration	Closing Price		Date	Action	Expected Direction	Duration	Closing Price
1	08-Oct-24 01:00:00	Add CW	Upside	30 Days	1,010.00	4	24-Sep-25 21:58:41	Remove STV	Upside	90 Days	1,340.00	7	08-Jan-26 23:15:15	Add CW	Upside	30 Days	1,685.00
2	07-Nov-24 19:58:59	Remove CW	Upside	30 Days	1,065.00	5	25-Sep-25 05:04:47	Add CW	Upside	30 Days	1,320.00	8	08-Feb-26 19:44:43	Remove CW	Upside	30 Days	1,780.00
3	25-Jun-25 22:57:46	Add STV	Upside	90 Days	1,070.00	6	24-Oct-25 14:20:26	Remove CW	Upside	30 Days	1,450.00	9	27-Mar-26 06:38:33	Add STV	Upside	90 Days	1,820.00

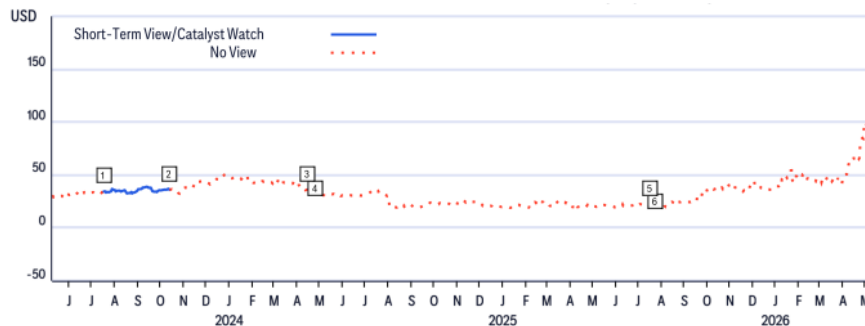
CW - Catalyst Watch, STV - Short-Term View

Rating/target price changes above reflect Eastern Time

Intel Corp (INTC)

Short-Term View/Catalyst Watch Research

Analyst: Atif Malik



	Date	Action	Expected Direction	Duration	Closing Price		Date	Action	Expected Direction	Duration	Closing Price		Date	Action	Expected Direction	Duration	Closing Price
1	17-Jul-23 03:11:15	Add CW	Upside	90 Days	34.37	3	15-Apr-24 02:04:21	Add CW	Upside	30 Days	36.31	5	17-Jul-25 23:00:00	Add STV	Upside	30 Days	22.80
2	15-Oct-23 12:07:05	Remove CW	Upside	90 Days	35.97	4	25-Apr-24 23:00:00	Remove CW	Upside	30 Days	35.11	6	24-Jul-25 23:00:00	Remove STV	Upside	30 Days	22.63

CW - Catalyst Watch, STV - Short-Term View

Rating/target price changes above reflect Eastern Time

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Citigroup Global Markets Taiwan Securities Company Limited Jack Chen; Laura (Chia Yi) Chen; Nicholas Lai

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