WinWay Technology

Your Trusted Partner in Semiconductor Testing

The Evolution of Co-Packaged Optics (CPO) Advanced Testing Methodologies for Silicon Photonics

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Presenter: Collins Sun

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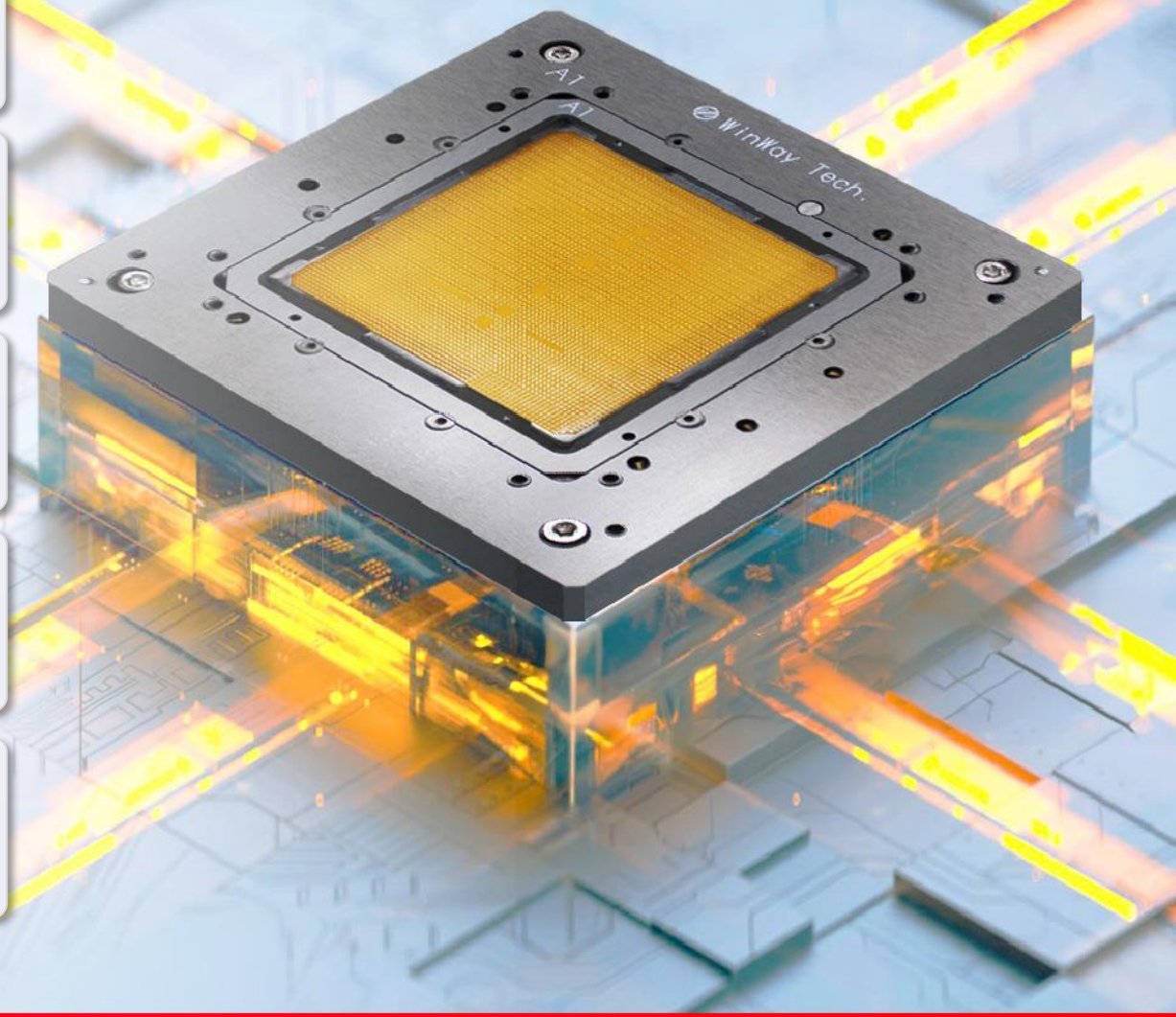
穎崴科技



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CPO and Test Flow

Optical Industry M&A Wave in the AI Era

~$10B+

Nov 2024

Celestial AI acquires Rockley Photonics IP

$20M
SiPho IP consolidation

Dec 2025

Marvell to acquire Celestial AI

$5.5M
Optical scale-up for AI

Feb 2025

Nokia acquires Infinera

$2.3B
Optical networking & DCI

Apr 2026

Credo to acquire DustPhotonics

$1.3B
SiPho PIC vertical integration

May 2025

AMD acquires Enosemi

Undisclosed
SiPho PIC for CPO

Apr 2026

Marvell acquires Polariton Technologies

Undisclosed
Plasmonics + SiPho modulation

Chipmakers & Hyperscalers Back Photonics

~$4.7B+

Oct 2024

Google Ventures et al. → Lightmatter

$400M

CSP → Photonic Computing

Oct 2024

Cisco · NVIDIA → Xscape Photonics

$44M

CSP/Networking + IC → DWDM

Dec 2024

AMD · Intel · NVIDIA → AyarLabs

$155M

IC Design (joint) → Optical I/O

Feb 2026

MediaTek → AyarLabs

$90M

IC Design → Optical I/O

Mar 2026

NVIDIA → Lumentum

$2.0B

IC Design → Laser / SiPho

Mar 2026

NVIDIA → Coherent

$2.0B

IC Design → Laser / Networking

No Single Company Can Solve These Problems

- Thermal Management & Wavelength Stability
- External Laser Source (ELS) Reliability
- **Nano-Scale Optical Alignment**
- **KGD (Known Good Die) Testing Efficiency**
- Modulator Bandwidth & Power Efficiency

System Integration

Thermal Management	⇄ Laser Stability	⇄ Signal Quality
Alignment Precision	⇄ Manufacturing Yield	⇄ Cost Structure
Power Demand	⇄ Architecture Design	⇄ Cooling Limits

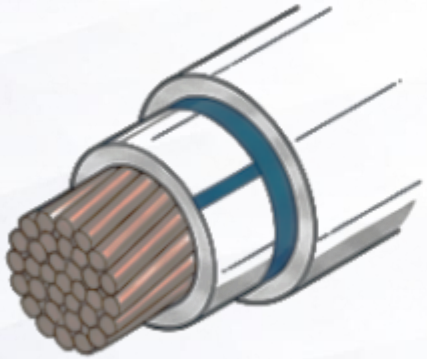
- Kilowatt-Level Power Supply Capacity
- **Signal Integrity (SerDes)**
- Ecosystem Fragmentation & Lack of Standardization
- Field Repair & Diagnostics Capability
- Heterogeneous Integration Manufacturing Variation

The Cost of Distance

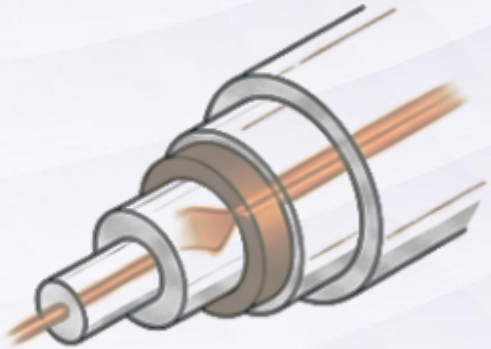
Traditional Pluggable Architecture

102.4T Co-Packaged Optics (CPO)

$$\nabla \cdot \mathbf{E} = \frac{\rho}{\varepsilon_0} \qquad \nabla \cdot \mathbf{B} = 0$$



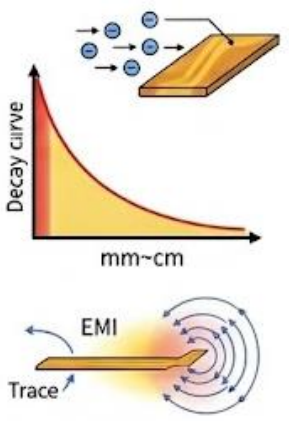
Light and electricity are not competing technologies. They are two manifestations of the exact same physical essence.



$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \qquad \nabla \times \mathbf{B} = \mu_0 \mathbf{J} + \mu_0 \varepsilon_0 \frac{\partial \mathbf{E}}{\partial t}$$

Light and Electricity : Two Quadrants of the Same Electromagnetic Field

Electrical



- Electron
- Conductor with return path
- Copper + Dielectric (Dk/Df)
- Skin effect~1dB/cm@53GHz
- mm~cm (in-package)
- Severe EMI, Coupling

Loss
~1 dB/cm v.s **<0.2 dB/km**

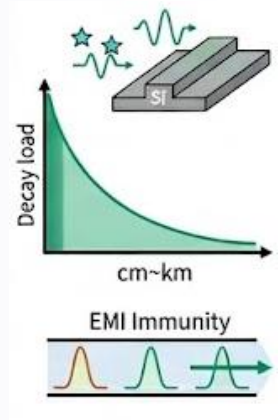
Frequency
DC~100 GHz v.s **~193 THz**

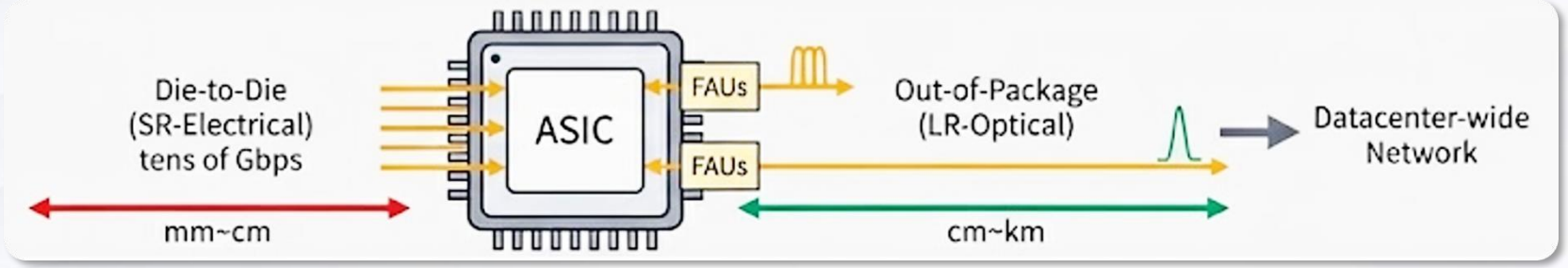
Distance
mm~cm (SR) v.s **cm~km (LR)**

EMI
EMI Sensitive v.s **EMI immune**

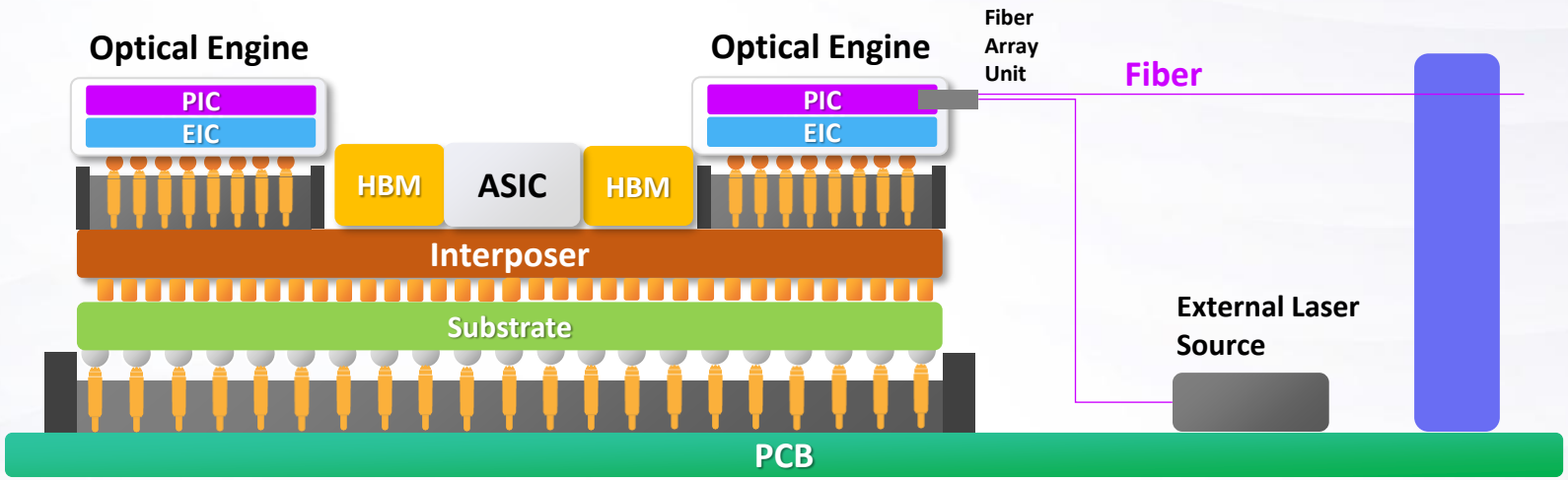
Optical

- Photon
- Internal reflection in wave guide
- Si+SiO2
- Rayleigh scatter <0.2dB/km@1550nm
- cm~km Cross datacenter
- EMI Immune





CPO (Co-Packaged Optics)



Source : AyarLabs

Speed Evolution

From Gbps to Tbps

800G to 1.6T ~ 6.4T

Energy Efficiency Leap

Saving Over 50% Power Consumption

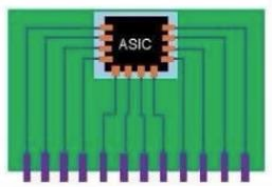
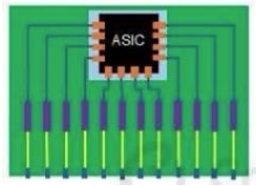
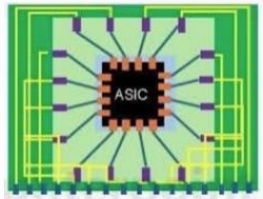
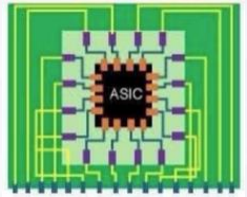
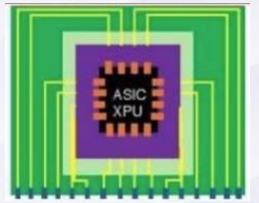
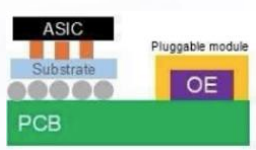
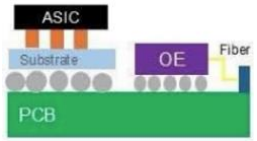
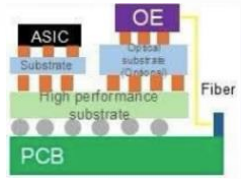
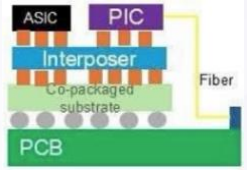
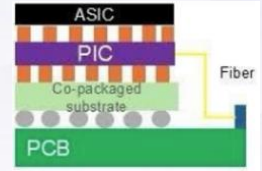
20 pJ/bit to below 5 pJ/bit

Spatial Optimization

Chip-level Packaging Revolution

reducing latency by over 15%

Co-Packaged Optics Trend

	~2016 →	2023 →	2025 →	2027 →	2030~
	Pluggable Optics	**OBO** (On-Board Optics)	**NPO** (Near-Packaged Optics)	**2.5D CPO** (COUPE Switch)	**3D CPO** (COUPE XPU)
					
	100% Cu	*80% Cu + 20% Optics*	*50% Cu + 50% Optics*	*20% Cu + 80% Optics*	*100% Optics*
					
Bandwidth	~800G	<1.6T	<3.2T	<6.4T	12.8T~
Power Use	1x	~0.8x	~0.6x	<0.5x	<0.1x
Latency	1x	<0.75x	<0.5x	<0.1x	<0.05x
Maintenance	●	●	●	●	●

Electrical Circuit | Optical Engine | Optical Circuit | Connector

Source : Counterpoint Research《矽光子與共同封裝光學（CPO）報告》

Silicon Photonics Supply Chain

CSP (End Customer)

NVIDIA, aws, Microsoft, Meta, ByteDance

SOI Wafer (Photonic Wafer)

soitec, Shin-Etsu, SIMGUI, IntelliEPI

Connector

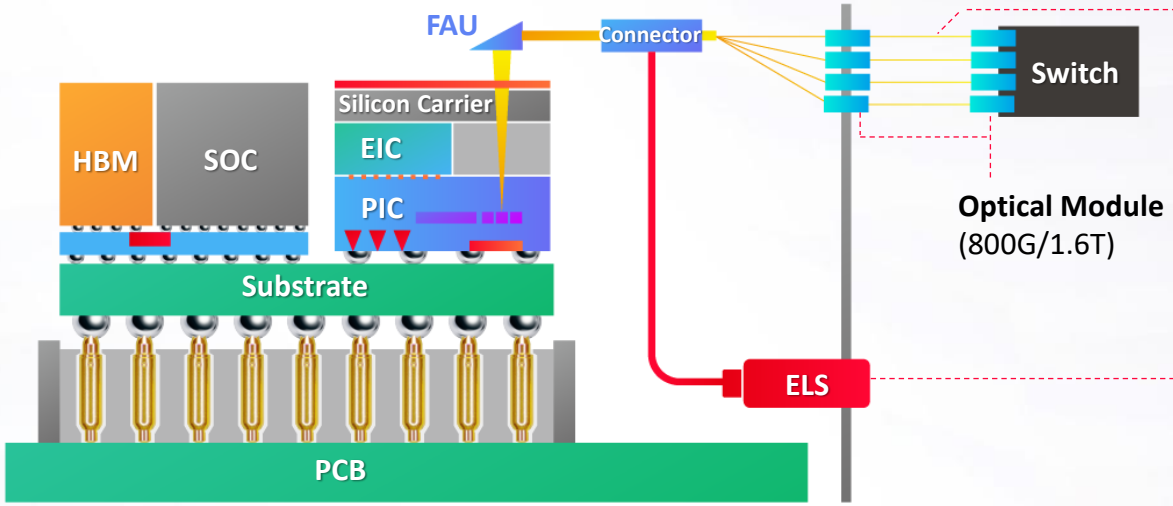
T&S, CONEC, SENKO, Amphenol, LightSense

Testing

WinWay Technology, MPI CORPORATION, HON PREC, Chroma

PIC Design & EDA

IBM, intel, sicoya, MACOM, Juniper, cisco, SiFotonics, POET, Ansys, AyarLabs, FUJITSU, MARVELL, LUMENTUM, Infinera, HUAWEI, RANOVUS, cadence, OpenLight, SKORPIOS, SYNOPSYS



Fiber

CORNING, YOFC, HYBO, SUMITOMO ELECTRIC, FURUKAWA ELECTRIC, 富通集团 FUTONG GROUP, FiberHome, prysmian, Fujikura, ZTT

ELS

FURUKAWA ELECTRIC, BROADCOM, LUMENTUM, COHERENT, SUMITOMO ELECTRIC, TE, O-Net Technologies

Foundry

tsmc, intel, Tower, AOI, silex, GlobalFoundries, SAMSUNG, UMC, ST, Acacia

EIC & DSP Design

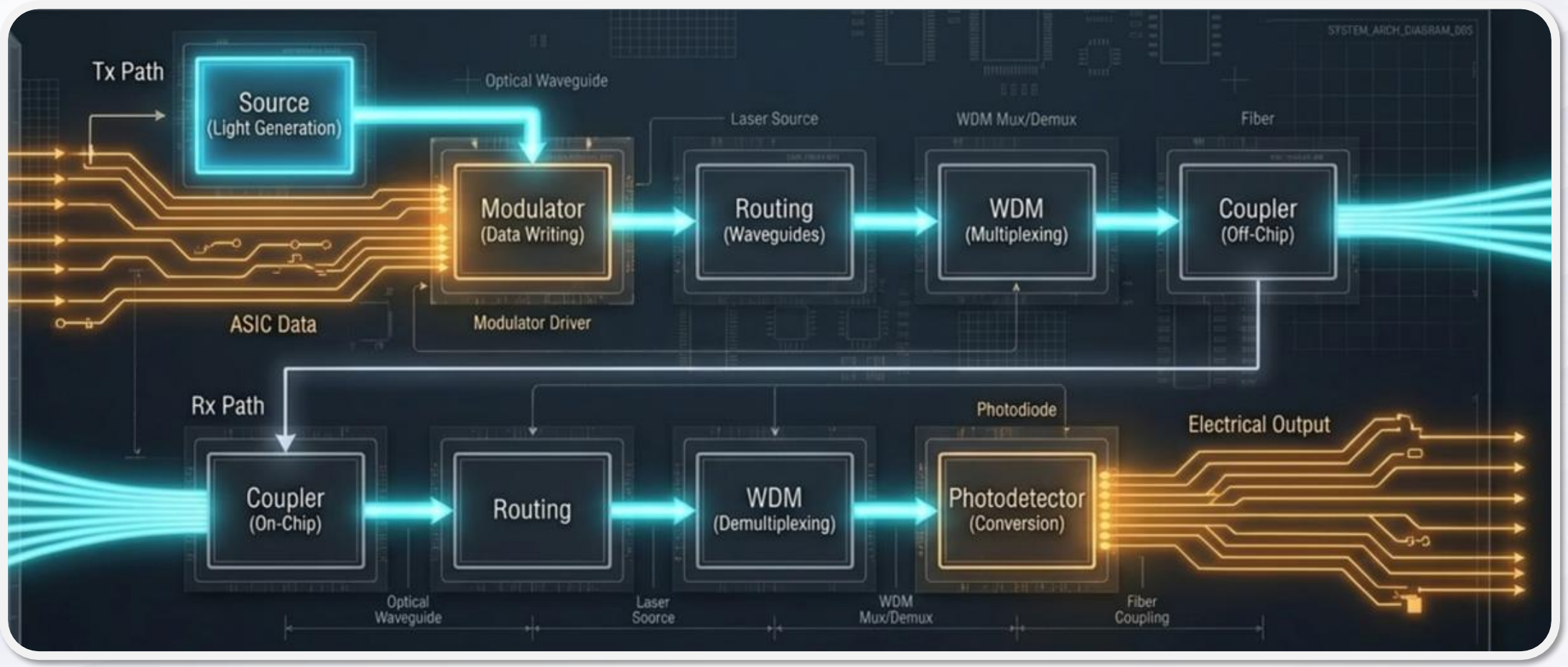
BROADCOM, COHERENT, LUMENTUM, MACOM, ciena, Infinera

Light Source (from EPI wafer)

LandMark, COHERENT, SUMITOMO ELECTRIC, IntelliEPI, IOE, NICHIA

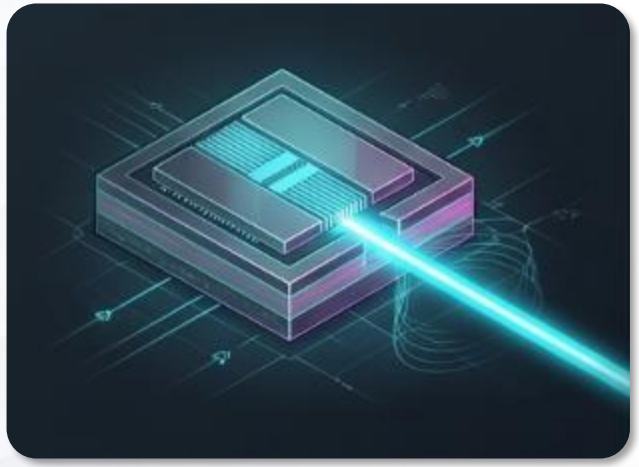
Source : SEMI VISION

The Photonic Integrated Circuit (PIC) Blueprint

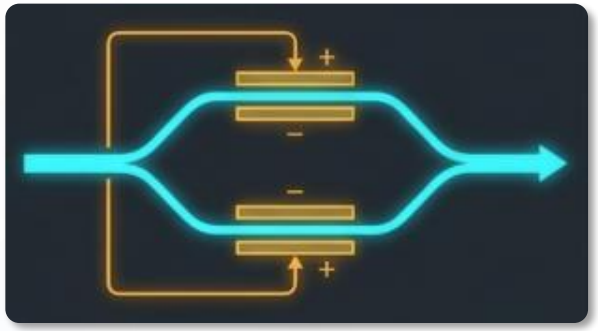
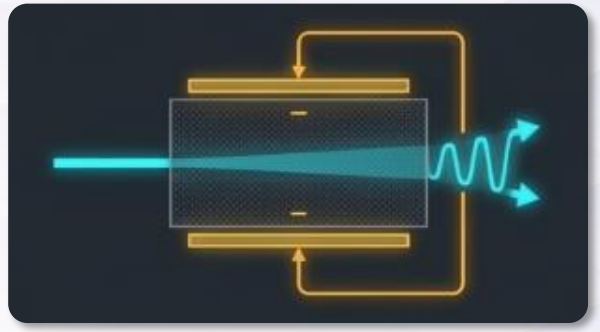


Source : Official Website

Step1 : The Light Source Matrix

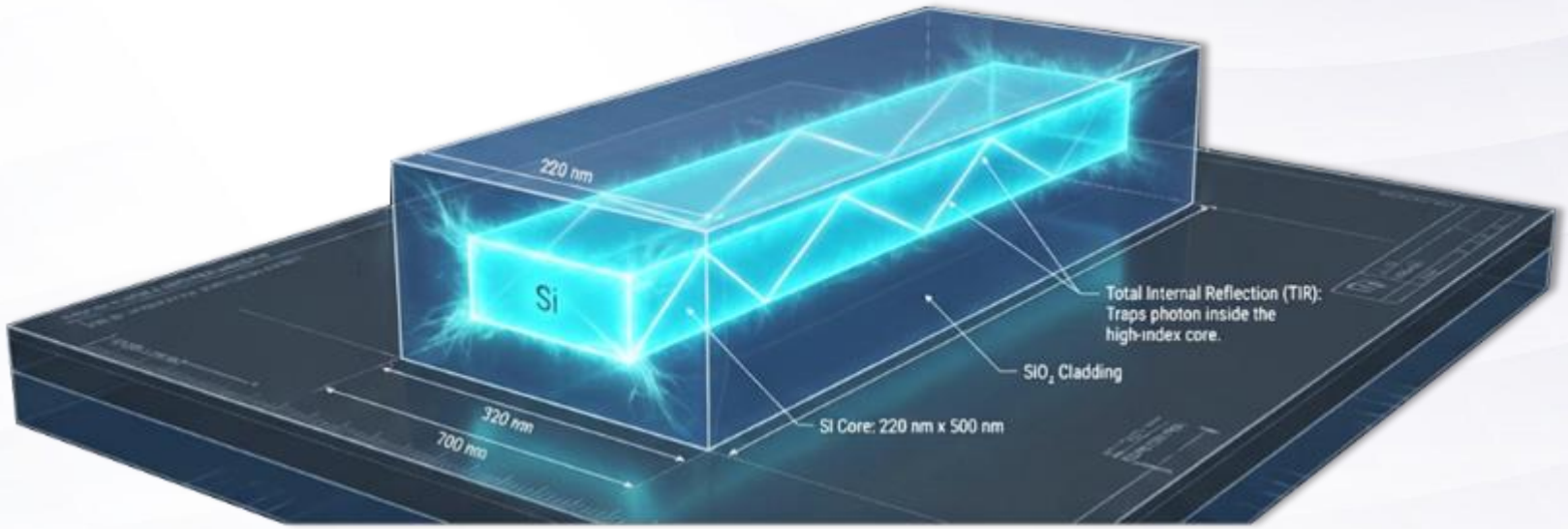
DFB Laser (Distributed Feedback)	VCSEL (Vertical-Cavity Surface-Emitting Laser)	Comb Laser
		
Highly Stable wavelength, narrow linewidth. Ideal for standard 1310nm/1550nm telecom.	Low cost, easy to form arrays. Ideal for short-reach data centers. Limitation : Less suited for long-reach / high-power	Crucial for 102.4T CPO. Generates multiple precise wavelengths from one device, enabling massive WDM density

Step2 : The Modulator Showdown

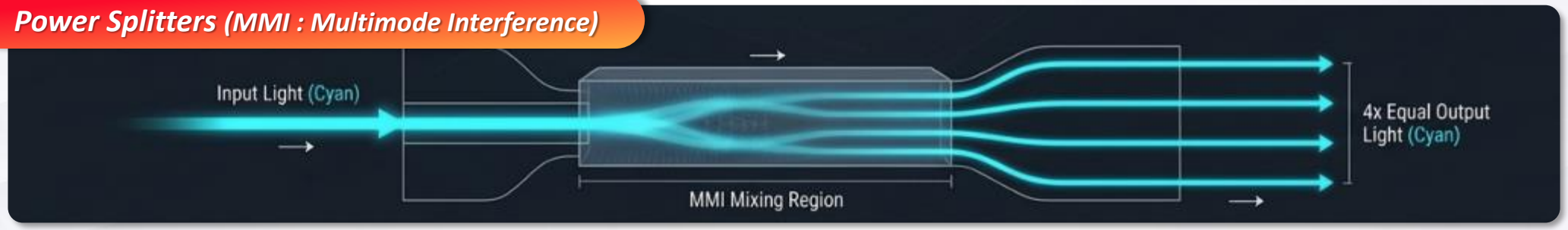
	MZM (Mach-Zehnder)	**MRM** (Micro-Ring)	**EAM** (Electro-Absorption)
			
Footprint	Large (1-3 mm)	Micro (10-20 um)	Small (50-100 um)
Bandwidth	High	Medium	Medium
Thermal Stability	High	Critical(Requires TEC)	Medium
PAM4 Linearity	Excellent	Moderate	Poor
Yield / Maturity	Highest(10+ Yrs)	Medium	Medium
Customer	Broadcom / Intel / Marvell / Lightmatter / Cisco	nVIDIA / AyarLabs	Coherent / Lumentum / Intel

Source : Official Website

Step3 : Routing The Light



Power Splitters (MMI : Multimode Interference)



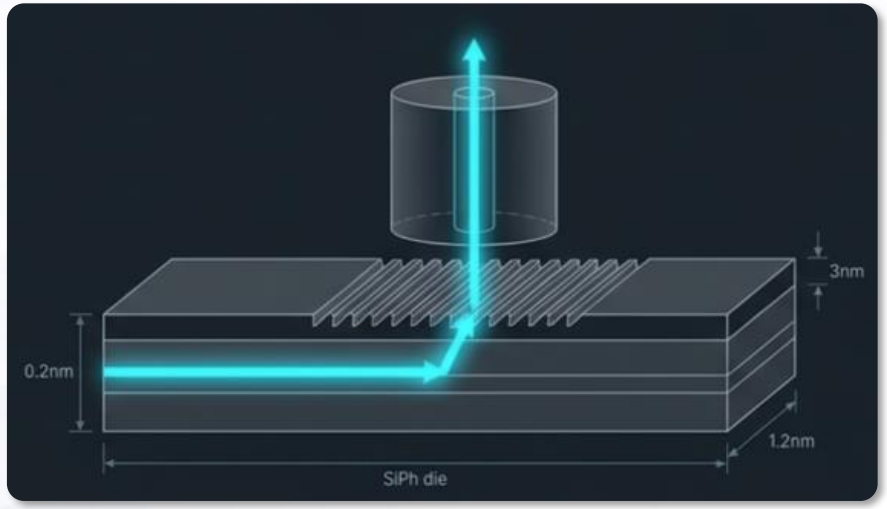
Step4 : Wavelength Division Multiplexing (WDM)

Target KPI

- Crosstalk must be maintained at -20 dB.

Step5 : I/O Coupling Strategy

Grating Couplers



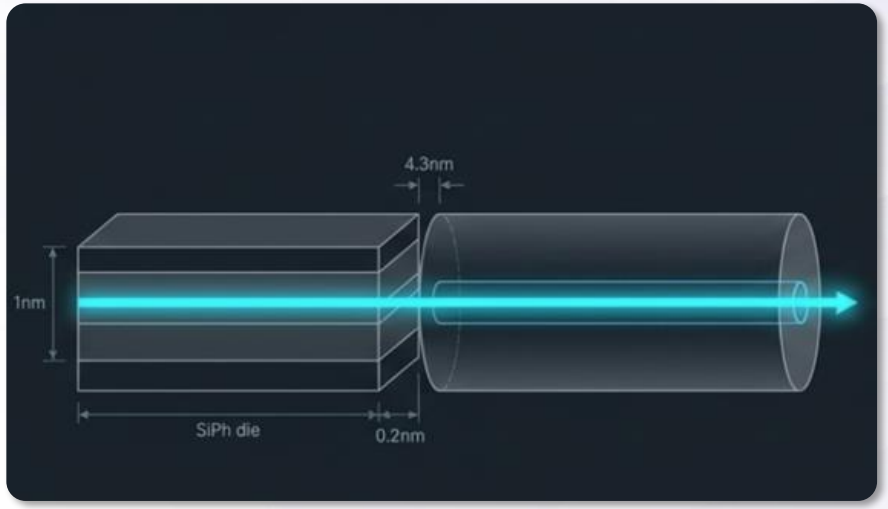
Light enters/exits vertically.

High insertion loss, wavelength sensitive.

Advantage

Enables wafer-level testing (testing from the top before dicing).

Edge Couplers



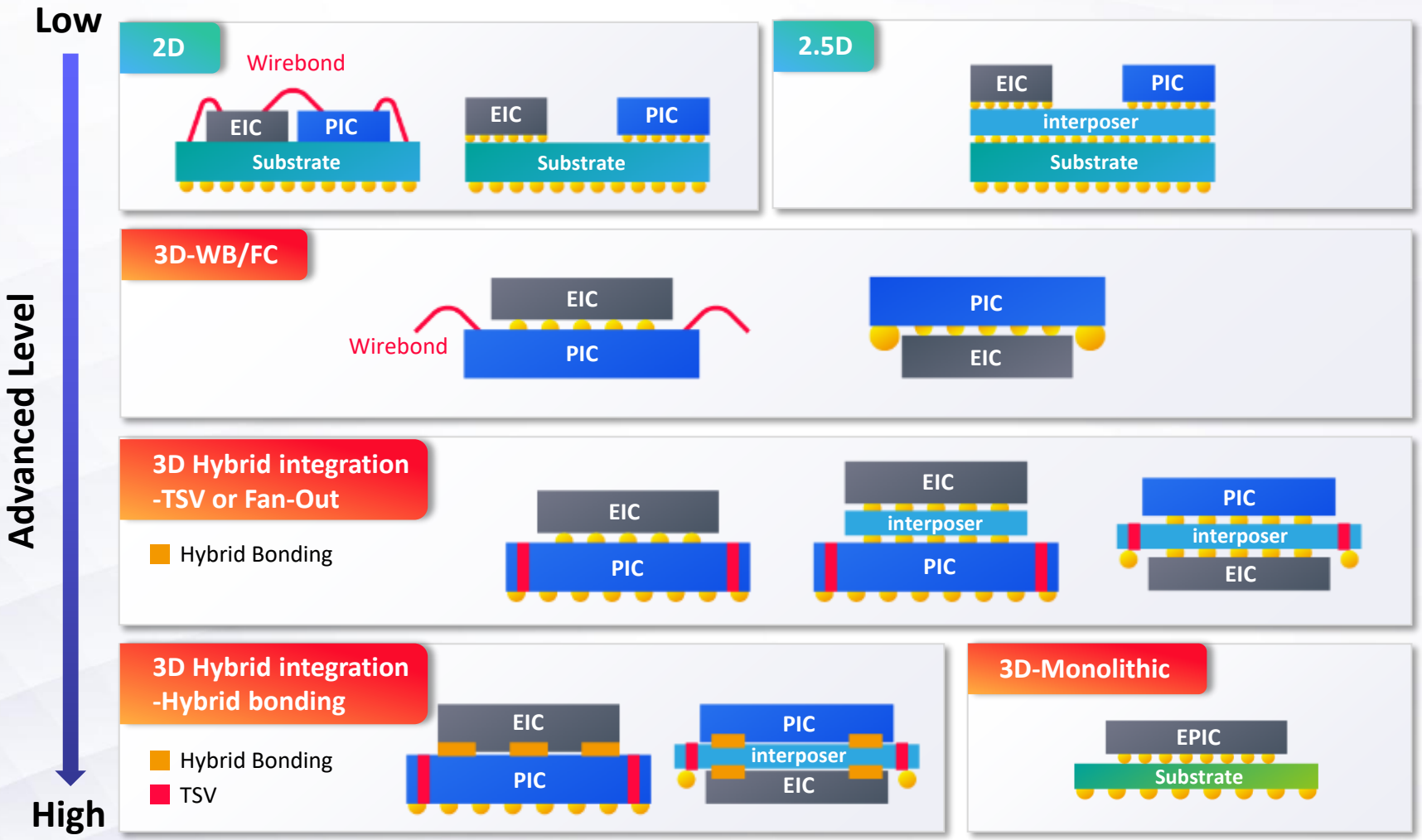
High bandwidth, ultra-low insertion loss (<1.0 dB).

Polarization insensitive. Ideal for 128-core FAU.

Challenge

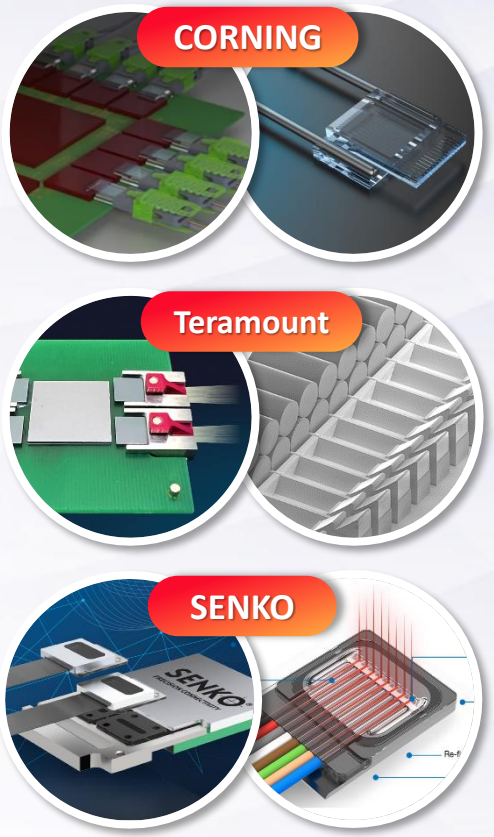
Demands extreme sub-micron alignment precision.

Different Optical Engine Design



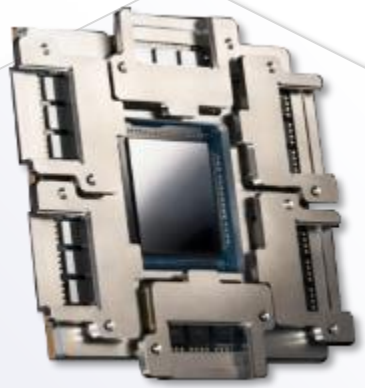
Source : IDTechEx Research

Optical Engine Connector

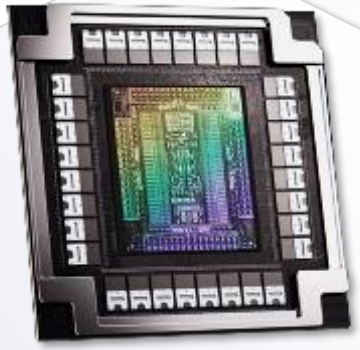


Source : Official Website

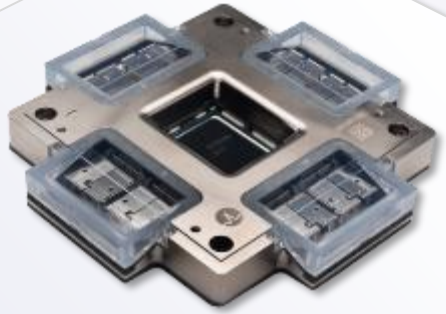
From OE to Module / Spec Diversity



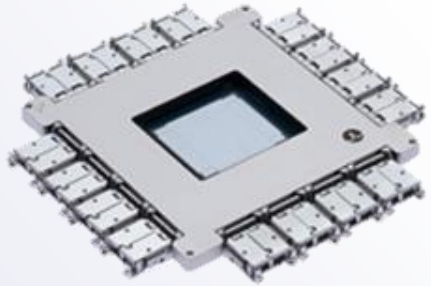
nVIDIA



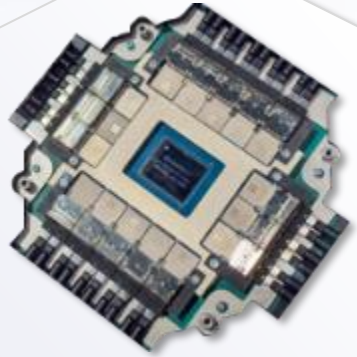
nVIDIA



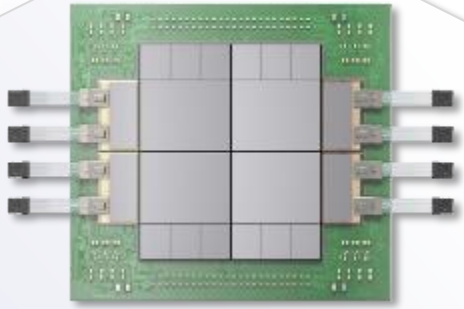
Broadcom



Broadcom



Marvell



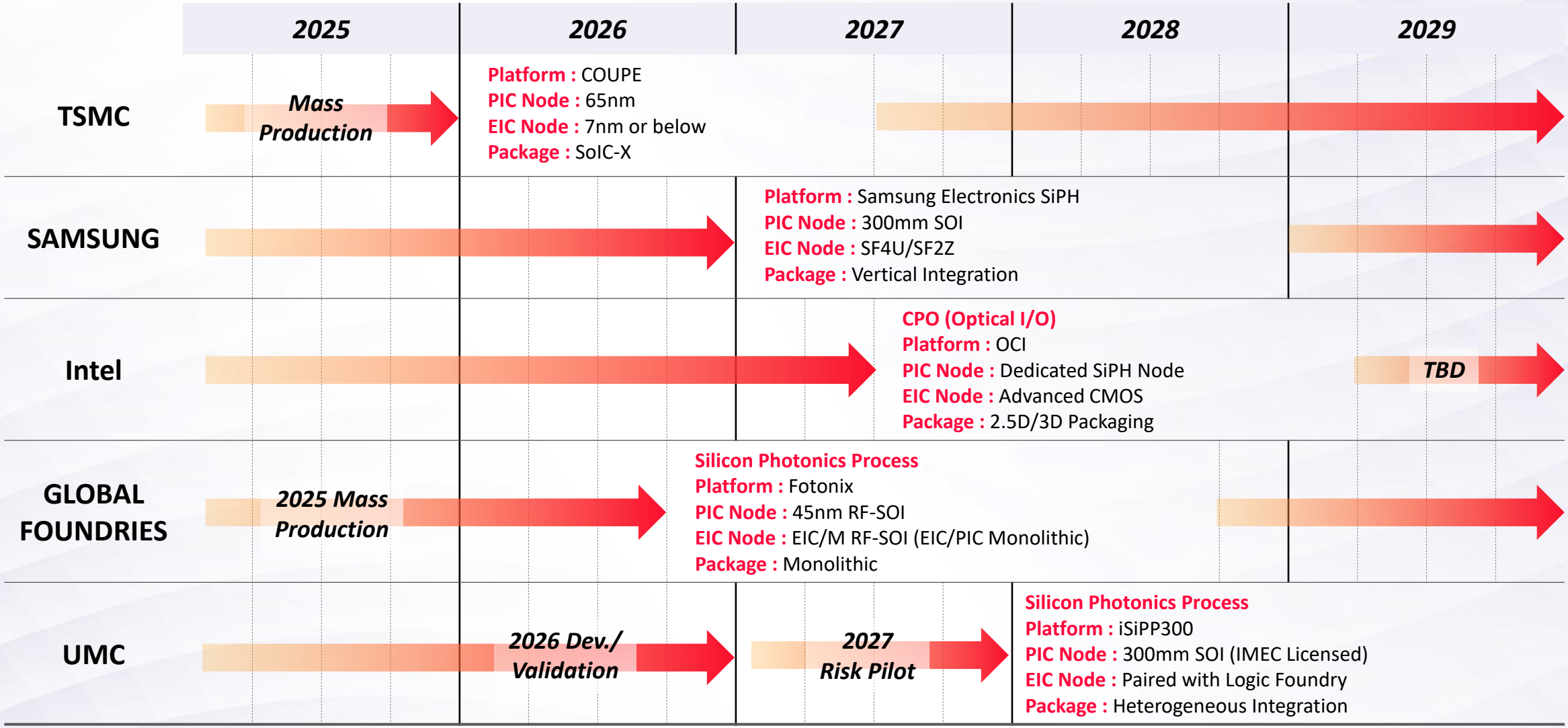
Lightmatter

Lightmatter

AyarLabs

Source : Official Website

Key Foundries of Silicon Photonics and CPO



Source : DIGITIMES, 2026/04

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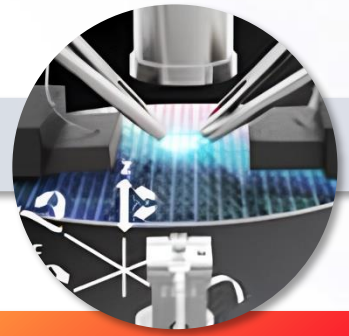
Bottleneck of Testing in CPO Production

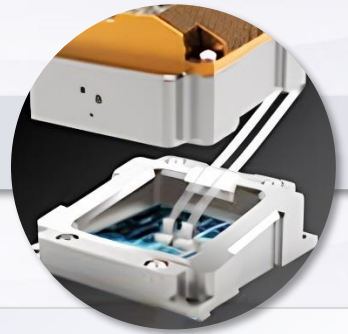
CPO Test Flow / Production Bottle Neck

Active Alignment

Probing PIC Wafer



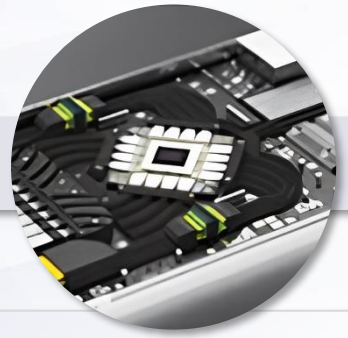
Double-Side Wafer Testing



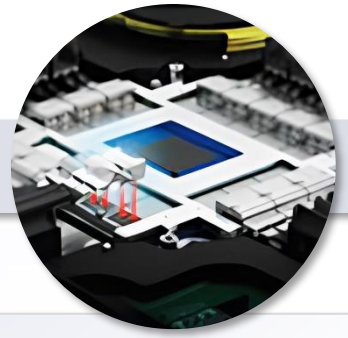
Electro-Optical Testing of Engines

Pick & Place, Plug & Play

Testing of Modules



Testing of Trays



Passive Cable Attachment

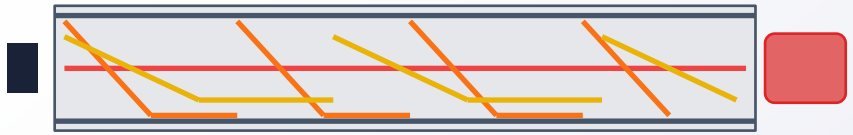
Source: Teradyne

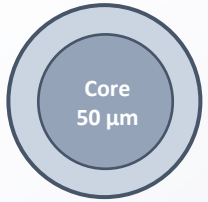
Why Must CPO Use Single Mode Fiber (SMF)?

Multi-Mode Fiber (MMF) Not Suitable for CPO

Modal Dispersion

many modes → different paths → different arrival times





Cross-section

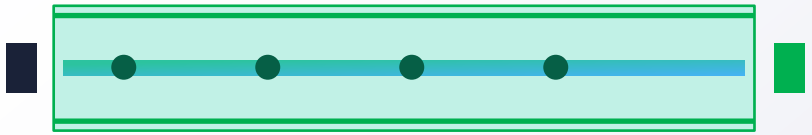
- Hundreds of modes propagate together
- ISI destroys signal beyond ~100 m
- Mismatched with SiPh single-mode waveguide

Result: collapses beyond 100 m or above 100 Gbps

Single Mode Fiber (SMF) The Only Choice for CPO

Single Fundamental Mode

one path → simultaneous arrival → pulse shape preserved



Cross-section

- Supports only 1 fundamental mode
- Maintains signal over 2 km+
- Native match with SiPh waveguide

Result: enables 200 Gbps+ over 2 km+, ideal for CPO deployment

The silicon photonics waveguide itself is single-mode — light leaving the ASIC is fundamental-mode from the start. Using SMF is not a design choice for CPO; it is a physical consequence dictated at the wafer level by the silicon photonics platform.

FAU Active Alignment Challenge

Fiber Roundness

≤0.8μm

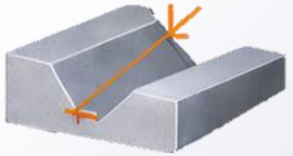
Core Concentricity

≤0.5μm

Fiber Size

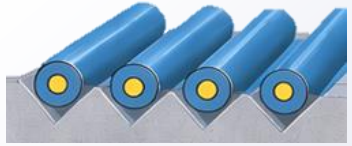
±0.7~1.0μm

V-groove Angle



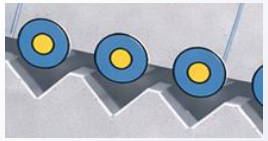
±0.3°

V-groove Depth

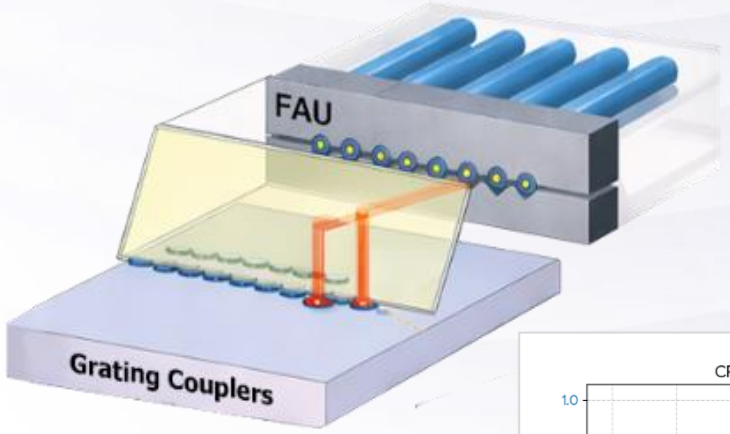


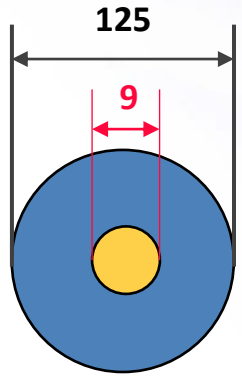
±0.5~1.0μm

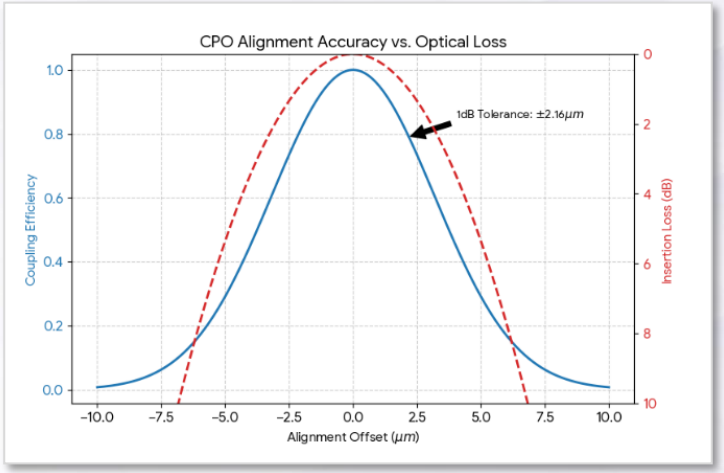
V-groove Pitch



±0.3~0.5μm







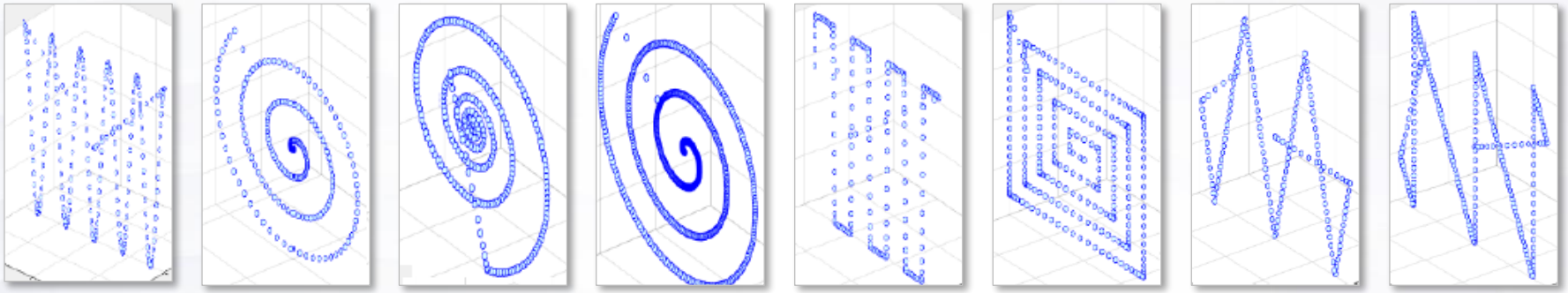
Tolerance Stack-up: 3.8μm | 42% of core diameter.

Active Alignment

Multi-Axis Photonics Alignment System

Hexapod

Piezo System for Nano positioning and Fiber Alignment



CPO Production Assessment

Solution 1 Golden FAU (Fixed Reference Focusing)

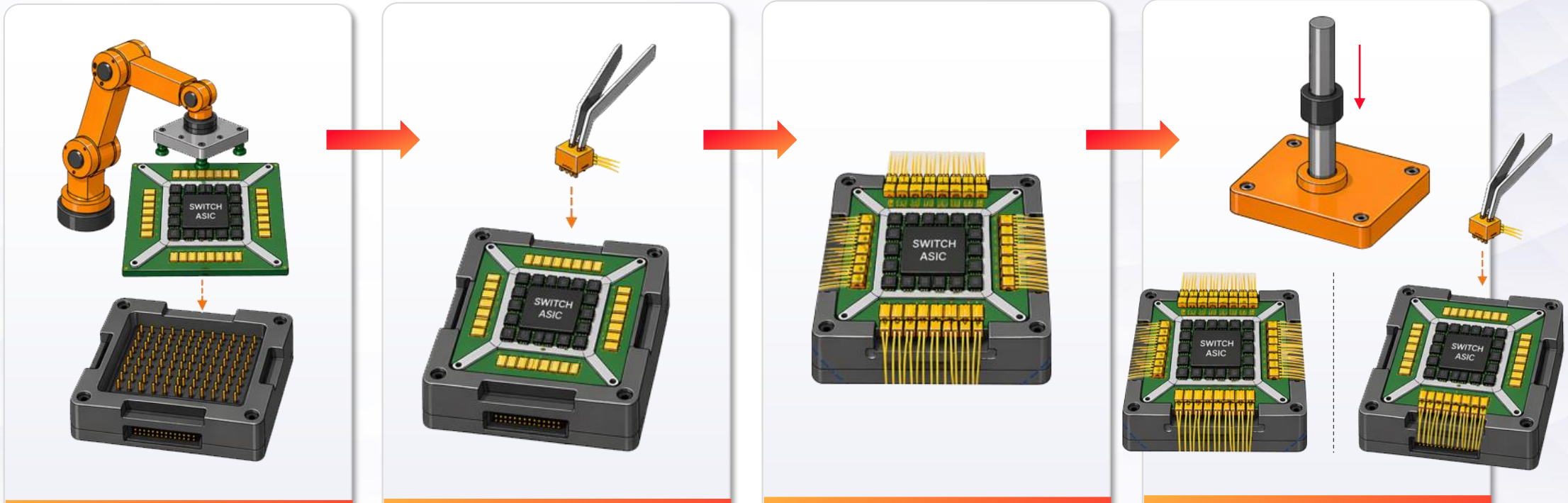
- Establish Golden Device
- Establish Golden FAU
- Move All FAUs to Reference Position
- Verify Focusing Efficiency
- Focusing efficiency ≥ 99% ?
  - No → Find Adjustment
  - Yes → Normal Production

Solution 2 Self-align (Auto Focus Calibration)

- Measure Intrinsic Component Variation
- Build Auto Calibration Model
- Auto Focus Calibration
- Verify Focusing Efficiency
- Focusing efficiency ≥ 99% ?
  - No → Find Adjustment
  - Yes → Normal Production

Module Test Challenge

Pick & Place, Plug & Play



Pick & Place

Handler places CPO IC into socket

Place FAUs

Selective placement of individual fiber arrays

Plug All FAUs

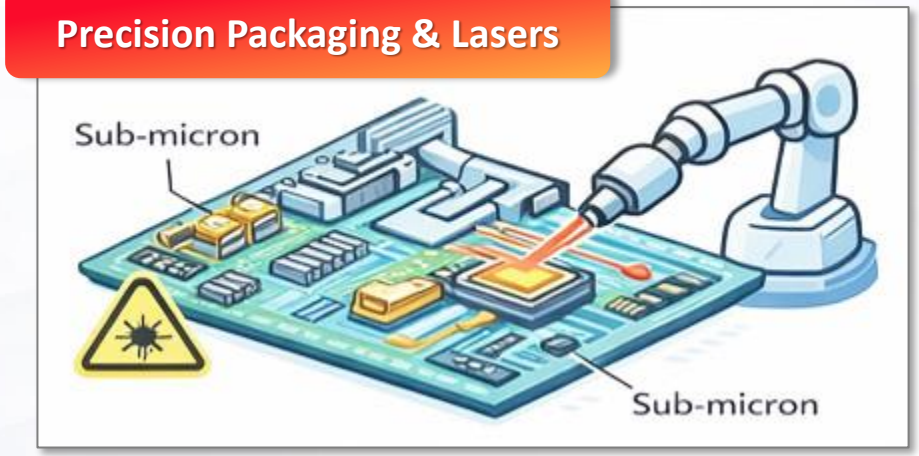
Complete FAU connection around the perimeter

Plug & Play

Full contact established, testing sequence begins

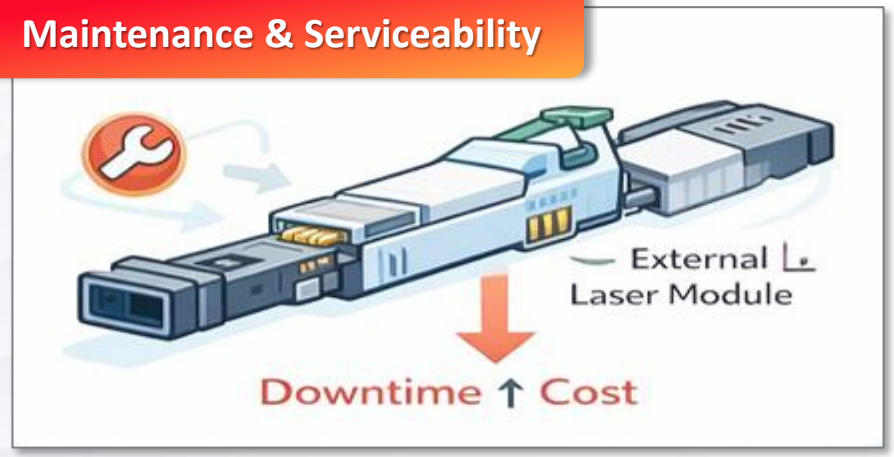
CPO Production Bottleneck
Four Technical Issues

Precision Packaging & Lasers



Lack of Standardization

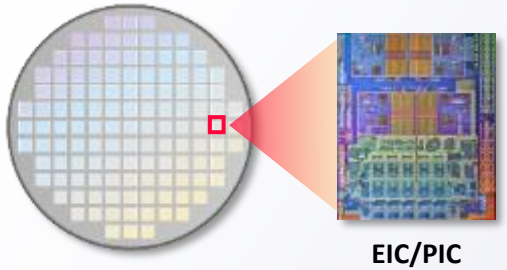
Maintenance & Serviceability



Yield & Cost Risk

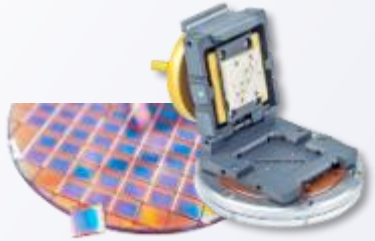
Co-Packaged Optics Test Flow

Wafer Level → Die Level



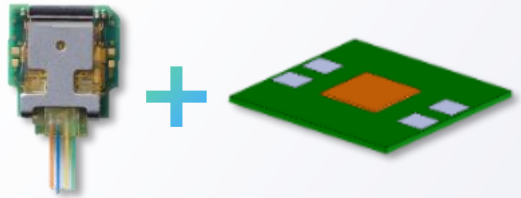
EIC/PIC Wafer

EIC/PIC Die



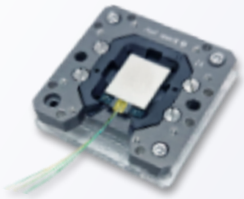
WLCSP Fine Pitch Probe Head
(EIC/PIC Wafer test)

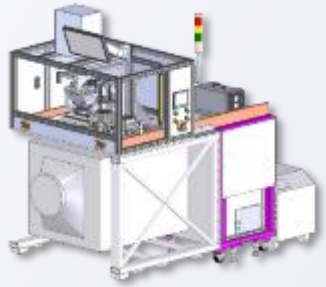
Package Level



Optical Engine

CPO Substrate

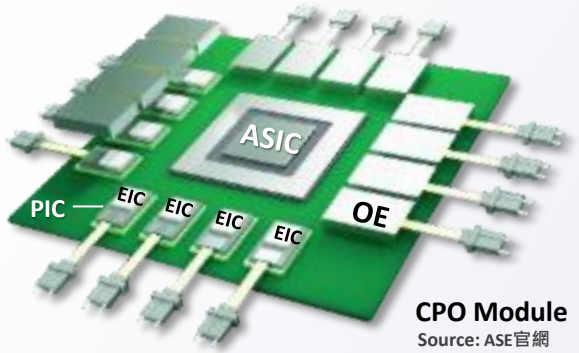




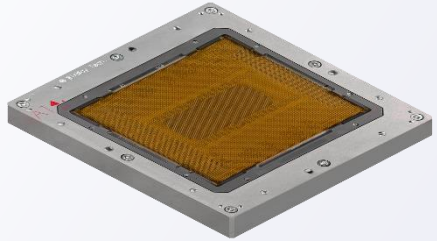
Optical and Electrical Test Socket
(Optical Engine)

Double Sided Probing System

Module Level



CPO Module
Source: ASE官網



HyperSocket™

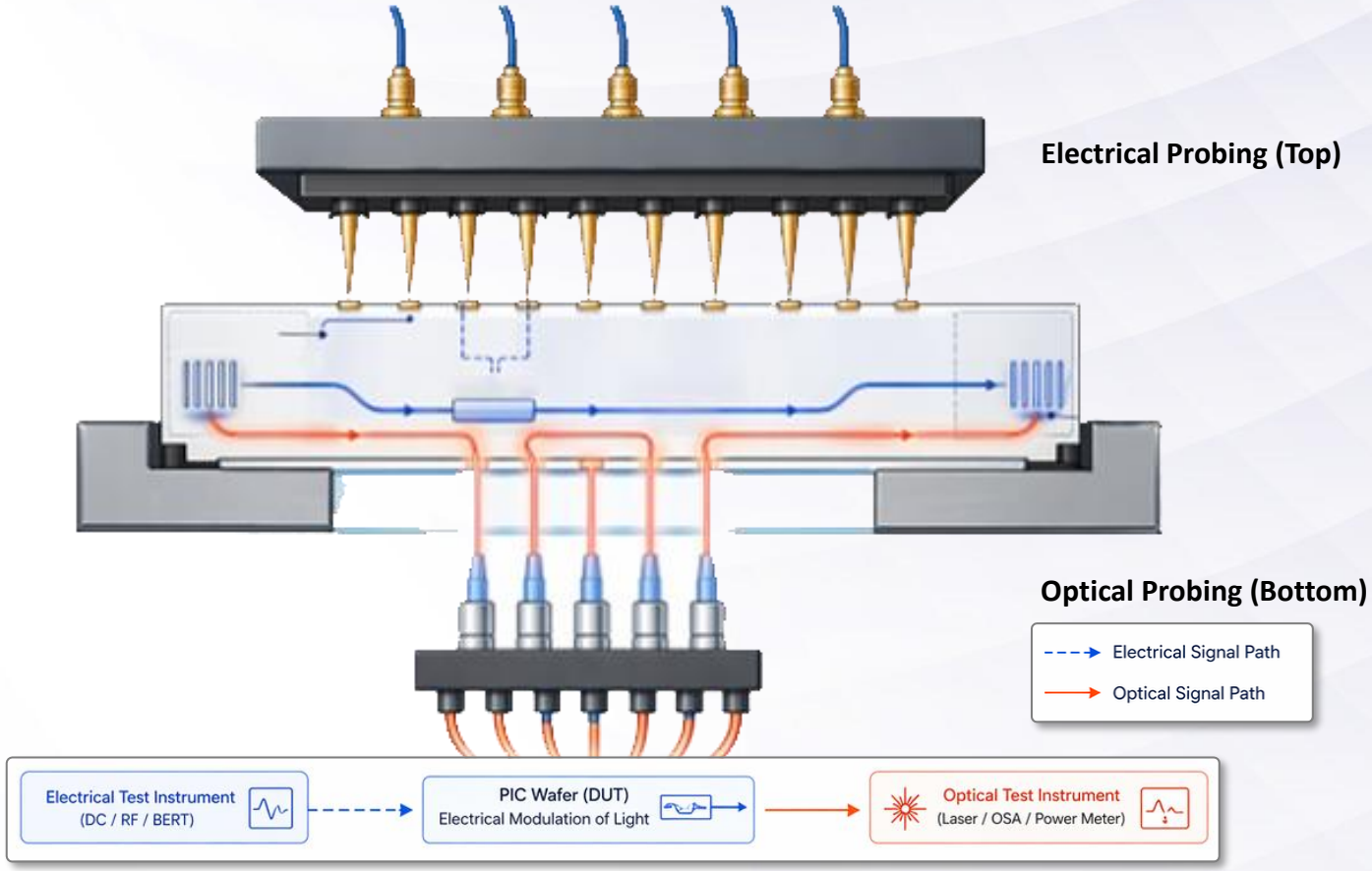
Wafer Level Test Methodology

Wafer Level Test

EIC/PIC Wafer

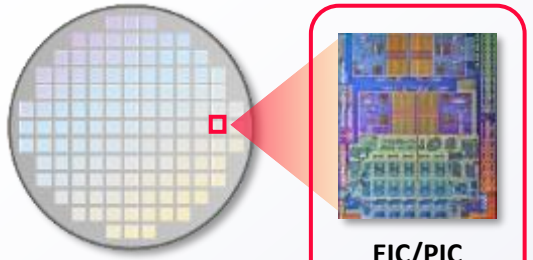
WLCSP Fine Pitch Probe Head
(EIC/PIC Wafer Test)

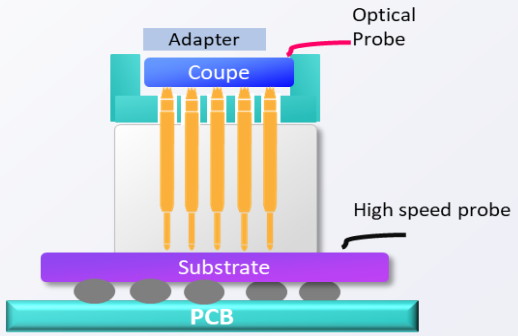
Test Requirement Electrical at TOP / Optical at BTM.



Die Level Test Methodology

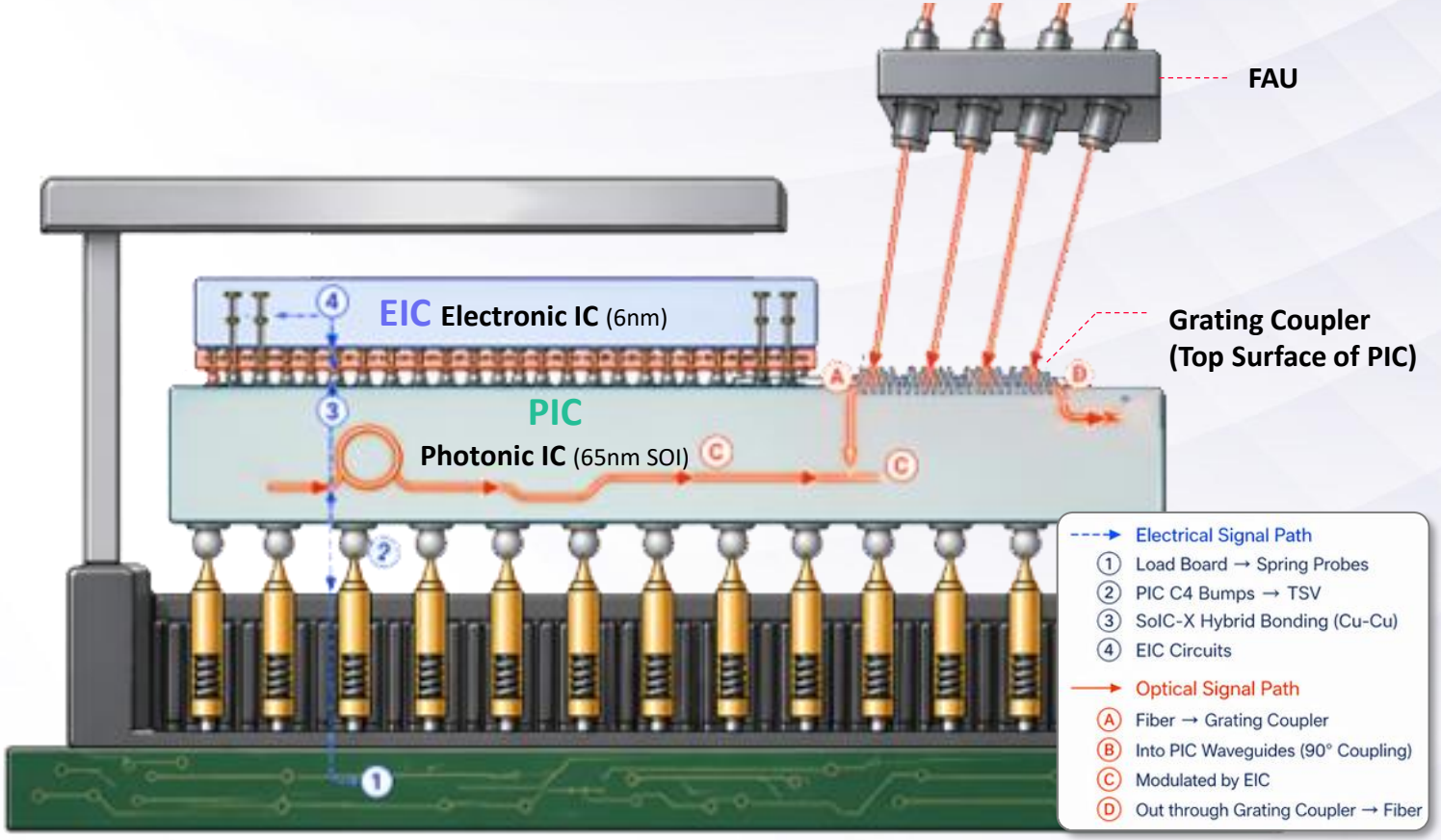
Die Level Test





WLCSP Fine Pitch Probe Head
(EIC/PIC Wafer Test)

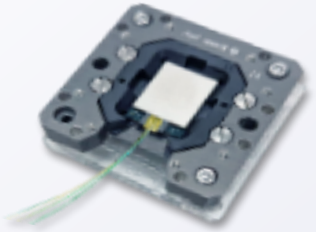
Test Requirement Optical at TOP / Electrical at BTM.



Package Level Test Methodology

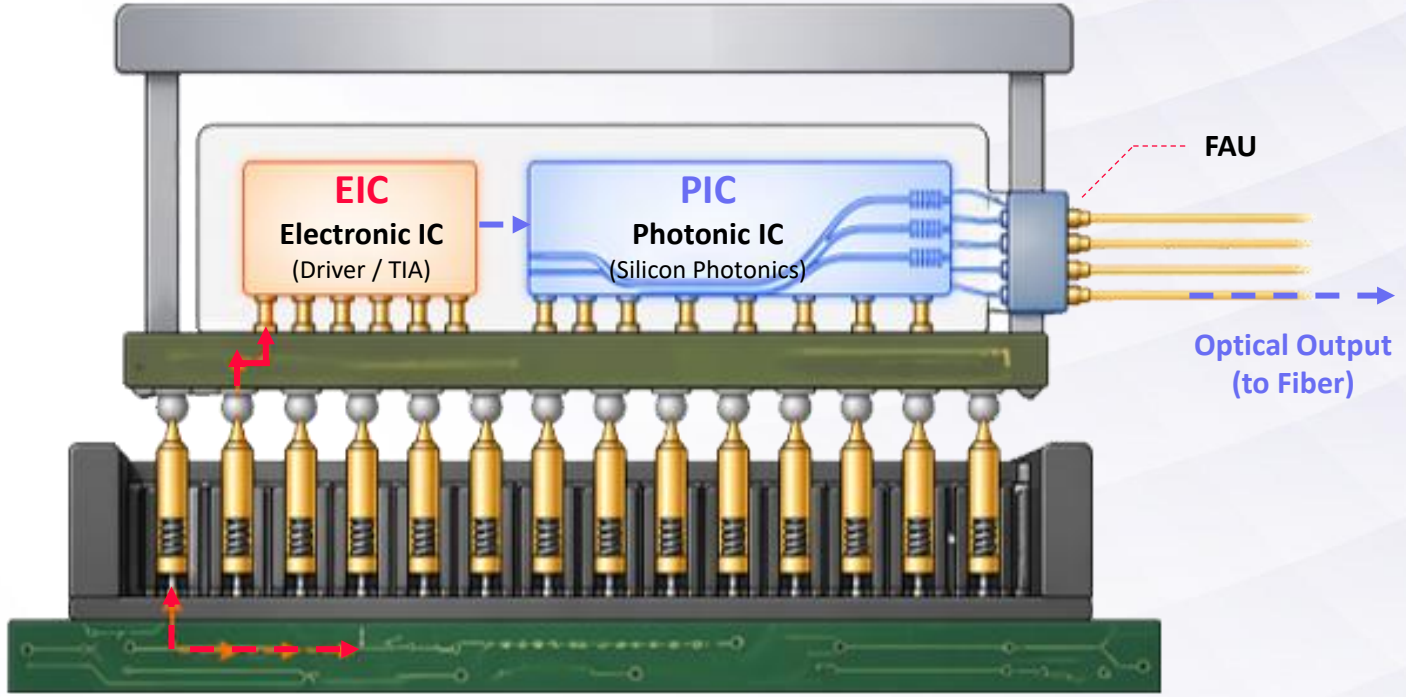
Package Level Test

Optical Engine



Optical and Electrical Test Socket
(Optical Engine)

Test Requirement Active alignment , Passive alignment, Direct with FAU

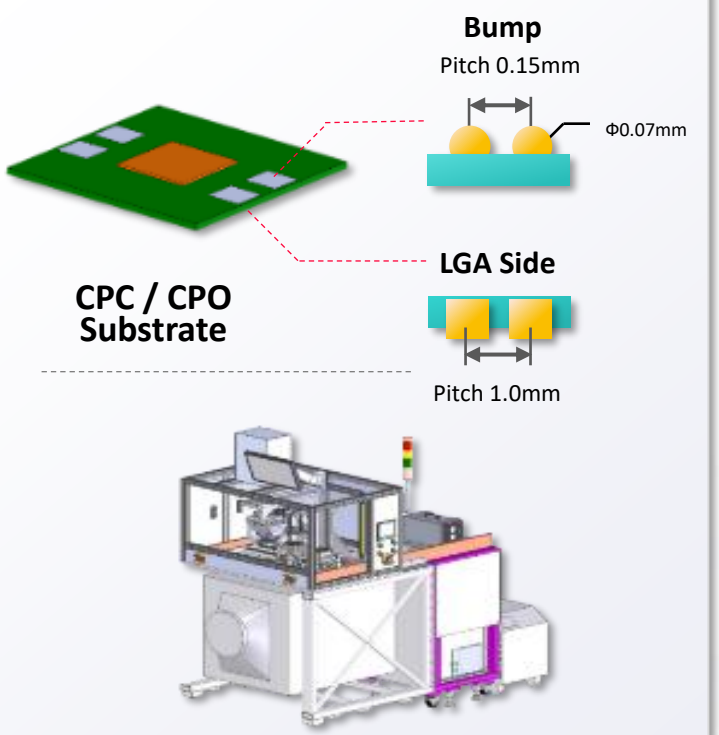


Electrical Signal Path
(Load Board → EIC)

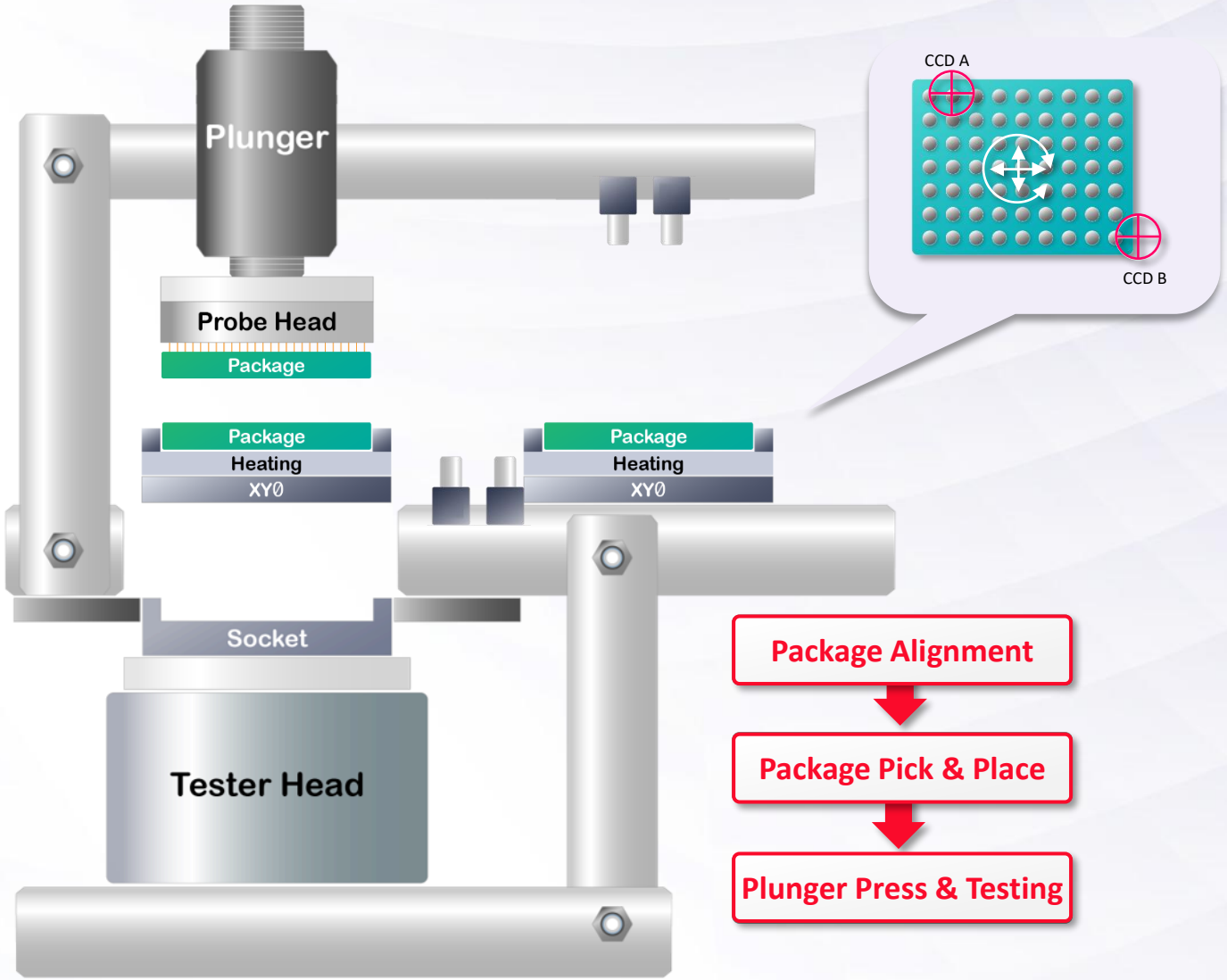
Optical Signal Path
(EIC → PIC → Fiber)

Package Level Test Methodology

Package Level Test



Double Sided Probing System



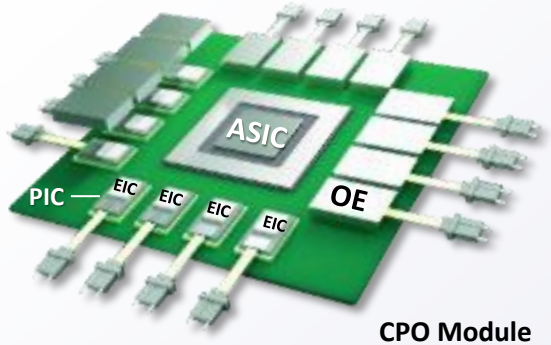
Package Alignment

Package Pick & Place

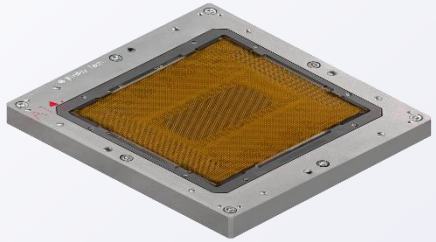
Plunger Press & Testing

Module Level Test Methodology

Module Test

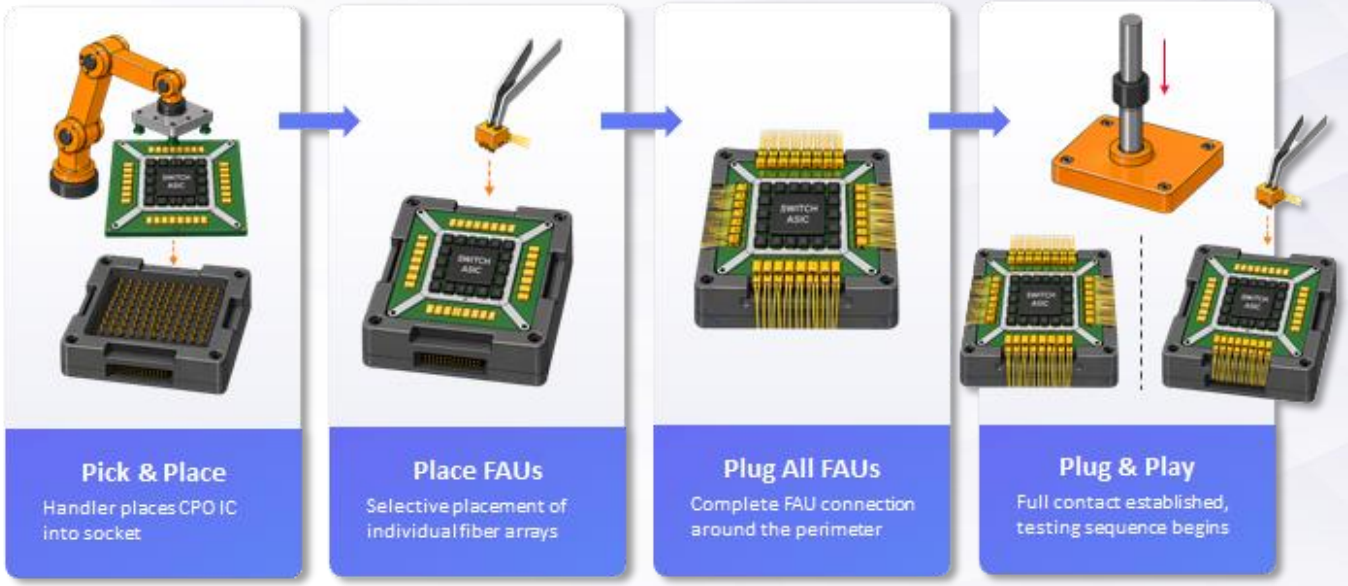


CPO Module
Source: ASE官網



HyperSocket™

Test Requirement Test speed, Alignment, Mechanism Design.



Pick & Place
Handler places CPO IC into socket

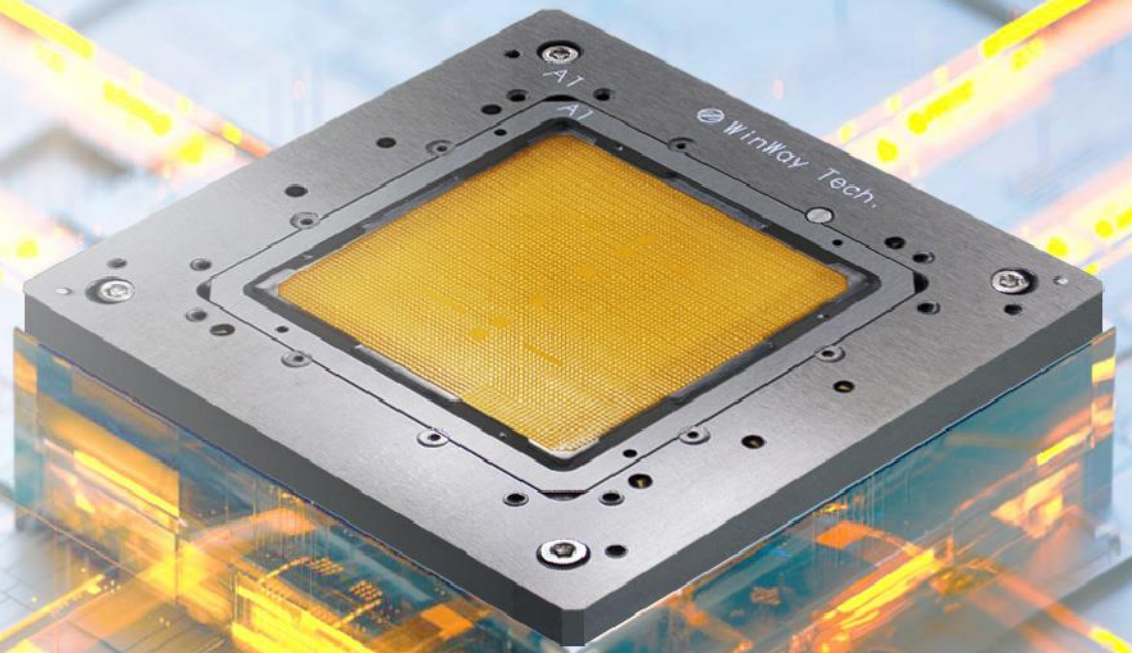
Place FAUs
Selective placement of individual fiber arrays

Plug All FAUs
Complete FAU connection around the perimeter

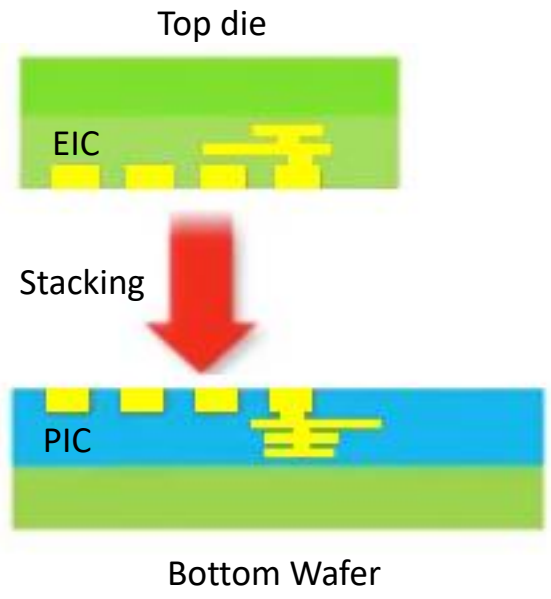
Plug & Play
Full contact established, testing sequence begins

WinWay
穎崴科技

CPO Roadmap

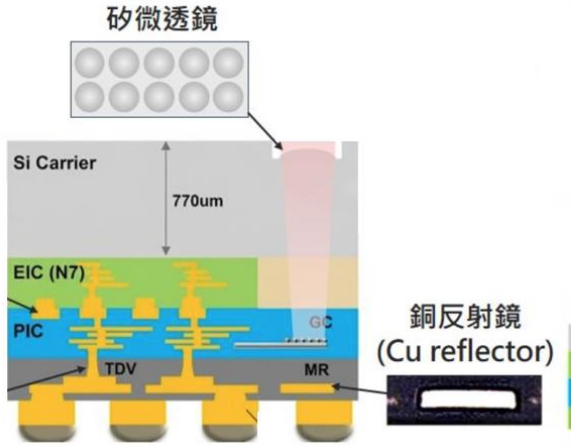


COUPE : COmpact Universal Photonic Engine

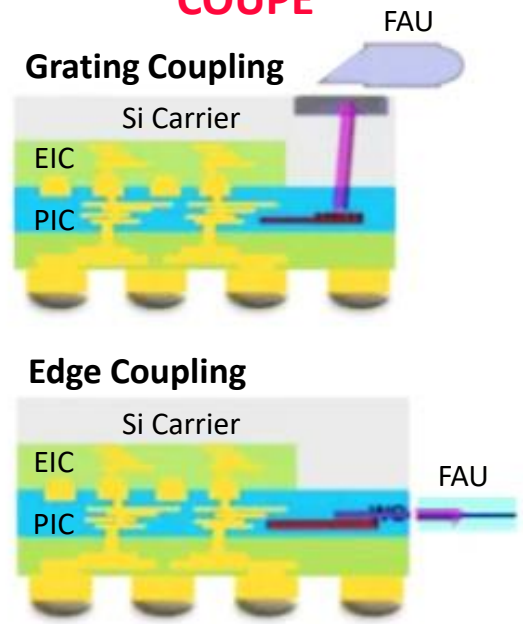


TSMC-SoIC Bond:

EIC die on PIC wafer

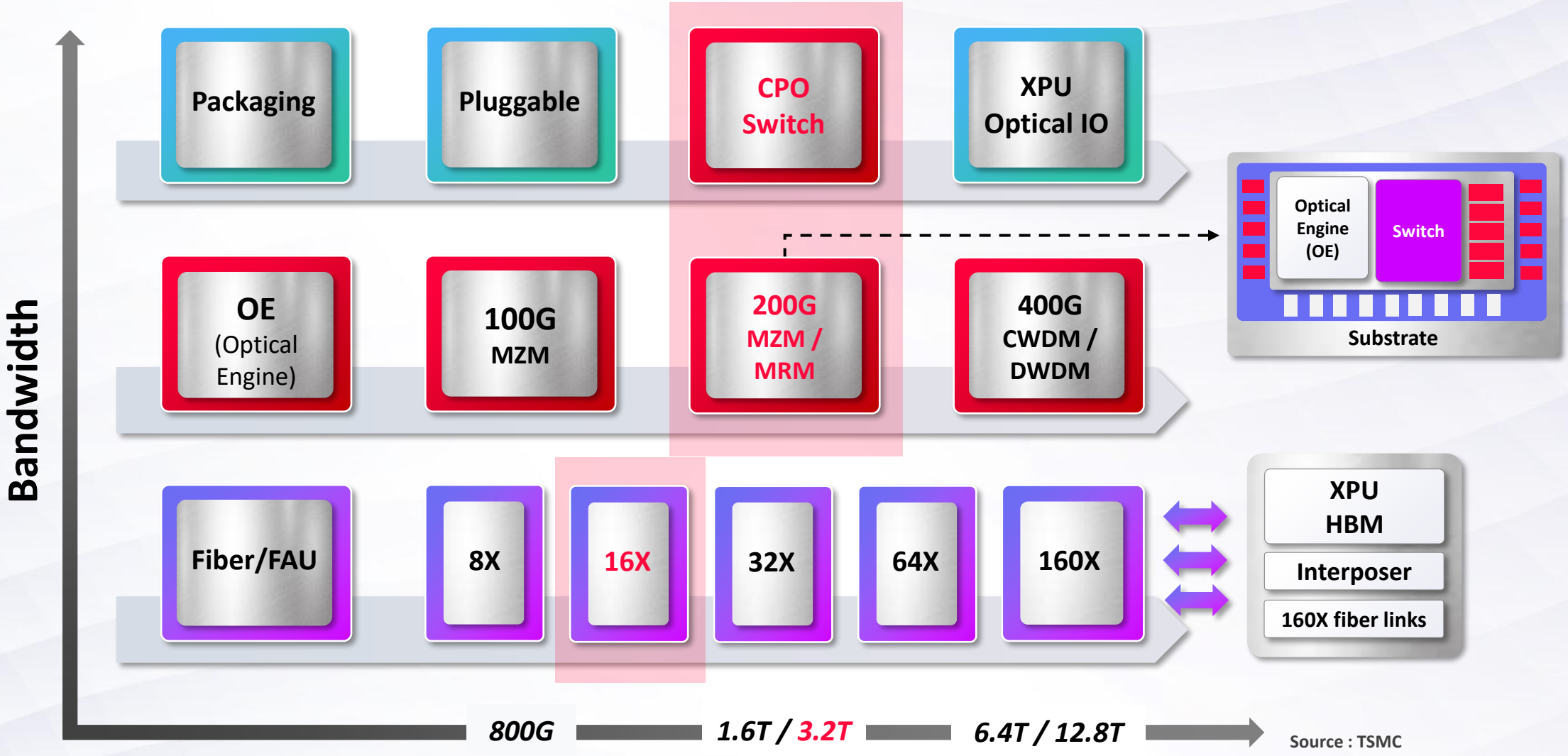


COUPE



Source : TSMC

CPO Roadmap

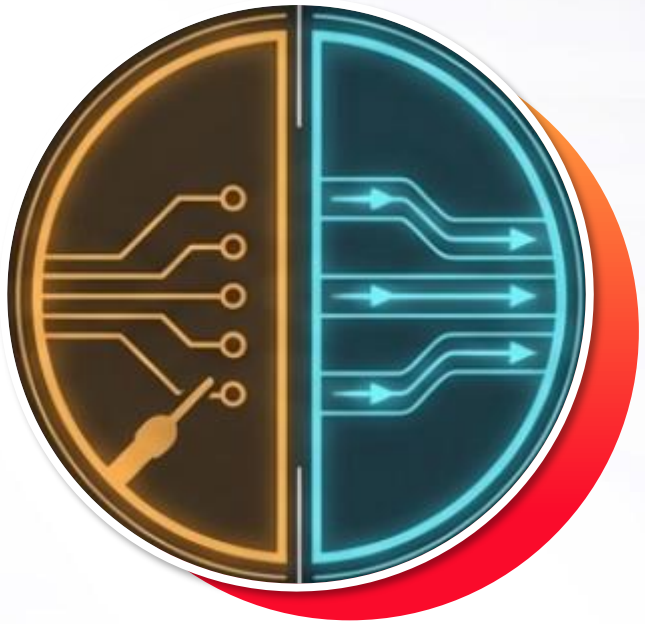


Source : TSMC

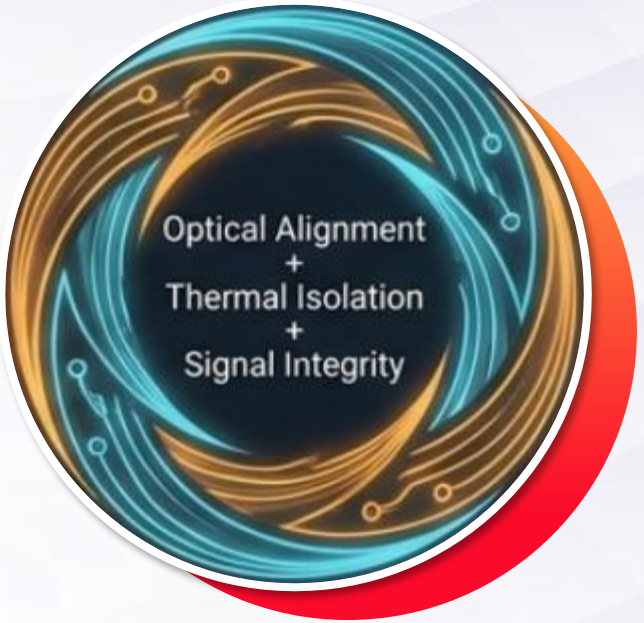
The I/O Interface Evolution

The Past
Electrical Interface

The Present
Electro-Optical Interface



The Future(102.4T+)
Co-Design Architecture



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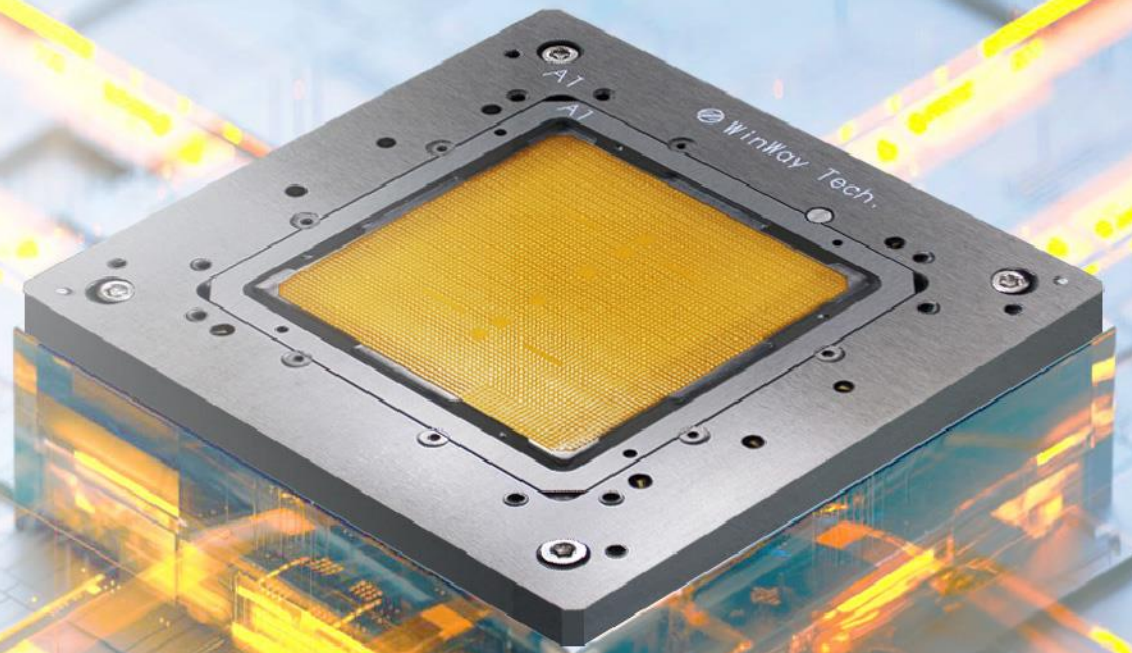
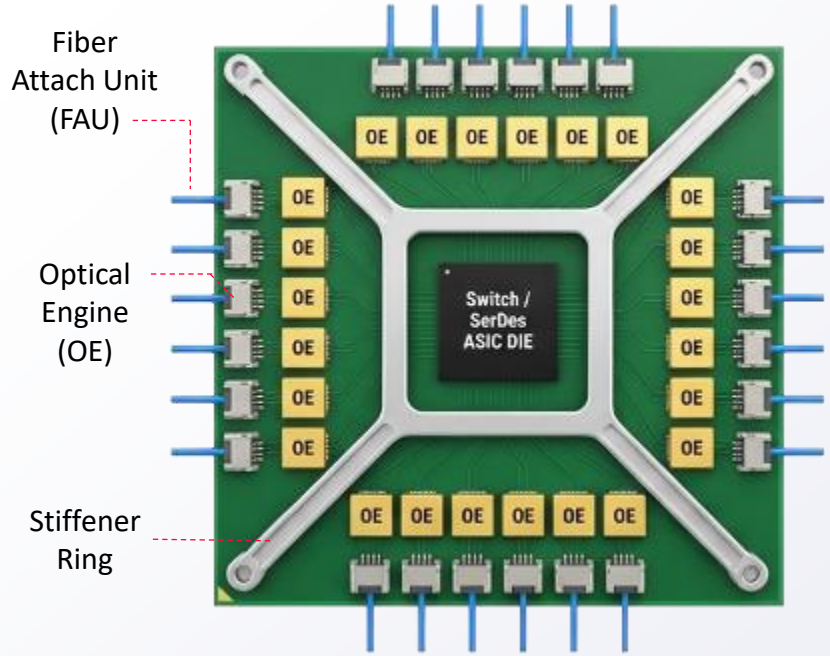
CPO/CPC Application



CPO / CPC Application

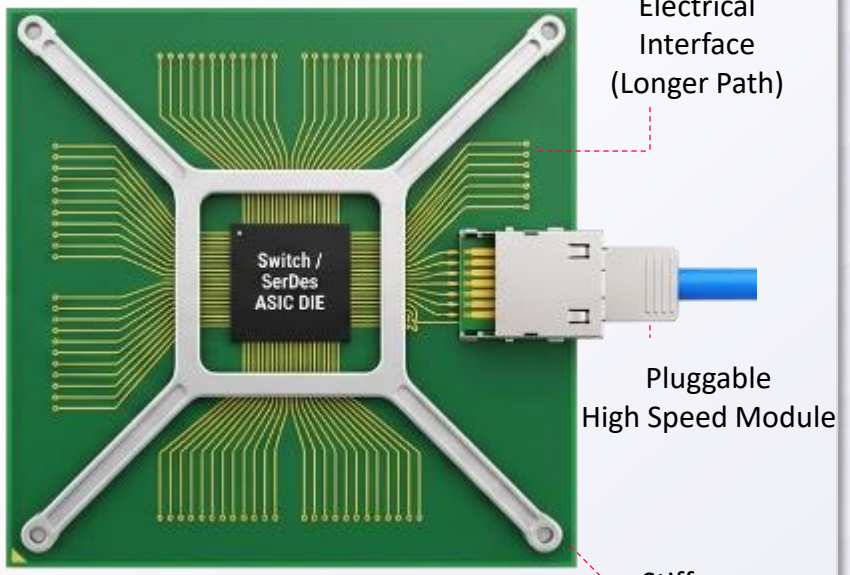
CPO Architecture (Co-Packaged Optics)



- Very short Electrical path (mm level)
- High bandwidth density
- Lower power consumption
- Requires optical alignment & advanced test

Switch / SerDes ASIC DIE

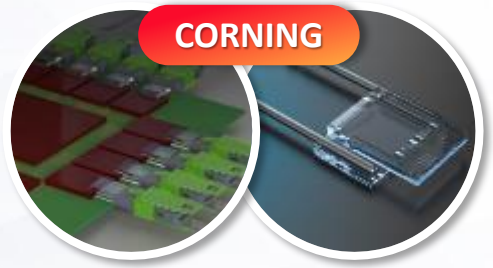
CPC Architecture (Co-Packaged Copper)



- Longer electrical Path (cm level)
- Hot-swappable & field replaceable
- Higher power consumption
- Mature ecosystem & cost-effective solution

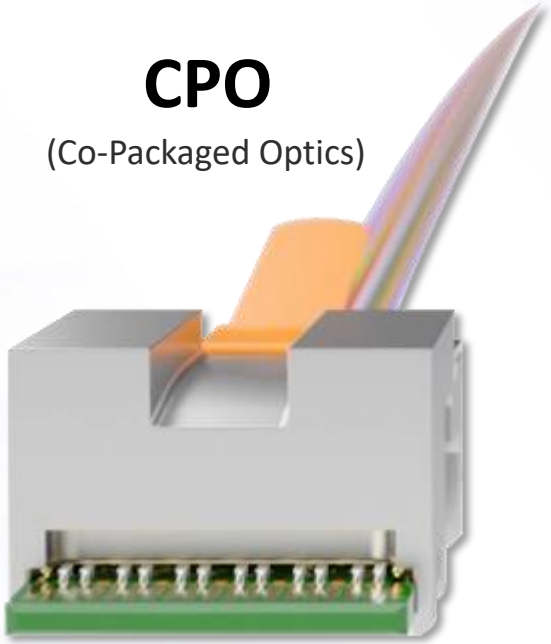
CPO / CPC Application

Pitch: 0.35mm



CPO

(Co-Packaged Optics)

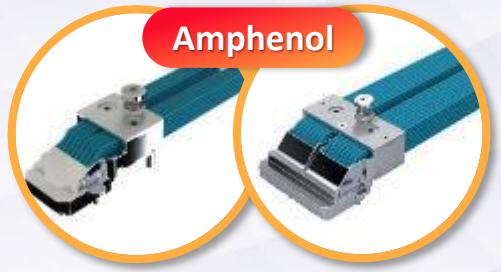


Optical

CPC

(Co-Packaged Copper)

Copper



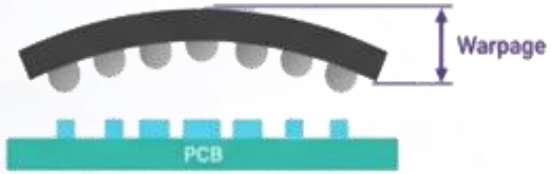
Source : Official Website

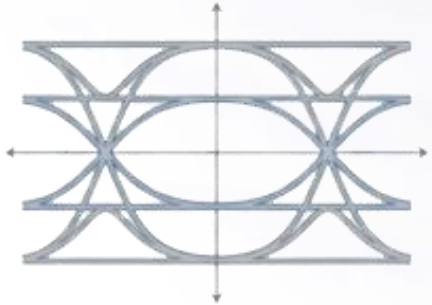
WinWay
穎崴科技

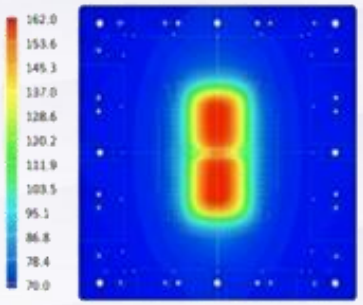
WinWay CPO/CPC Total Solution

Future Technical Challenge

A. Mechanical Extremes	B. Electrical Performance Barriers	C. Thermal Density Crisis







- **Package Size** > 100 mm up to 200mm
- **Pin Count** > 10,000 pins up to 50,000 pins
- **Key Challenge** Warpage up to 0.6mm

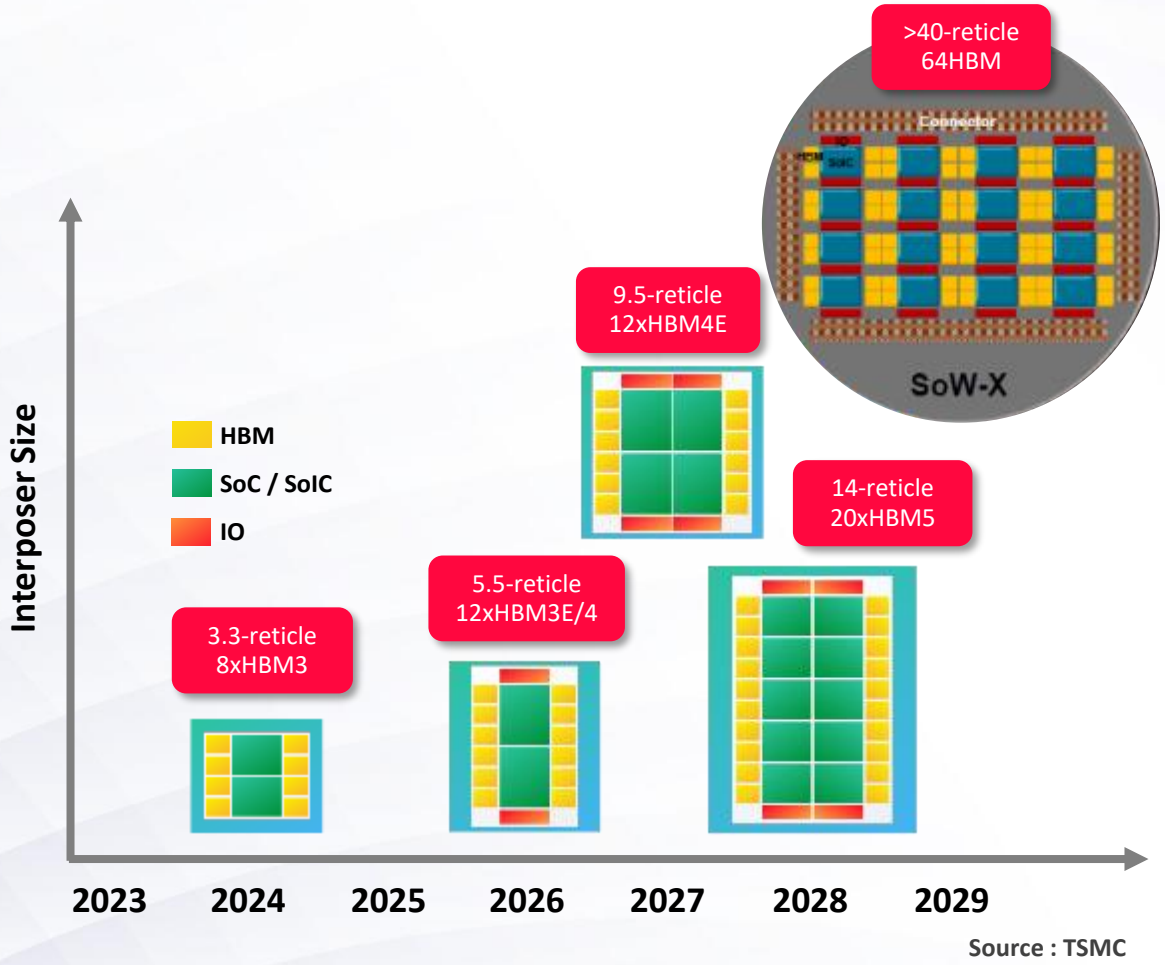
- **Signal Speed** 224Gbps PAM4 and beyond
- **Key Challenge** Signal Integrity, Crosstalk

- **Power Consumption** > 4000W per device
- **Key Challenge** Thermal Runaway / Solder Melt

Technical Development Direction to “Optics”

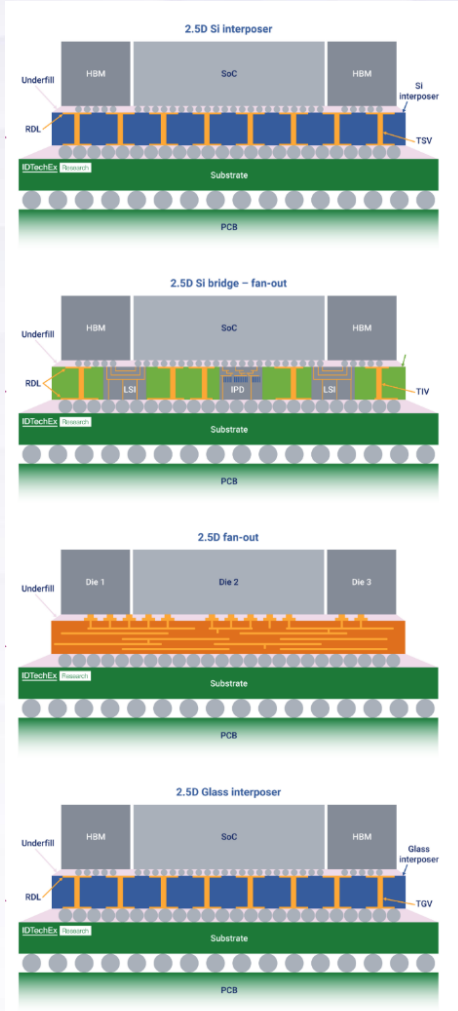
The challenges of package testing have evolved from a focus on mechanical machining accuracy **to multi-physics coupled design**, encompassing **mechanical integrity, electrical performance, thermal management.**

A. Mechanical Extremes / TSMC



Source : TSMC

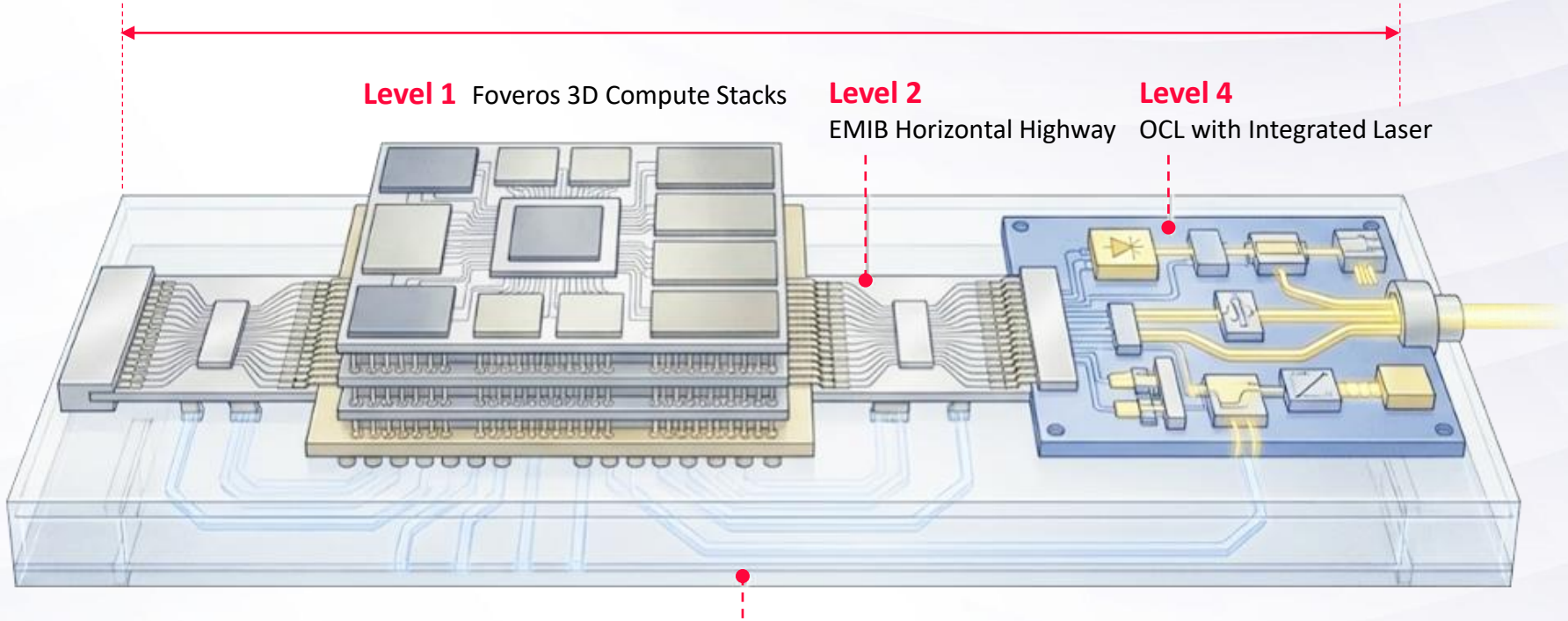
Si-based Interposer	CoWoS-S (Si Interposer)
	CoWoS-L (Si bridge)
Organic-based Interposer	CoWoS-R (Organic fan-out RDL)
Glass-based Interposer	CoPoS/Panel Level Package (Glass interposer)



Source : IDTechEx Research

Package size dimension determine by # of Die, Memory, High Speed I/O Channel, Manufacturing limitation…

A. Mechanical Extremes / Intel



Level 1 Vertical :
Faveros Hybird Bonding enables extremely dense die-to-die logic stacking

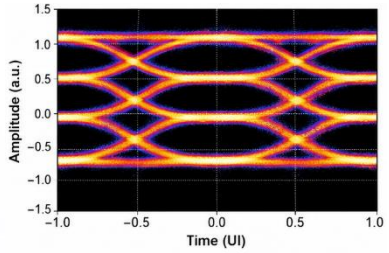
Level 2 Horizontal :
EMIB enables high-bandwidth, low-latency links between XPU, Memory, and Optics

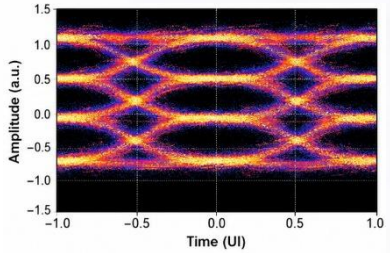
Level 3 Platform :
Glass Substrates provide the ultra-flat, thermally stable foundation required for massive package footprints

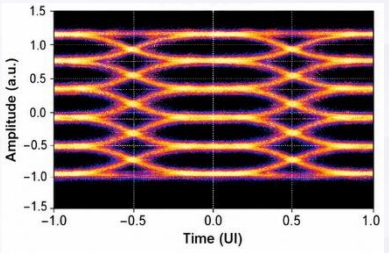
Level 4 Output :
The OCI translates massive electrical bandwidth into scalable, laser-driven optical interconnects

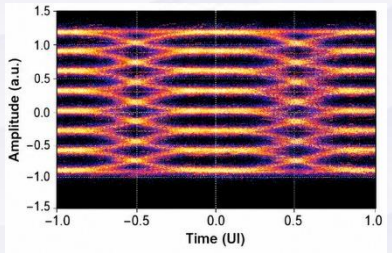
Source : Intel

B. Electrical Performance Barriers



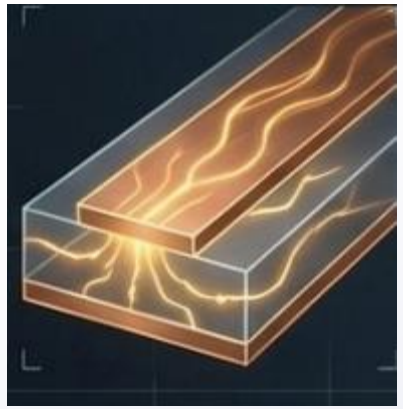






Parameter	224G (PAM4)	448G(PAM4)	448G(PAM6)	448G(PAM8)
Data rate	224Gbps	448Gbps	448Gbps	448Gbps
Bits / Symbol	$\log_2(4)$=2	$\log_2(4)$=2	$\log_2(6)$~2.58	$\log_2(8)$=3
Baud Rate	112 GBaud	224 GBaud	~173.6 GBaud	~150 GBaud
Nyquist Freq.	56GHz	**112GHz**	86.8 GHz	**74.7GHz**
SNR Penalty	0 dB (Ref)	0 dB (Ref)	**-3.7 dB**	**-6.2 dB**
DSP Complexity	Medium	High	Higher	Highest
Pros	Mature ecosystem : Feasible on standard PCB/Cable	Simple architecture : Best theoretical SNR.	Goldilocks Choice : Balances BW & SNR.	Low Baud Rate for 448G target
Cons	Requires 2X lanes to match 448G total rate.	**Bandwidth Wall** : Unfeasible for copper	SNR Penalty : Complex encoding logic	**SNR Cliff** : Requires powerful FEC

The 448G Electrical Wall



Copper Channel Loss

Insertion loss approaches -10dB on just 1 inch of premium dielectric at 112 GHz Nyquist.

The Skin Effect Limit

At > 100GHz, skin depth drops below 0.2 um

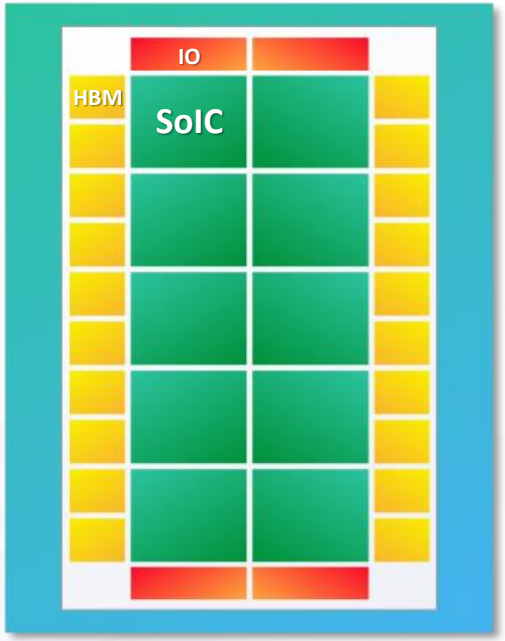
Dielectric Loss Multiplier

Loss scales linearly with frequency.

DSP Power Explosion

Compensating for physical loss requires ADC sampling > 224 GS/s.

C. Thermal Density Crisis

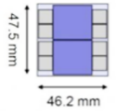
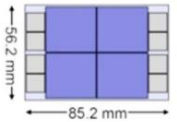
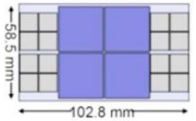
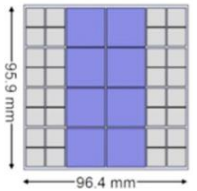


1 reticle Max. ~830mm²

Chip heat density design reference :

1.1~2 W/mm²

- Advanced Thermal Control System
- Higher CCC requirement (>6A/pin)

GPU Architecture	2026 *AI Chip*	2029	2032	2035
GPU Die Size	728 mm²	750 mm²	700 mm²	600 mm²
GPU Power	800 W	900 W	1,000 W	1,200 W
Interposer Size ■ GPU ■ HBM ■ Interposer				
# of GPU Dies	X2	X4	X4	X8
# of HBM Stack	HBM4 X8	HBM5 X8	HBM6 X16	HBM7 X32
HMB Power per Stack	75 W	100 W	120 W	180 W
Interposer Die Stack	2,198 mm² (46.2 mm x 48.5 mm)	4,788 mm² (85.2 mm x 56.2 mm)	6,014 mm² (102.8 mm x 58.5 mm)	9,245 mm² (96.4 mm x 95.9 mm)
Total Bandwidth	16/32 TB/s	48 TB/s	128/256 TB/s	1,024 TB/s
Total HBM Capacity	288/384 GB	400/500 GB	1,536/1,920 GB	5,120/6,144 GB
Total Power	**2,200 W**	**4,400 W**	**5,920 W**	**15,360 W**

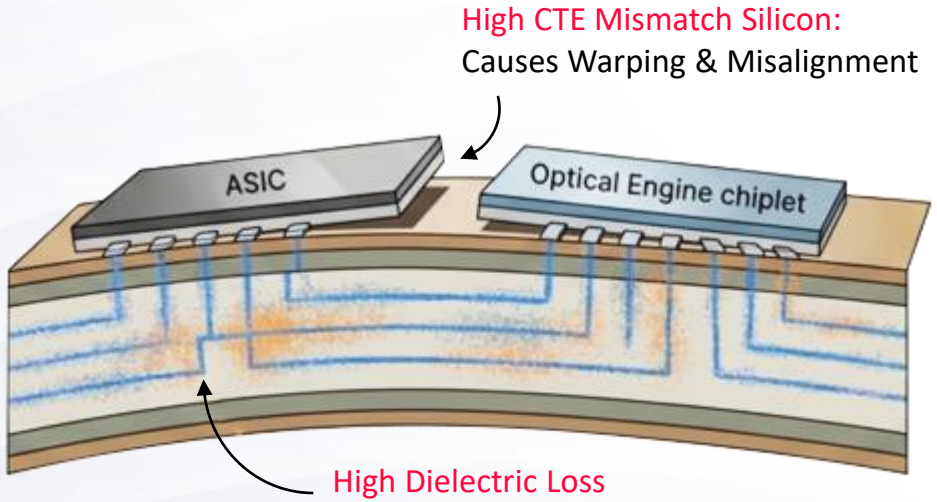
Source : KAIST TERALAB

A+B+C : Heterogeneous Integration

CPO is the path to success in near future

The Problem with Organic Substrates

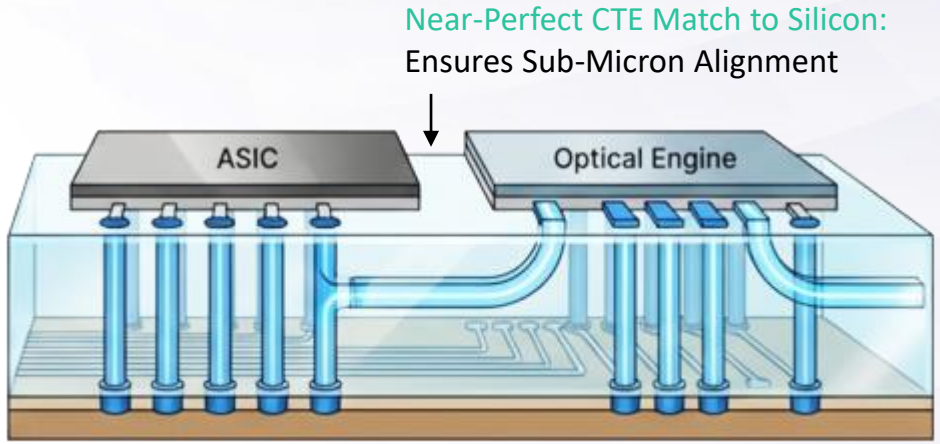
- Thermal / Mechanical Instability
- Electrical Loss



Organic Substrate

Why Glass is the Breakthrough Solution

- Superior Stability
- Pristine Electrical Performance
- Advanced Integration



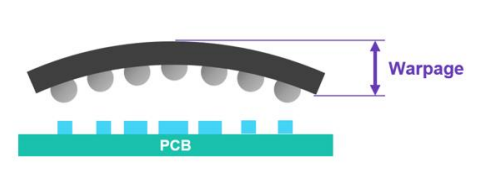
Glass interposer / Substrate

Challenges of Advanced Package Test Solutions

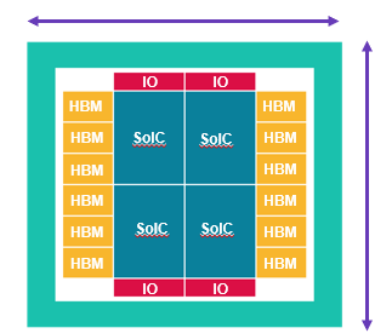
Ultra Large Package

>100X100mm²

- PKG Warpage
- PKG Dimension Tolerance
- Bent pin



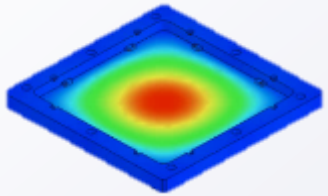
Warpage > 0.4mm



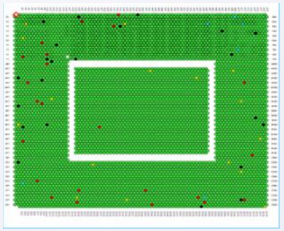
High Pin Count

>20KPin

- Preload force
- Maintenance
- Random fail concern



Housing Warpage by Preload

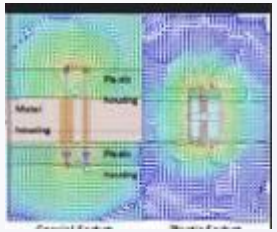


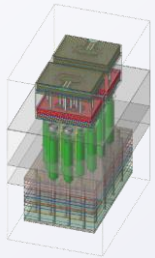
Contact Resistance random fail
(If 20 pin fail/20,000~0.1%)

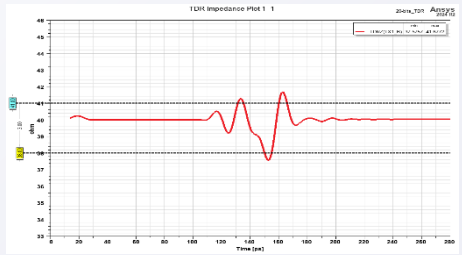
High-Speed Testing

>224Gbps

- Insertion Loss / Return Loss / Crosstalk
- Impedance need precise control





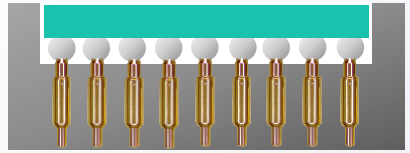


High Heat Density

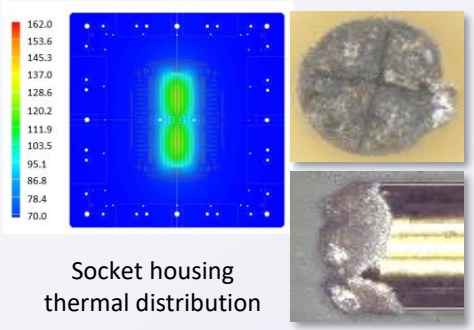
>4000W

- Socket thermal domain
- Thermal run away

IC>4000W



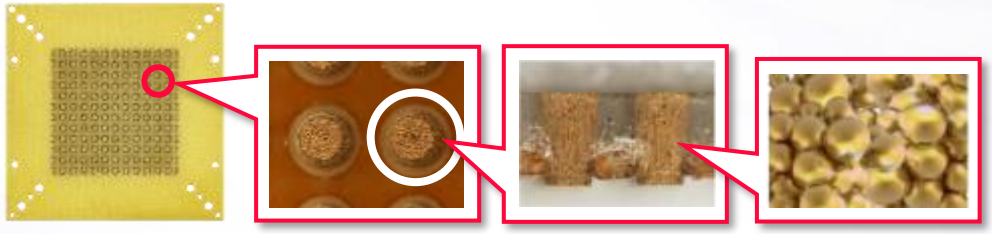
Socket Power Loss>500W



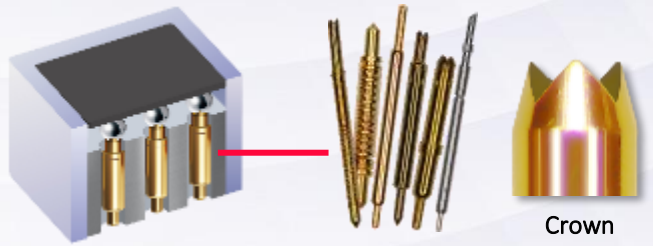
Socket housing
thermal distribution

Innovation of Hybrid Architecture / Conventional Test Interface

Elastomer



Spring probe

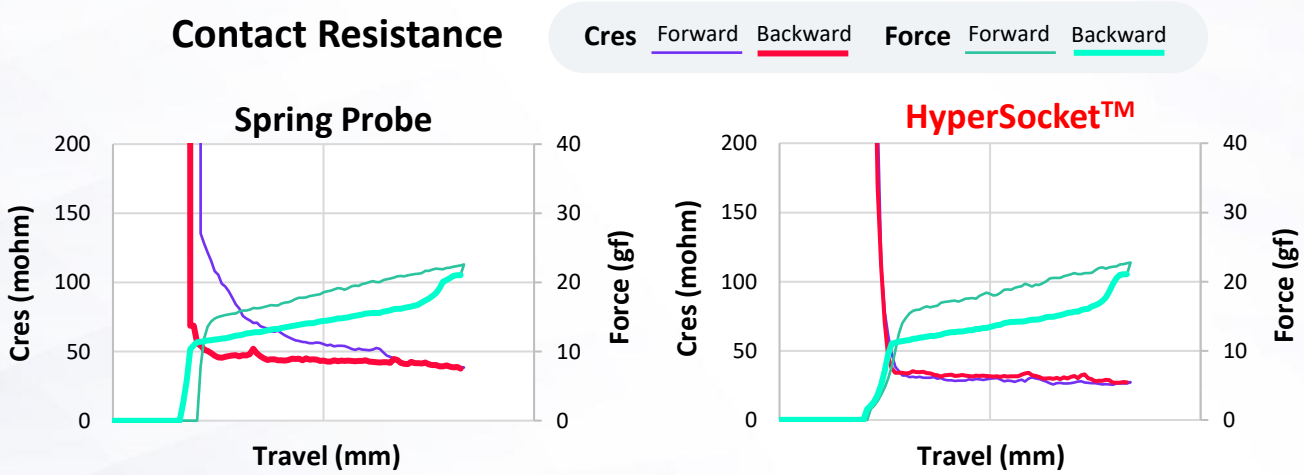


Length(mm)	0.5~2.0	**★1.5~6 even longer depend on the requirement**
Resistance (mohm)	**★ <50 (Multiple contacts)**	<60 (Design dependent, including probe structure)
Travel (mm)	0.2(Min.)~0.4(Max.)	**★ 0.35(Min.)~1.0(Max.)**
Force(g)	20~50/per bump	**★ 15~25/per pin**
CCC(A)	~4	**★ Up to 6**
Coaxial Structure	Not really applicable	**★ Applicable**
Maintenance	**★ clean by sticker**	clean by brush/clean pad/laser
Spare part	Whole piece, but easy to replace	**★ Individual probe replaeable, but take times to replace & maintenance**
Limitation	• Hard to balance lower force <20g, contact resistance and lifetime PS: Normally, reflected force varies from 30~50g/per bump • Shorter contact travel <0.4mm(Max) to cover package warpage • Shorter lifetime (can not replace individually) • No coaxial structure for large package application	• Limited four contact points of top plunger design • Need regular clean to maintain Cres • Physical damage to solder ball and pad if wrong setup

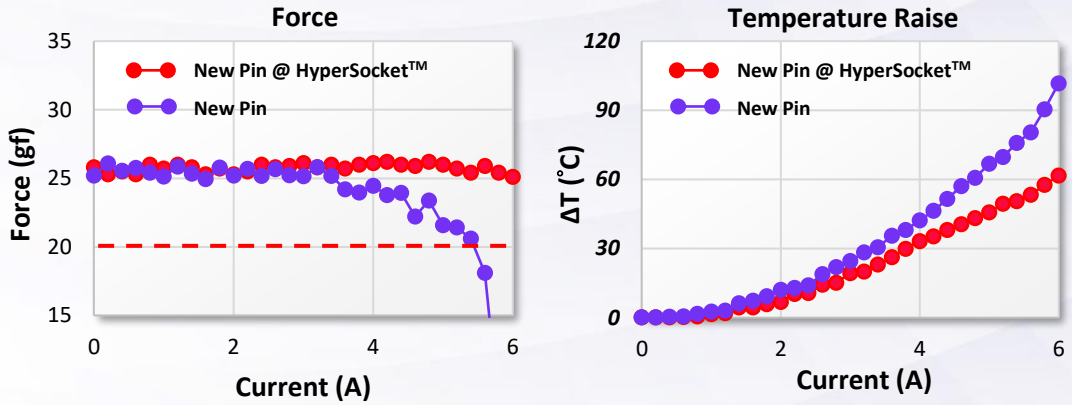
***Comparison table for pitch 0.8mm conventional test interface**

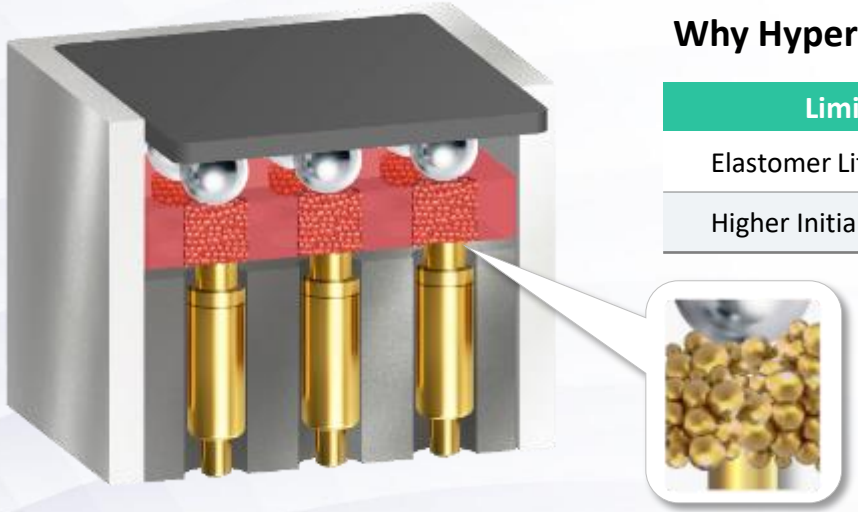
Innovation of Hybrid Architecture HyperSocket™

Contact Resistance



Current Carrying Capacity





Why HyperSocket is suitable for Advantaged Package Testing(Ultra Large Package)?

Limitation	Characteristics
Elastomer Lifetime	Significantly increase contact surface between contactor to solder ball and PCB pad
Higher Initial investment	Less and stable contact resistance ↓30%
	Higher current carrying capacity(C.C.C.) ↑30%
	Less joule heat generation by high current ↓30%
	No housing warpage of spring probe socket
	Lower total test cost of ownership: Factory operation, Hardware, Maintenance and Test interface including Change Over Kit, Socket, PCB.

Innovative Test Solution HyperSocket™

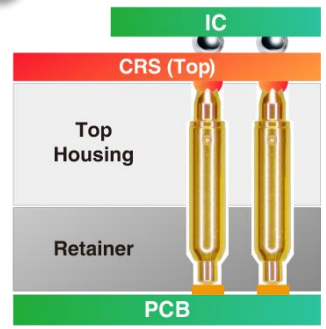
Requirements for HyperSocket™ Design

- **Package Size** >100 X 100 mm²
- **Pin count** >10,000 pin
- **Device Warpage** >0.4 mm
- **High Current Density** >6 A
- **SACQ(Frequent Clean)** ~10 TD
- **Solder Ball Melting**
- **Probe bent and worn out issue**

Patent NO.

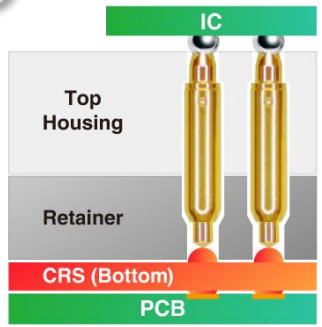
- TWI862047
- TWI922268
- TWI901181
- TWI862191
- TWI884802
- CN220584352
- TWI901161
- TWI923382
- US(Granted)

Hyper-UF



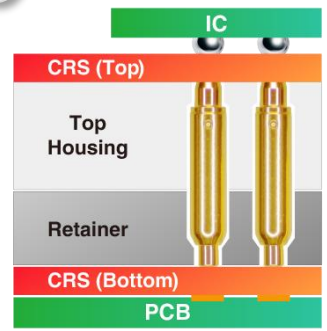
Frequent Clean, Solder Ball Melting

Hyper-LF



Ultra Large Package, High Pin Count

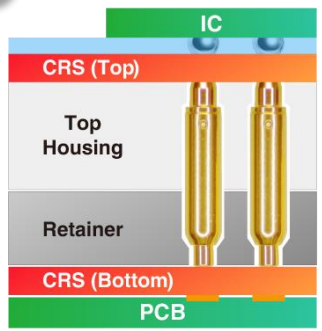
Hyper-DH



High Current Density, Probe Bent

Hyper-Liquid

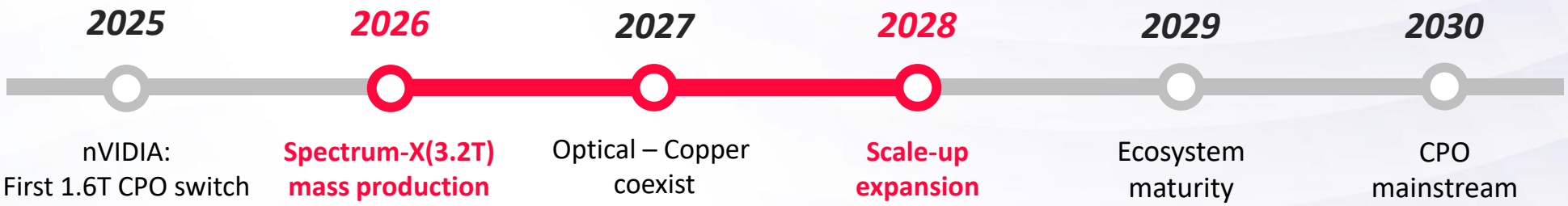
Under Validation



Extremely High Power > 2500W

Summary

CPO Market Trends & Challenges



2026 – 2028 is the golden window for ASIC platform flexibility.

One ASIC supporting both CPO and CPC —Scale-up via CPO for performance, Scale-out via pluggable for flexibility.

NVIDIA SIGNALS

- 1.6T CPO saves 180MW at million-GPU scale
- Spectrum-X: 5× efficiency, 2Tb/s, 10× reliability
- CPO and copper coexist, layered deployment

FUTURE TRENDS

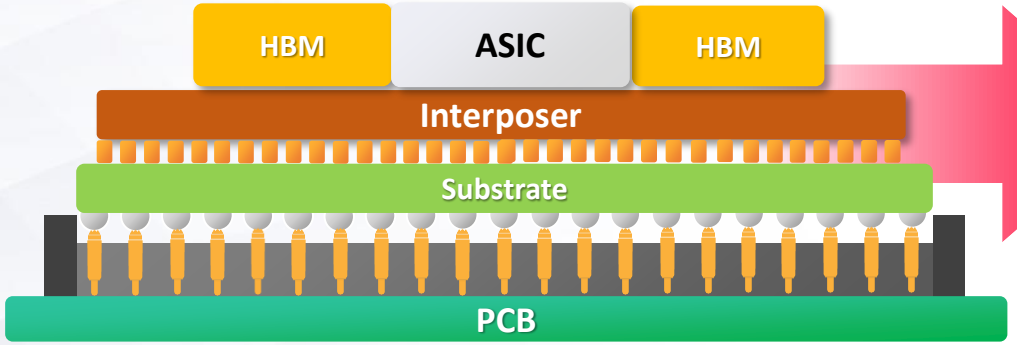
- Scale-up is the main battlefield
- Adoption: coexist → expand → mainstream
- ELS architecture, DSP-free design

CORE CHALLENGES

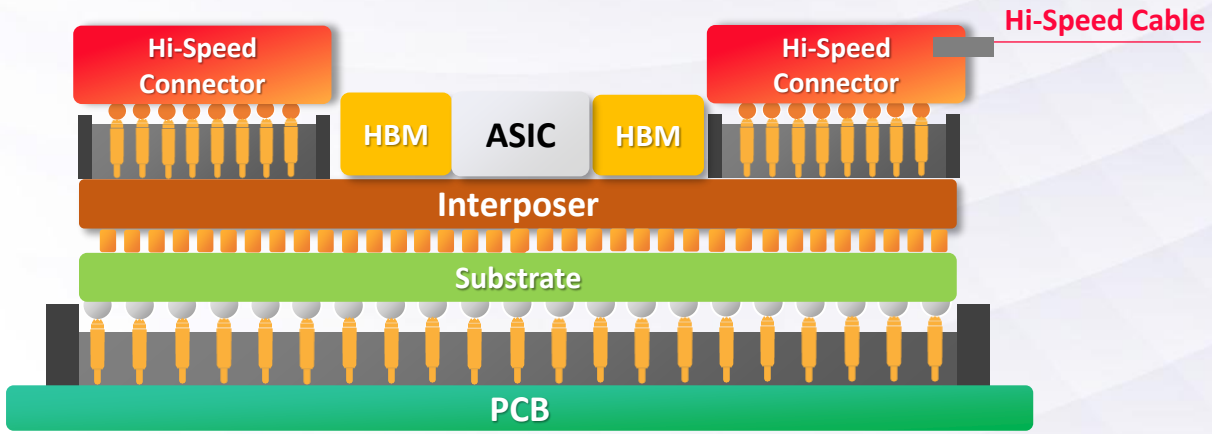
- Thermal & yield: one defect kills package
- Serviceability: operations SOP rebuilt
- Standards & cost: ecosystem immature

WinWay is Ready for CPO & CPC Testing

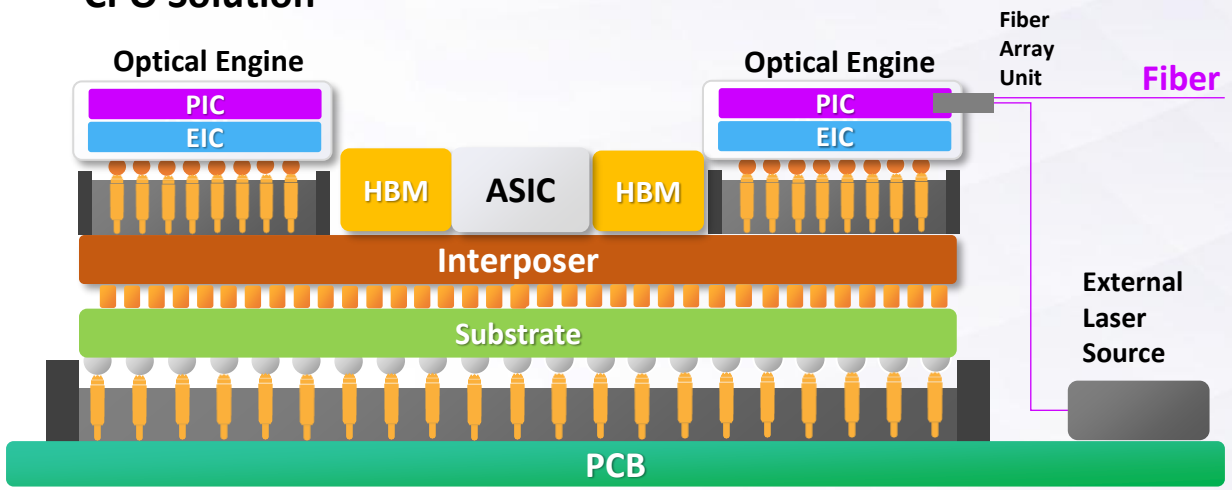
Advanced Package Test Solution



CPC Solution



CPO Solution



THANK YOU

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